# MAX 9000 Contents

November 2000

## Application Notes


AN 39 IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices
AN 41 PCI Bus Applications in Altera Devices
AN 42 Metastability in Altera Devices
AN 43 Designing with MAX 9000 Devices
AN 74 Evaluating Power for Altera Devices
AN 77 Understanding MAX 9000 Timing
AN 80 Selecting Sockets for Altera Devices
AN 81 Reflow Soldering Guidelines for Surface-Mount Devices
AN 85 In-System Programming Times for MAX Devices
AN 95 In-System Programmability in MAX Devices
AN 100 In-System Programmability Guidelines


## Catalogs


Intellectual Property Catalog
LPM Quick Reference Guide


## Data Sheets


Altera Device Package Information Data Sheet
Altera Programming Hardware Data Sheet
BitBlaster Serial Download Cable Data Sheet
ByteBlaster Parallel Port Download Cable Data Sheet
ByteBlasterMV Parallel Port Download Cable Data Sheet
Configuration Elements Data Sheet
MAX 9000 Programmable Logic Device Family Data Sheet
MasterBlaster Serial/USB Communications Data Sheet
Operating Requirements for Altera Devices Data Sheet
QFP Carrier & Development Socket Data Sheet

## General Information

Introduction (to the Altera ***1999 Data Book***)
Ordering Information

## Product Information Bulletins

PIB 24 Advantages of ISP-Based PLDs over Traditional PLDs
PIB 26 Concurrent Programming through the JTAG Interface for MAX Devices

## Selector Guides

Component Selector Guide

## Technical Briefs

TB 28 Advantages of ISP-Based CPLDs
TB 32 ISP Programming Methods & Ordering Codes