MIPS-Based Embedded Processor Device Overview

EXCALIBUR™

Preliminary Information

MIPS TECHNOLOGIES

Features…

- Industry-standard MIPS32™ 4Kc™ 32-bit RISC processor core operating at up to 166 MHz
  - Memory management unit (MMU) included for real-time operating system (RTOS) support
  - Single-cycle 16×16 multiply divide unit (MDU)
  - 32-bit MIPS® RISC processor instruction set, user-level compatible with the R3000® and R4000® (32-bit mode)
- Part of the Altera® Excalibur™ embedded processor solutions: system-on-a-programmable-chip (SOPC) architecture (see Figure 1 on page 4) builds upon features of the APEX™ 20KE family of PLDs, with up to 1,000,000 gates (see Table 1 on page 2)
- Advanced memory configuration support
  - Harvard cache architecture with separate 16-Kbyte instruction and 16-Kbyte data caches
  - Internal single-port SRAM up to 256 Kbytes
  - Internal dual-port SRAM up to 128 Kbytes
  - External SDRAM 133-MHz data rate (PC133) interface up to 512 Mbytes
  - External dual data rate (DDR) 266-MHz data rate (PC266) interface up to 256 Mbytes
  - External flash memory up to 32 Mbytes
- Expansion bus interface (EBI) is compatible with industry-standard flash memory, SRAMs, and peripheral devices
- Advanced bus architecture based on advanced microcontroller bus architecture AMBA high-performance bus (AHB) interface
- Embedded programmable on-chip peripherals
  - Flexible interrupt controller
  - Universal asynchronous receiver/transmitter (UART)
  - General-purpose timer
  - Watchdog timer
- PLD configuration/reconfiguration possible via the embedded processor software
- Integrated hardware and software development environment
  - Extended Quartus™ development environment for Excalibur support
  - Altera MegaWizard® Plug-In Manager interface configures the embedded processor, PLD, bus connections, and peripherals
  - C/C++ compiler, source-level debugger, and RTOS support

Table 1. Current MIPS-Based™ Embedded Processor Device Features Note (1)			
Feature	**XM1**	**XM4**	**XM10**
Maximum system gates	263,000	1,052,000	1,772,000
Typical gates (2)	100,000	400,000	1,000,000
Logic elements (LEs)	4,160	16,640	38,400
Embedded system blocks (ESBs)	26	104	160
Maximum RAM bits	53,248	212,992	327,680
Maximum macrocells	416	1,664	2,560
Maximum user I/O pins	178	360	521
Single-port SRAM (3)	32 Kbytes	128 Kbytes	256 Kbytes
Dual-port SRAM (3)	16 Kbytes	64 Kbytes	128 Kbytes

Notes:
(1) These features are preliminary. Contact Altera for up-to-date information.
(2) The embedded IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan circuitry contributes up to 57,000 additional gates
(3) Single- and dual-port memory sizes are preliminary. Contact Altera for the most up-to-date information.

... and More Features

- Advanced packaging options including SameFrame™ pin migration (see Tables 2 and 3 on page 3)
- 1.8-V supply voltage; can interface with 1.8-V, 2.5-V, and 3.3-V devices
- Fully configurable memory map
- Extensive embedded system debug facilities
    - SignalTap® embedded logic analyzer
    - Software debug monitor
    - Enhanced IEEE Std. 1149.1 JTAG, or EJTAG, interface to assist software debugging
- Multiple and separate clock domains controlled by software-programmable phase-locked loops (PLLs) for embedded processor, SDRAM, and PLD
- PLL features include
    - ClockLock™ feature reducing clock delay and skew
    - ClockBoost™ feature providing clock multiplication
    - ClockShift™ programmable clock phase and delay shifting

Table 2. MIPS-Based Embedded Processor FineLine™ BGA & BGA Package Sizes *Note (1)*

Feature	FineLine BGA			BGA	
	484 Pin	**672 Pin**	**1,020 Pin**	**612 Pin**	**864 Pin**
Pitch (mm)	1.00	1.00	1.00	1.27	1.27
Area (mm^2)	529	729	1,089	1,225	2,025
Length × Width (mm × mm)	23 × 23	27 × 27	33 × 33	35 × 35	45 × 45

Table 3. MIPS-Based Embedded Processor FineLine BGA & BGA Package Options & PLD I/O Counts *Notes (1), (2)*

Device	FineLine BGA			BGA	
	484 Pin	**672 Pin**	**1,020 Pin**	**612 Pin**	**864 Pin**
XM1	173 *(3)*	178 *(3)*		178	
XM4		275 *(4)*	360	215	360
XM10			521		365

Notes to tables:

(1) Contact Altera for up-to-date information on package availability.

(2) I/O counts include dedicated input and clock pins.

(3) All FineLine BGA packages, except the 1,020-pin packages, are footprint-compatible via SameFrame pin-out. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across device densities and pin counts. Device migration is fully supported by Altera development tools.

(4) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

General Description

Part of Altera's Excalibur solution, the MIPS-based embedded-processor devices combine an unrivalled degree of integration and programmability. The MIPS-based devices are outstanding embedded system development platforms, providing embedded-processor and PLD performance that is leading edge, yet cost efficient.

The MIPS-based devices are offered in a variety of PLD densities and memory sizes to fit a wide range of applications and requirements. Their high-performance, flexible embedded architecture is ideal for compute-intensive and high data-bandwidth applications.

Figure 1 shows the structure of the MIPS-based devices. The embedded processor stripe contains the MIPS processor core, peripherals, and memory subsystem. The amount of single- and dual-port memory varies as shown, and as listed in Table 1 on page 2. Figure 2 on page 5 shows the system architecture of the stripe, and its interfaces to the PLD portion of the devices. This architecture allows stripe and PLD to be optimized for performance, enabling maximum integration and system cost reductions.
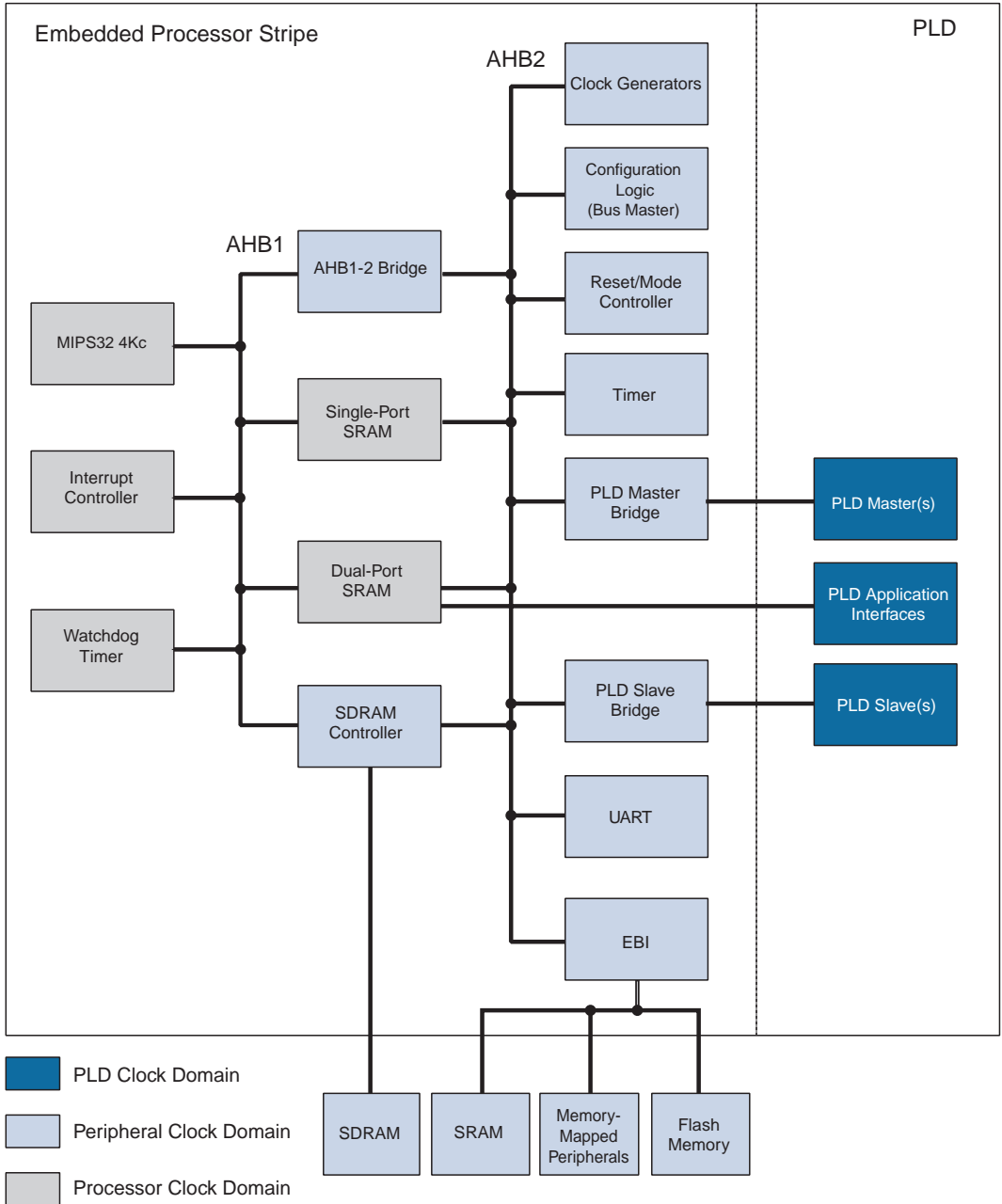
Figure 1. MIPS-Based Embedded Processor PLD Architecture   Note (1)
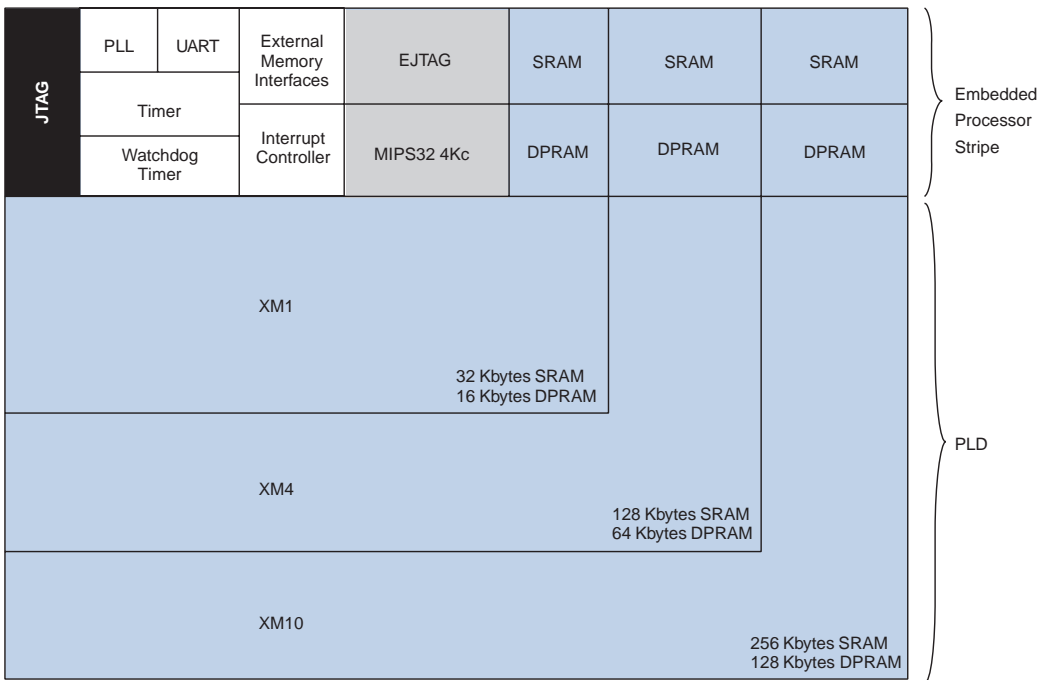
Note:
(1)   Single- and dual-port memory sizes are preliminary. Contact Altera for the most up-to-date information.

Figure 2. MIPS-Based System Architecture

Two AMBA-compliant AHB buses ensure that MIPS-based embedded processor activity is unaffected by peripheral and memory operation. Three bidirectional AHB bridges enable the peripherals and PLD to exchange data with the MIPS-based embedded processor.

The performance of the MIPS-based family is not compromised by the addition of the interfaces to or from the embedded logic, and is equivalent to an ASIC implementation of the MIPS32 4Kc on a 0.18-µm CMOS process. The 32-bit MIPS RISC processor instruction set is binary-compatible with many other MIPS family members.

MIPS-based embedded processor devices are supported by Altera's Quartus development system, a single, integrated package that offers HDL and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

The Quartus software provides NativeLink™ interfaces to other industry-standard PC- and UNIX workstation-based EDA tools. For example, designers can invoke the Quartus software from within third-party design tools. Further, the Quartus software contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for MIPS-based embedded processor devices.

Functional Description

The MIPS-based embedded processor PLDs have a system architecture (embedded processor bus structure, on-chip memory, and peripherals) that combines the advantages of ASIC integration with the flexibility of PLDs.

MIPS-Based Embedded Processor

Figure 3 shows the MIPS32 4Kc embedded processor block diagram.

Figure 3. MIPS32 4Kc Embedded Processor Block Diagram
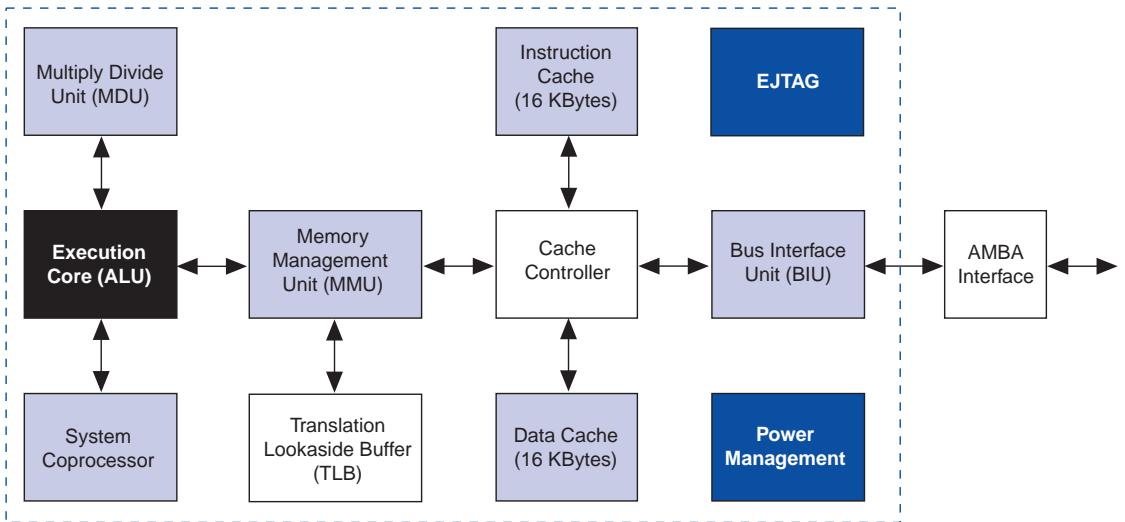
The MIPS32 4Kc is a member of the MIPS32 family of processor cores, with Harvard architecture implemented using a five-stage pipeline. Most instructions execute in one clock cycle. The architecture includes four execution units:

- Integer unit (arithmetic logic unit and shifter)
- Multiply divide unit (MDU) that supports multiply accumulate (MAC) instructions
- Branch control
- Processor control: privileged architecture functions and exception model

Independent of PLD configuration, the embedded processor can:

■ Access external boot memory
■ Boot and run
■ Program/reprogram the PLD without corruption of memory
■ Run interactive debugging
■ Detect errors and restart/reboot/reprogram the entire system as necessary
■ Communicate with the external world and receive PLD updates
■ Run a real-time operating system

PLD Interfaces

The PLD can be configured via the configuration interface or the embedded processor. It can implement:

■ Additional peripherals that connect to the embedded bus as masters, slaves, or both
■ Coprocessors sharing the embedded logic as well as on-chip and off-chip memories
■ Standard interface to on-chip dual-port RAM (allowing SRAM to function as a 'large' embedded system block (ESB))
■ Additional embedded processor interrupt sources and controls

The master/slave/memory ports are synchronous to the PLD clock domain; however, the embedded processor domain and PLD domain can be asynchronous, to allow optimized clock frequencies for each domain. Resynchronization across the domains is handled by the AHB bridges in the embedded processor stripe.

Both the PLD master interface and the embedded processor-to-PLD slave interface are capable of supporting 32-bit data accesses to the whole 4-Gbyte address range (32-bit address bus).

The PLD can take full advantage of the extensive range of Altera intellectual property (IP) MegaCore® functions, reducing time-to-market and enabling complex SOPC designs.

PLLs

The device PLLs build on the PLL features of the APEX 20KE devices. Within the PLD, four PLLs are available. The PLLs can be configured in a manner similar to APEX 20KE PLLs.

In addition to the four APEX-style PLLs, MIPS-based embedded processor PLDs have two PLLs that are frequency-programmable—both at configuration and via the system bus—to provide clocks for the:

■ Embedded processor and associated modules
■ Memory controller

The additional PLLs and associated routing support the following features:

■ A common source for running additional PLLs
■ Clock generation for the embedded processor and memory subsystem, allowing a synchronous mode
■ LVTTL 2.5-V and 3.3-V clock input
■ PLL disabling, which allows the raw input clock to be routed as the main clock source

The memory controller PLL allows users to tune the frequency of the system clock to the speed of the external memory implemented in their systems.

External Memory Controllers

The MIPS-based embedded processor PLDs provide two embedded memory controllers that can be accessed by any of the bus masters: one for external DRAM, and a second for external flash memory or SRAM.

The DRAM memory controller supports the following commonly-available memory standards (SDRAM and DDR), without the addition of any glue logic:

■ SDRAM 133-MHz data rates
■ DDR 266-MHz data rates

A software-programmable PLL is used within the DRAM memory controller subsystem to supply the appropriate timings. Users can program the frequency to match the chosen memory components.

A second memory controller supports the interface to system ROM, allowing external flash memory access and reprogramming. In addition, static RAM and simple peripherals can be connected to this interface externally.

Peripherals

The following peripherals are connected to the AHB:

- UART
- Timer
- Watchdog timer
- Interrupt controller

Software Development Tools

The target software development tools offered by Altera are a combination of GNUPro tools and Altera tools. The MIPS-based embedded processor device is compatible with tools available from third parties for the MIPS32 4Kc processor core.

The development tools include:

- GNUPro tool suite
    - Graphical debugger
    - C/C++ compiler
    - Assembler
    - Linker
- Quartus support
    - C/C++ text editor
    - Software mode to build applications

Figure 4 shows the Quartus development tool flow.

Figure 4. Quartus Development Tool Flow
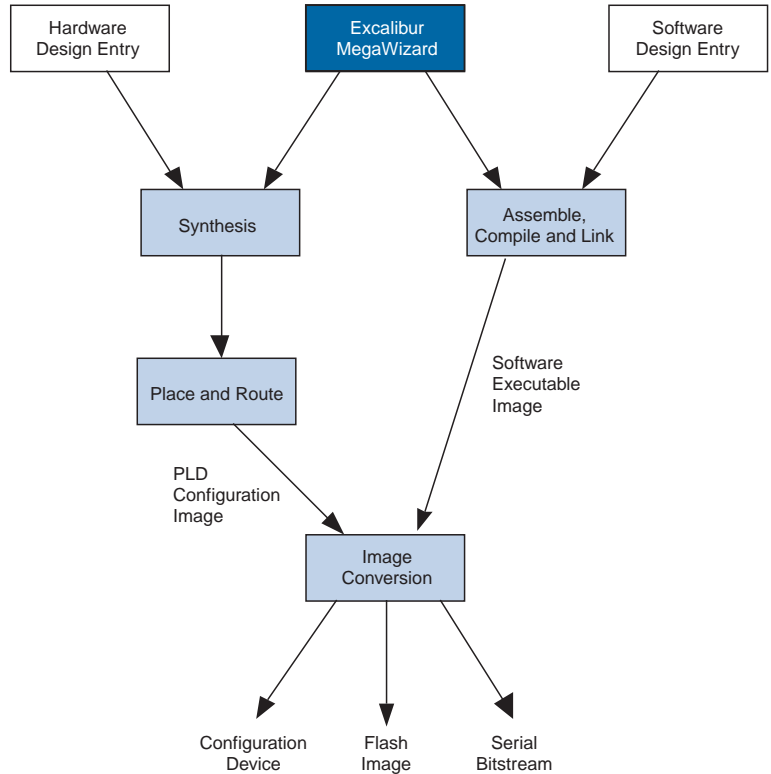
Altera supplies a variety of embedded software functions to support flash memory programming and PLD configuration. In addition, Altera provides device drivers for the on-chip peripherals, and drivers to support PLD logic peripherals.

MIPS-based embedded processor PLDs are configured at system power-up with data stored in a configuration device or flash memory. The same memory can also be used to store the application software for the embedded processor. The user can reconfigure the device in-circuit using the on-chip processor, using configuration data stored anywhere in its memory system. The user can make real-time changes during system operation, which enables innovative reconfigurable computing applications.

Configuration Wizard

The Altera Quartus development environment is enhanced by an Excalibur configuration wizard that allows pre-runtime setup of hardware and software functions. Figure 5 shows a typical set of screen shots from the configuration wizard, demonstrating how users can, for example, select clock frequencies and booting options, and specify peripherals. This information is used to prepare a configuration bitstream that configures the PLD setup registers and on-chip SRAM as part of the configuration bitstream.

Figure 5. Excalibur Configuration Wizard
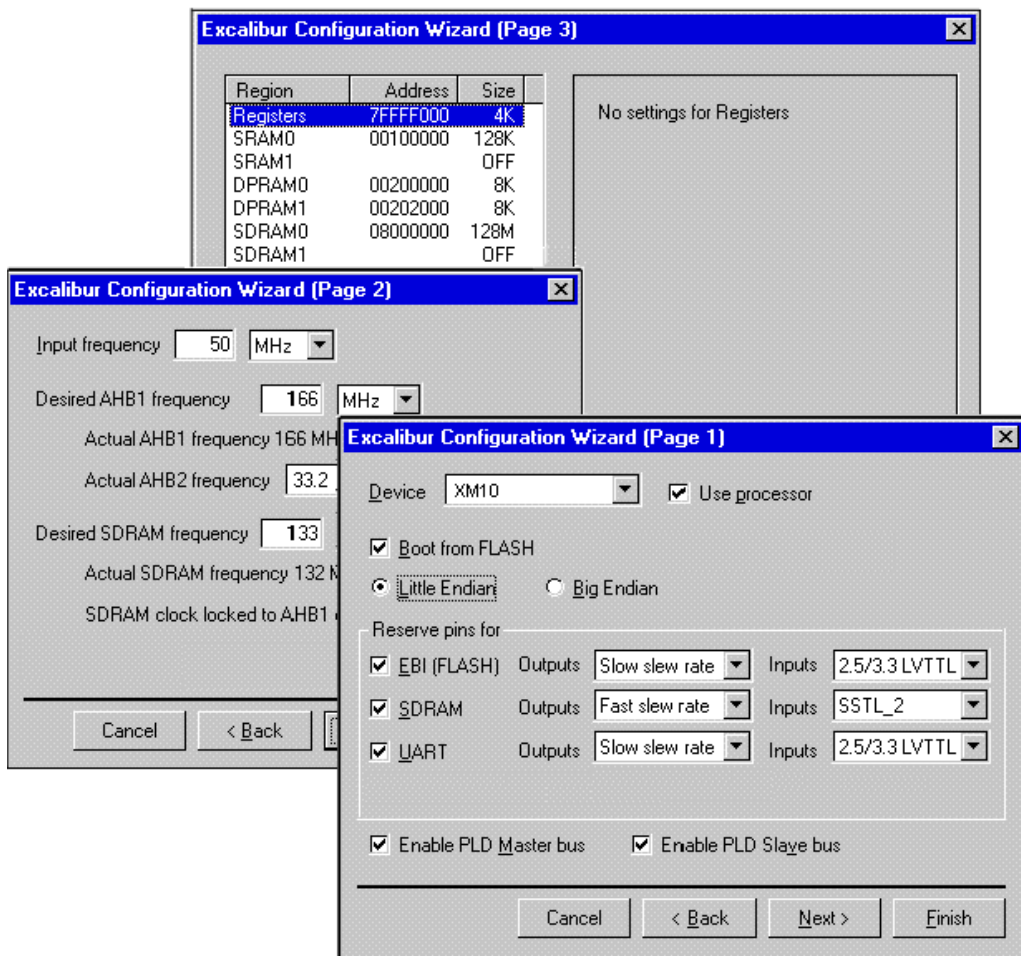
Simulation Model

Initial simulation models of the MIPS32 4Kc are compatible with the following simulators:

■ Quartus simulator
■ Verilog XL simulator
■ Model*Sim* simulator
■ Synopsys VSS simulator

Evaluation Board

Altera offers separately an evaluation board compatible with the MIPS-based embedded processor PLDs, along with high-performance memories, debug interfaces, PCI bus connections, and a capability for prototyping physical interfaces. Figure 6 illustrates the Altera evaluation board, showing the provision for board expansion.

Figure 6. MIPS-Based Evaluation Board
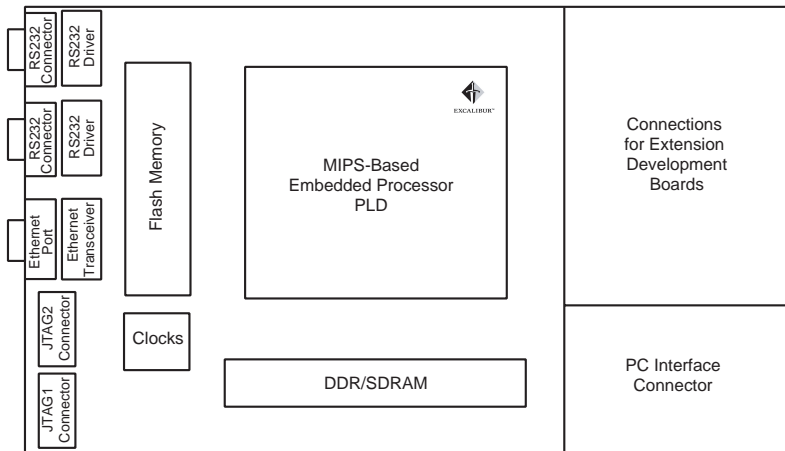
Typical Application

Figure 7 shows how the MIPS-based embedded processor and other elements can be integrated on a device. In this example, the MIPS 32 4Kc embedded processor device is configured for a voice-over packet gateway application. The elements of the embedded processor stripe, PLD modules, and off-chip peripherals are clearly identified.

Figure 7. MIPS-Based Embedded Processor Device in a Voice-Over Packet Gateway Application
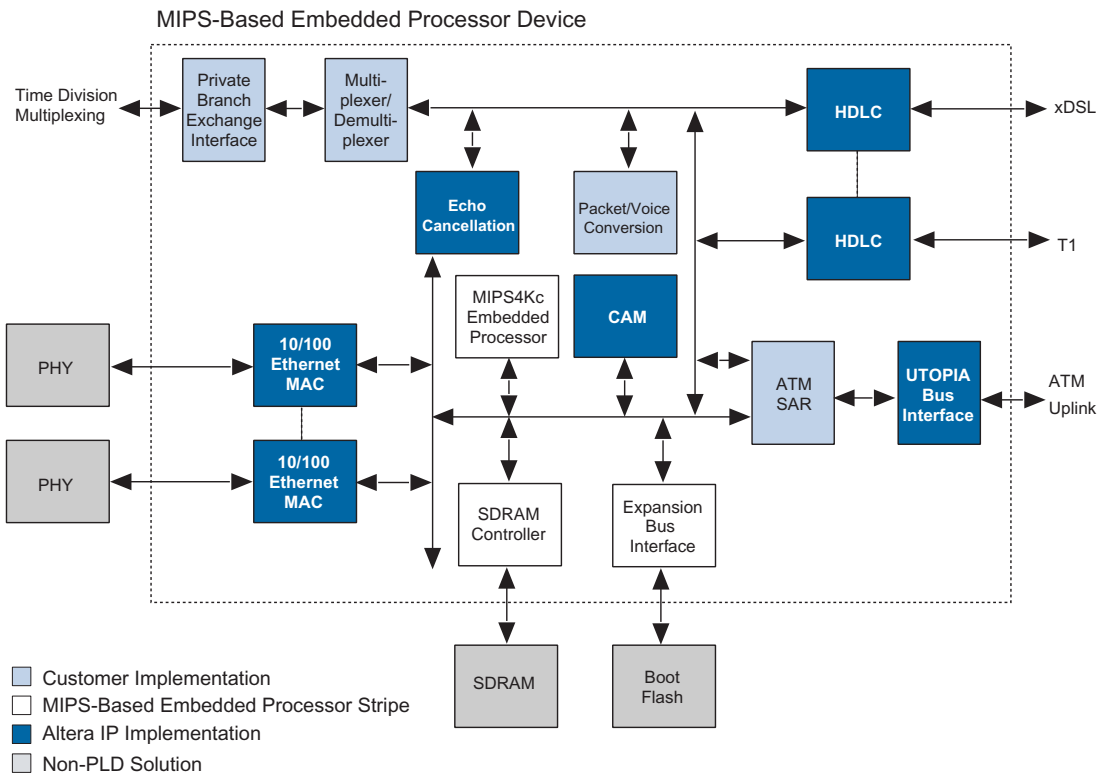
Revision History

This version provides updated information, including:

■ Revised maximum amount of external SDRAM supported

Notes:

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