Targeting Altera with FPGA Express

Synopsys' FPGA Express and Altera's MAX+PLUS II tools are tightly integrated to provide designers with a seamless design flow.

This application note describes a flow for designers to achieve the best results using Altera's industry-leading FLEX and MAX family devices.

Design Entry
Create VHDL or Verilog design files using any text editor, including those built into MAX+PLUS II and FPGA Express.

LPM Usage
FPGA Express supports LPMs (Library of Parameterized Modules). Designers can instantiate various LPMs in the HDL code as parameterized black boxes, or allow FPGA Express to infer LPMs. For FLEX synthesis, FPGA Express infers LPMs from relational operators with non-constant operands and multiplication operands. For MAX synthesis, LPMs are inferred from all relational and arithmetic operands.

Memory Usage
Altera recommends instantiating memory functions using LPMs. Memory functions supported include RAM, ROM, CSDPRAM and CSFIFO. Designers may also use Altera-provided genmem utility for memory instantiation.

For the best use of resources, FPGA Express also enables you to map logic functions into FLEX EABs. Please refer to the FPGA Express help for more information.

Synthesis
To achieve best results from FPGA Express select any or all of the options listed below.

In FPGA Express, from the menu item Synthesis – Options, under Project tab select:
- One-hot FSM encoding style for FLEX devices, and binary FSM encoding style for MAX devices.
- "fastest & smallest" interpretation of VHDL 'when others' for FSM synthesis.
- Turn OFF the option "Insert LCELL buffers, style WYSIWYG (Altera FLEX only)". However, for faster compilation time in MAX+PLUS II, it is recommended to turn this option ON. There may be a slight decrease in performance by turning this option ON.

From the Create Implementation dialog box, select
- Effort – High
- Set the "Optimize for" switch to match your design goals

Place and Route
To compile the design in MAX+PLUS II, use the assignments and constraints file (.acf file) and library mapping file (.lmf file) generated by FPGA Express.

If "Insert LCELL buffers" option was OFF in FPGA Express, then MAX+PLUS II uses FAST synthesis style, otherwise WYSIWYG synthesis style is used.

For MAX devices, if a design does not fit then from the menu item Assign – Global Project Logic Synthesis, select option Multi-Level Synthesis for MAX 5000/7000 and/or 9000 devices.

For detailed information on any of the topics discussed above, please refer to Altera's ACCESS Key Guidelines (http://www.altera.com/html/maxkey/synopsys/fpgaex/fpexpg.htm)