LVDS Comparison

APEX 20KE vs.Virtex-E Devices

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Introduction

The low-voltage differential signaling (LVDS) input/output (I/O) standard is a data interface standard that supports high-speed data transfers. Unlike other single-ended voltage standards, such as the complementary metal-oxide semiconductor (CMOS) standard or the transistor-to-transistor logic (TTL) standard, LVDS uses differential signals. Differential signals increase noise margins, design performance, and design reliability. LVDS also allows a reduced signal swing resulting in shorter switching times and higher bandwidth.

This product information bulletin compares the LVDS solutions offered by APEX 20KE™ devices and Virtex-E devices and shows how APEX 20KE devices offer better LVDS solutions than Virtex-E devices. The following topics are discussed:

- LVDS I/O standard
- Overview of LVDS features
- LVDS receiver implementation
- LVDS transmitter implementation
- LVDS timing specifications
- LVDS software support
- Board level issues

LVDS I/O Standard

Table 1 compares the LVDS I/O standard to other differential I/O standards.

Table 1. Comparison of LVDS to Other Differential I/O Standards			
Standard	**Voltage Swing**	**Common Mode Voltage (V)**	**Speed** *(1)*
LVDS *(2)*	350 mV	0.2 to 2.2	>1 Gbps
ECL/PECL *(3)*	300–600 mV	2.0 to 2.5	500 Mbps
PCML *(4)*	450 mV	3.0 to 3.3	622 Mbps
USB *(5)*	2.5 V	0.8 to 2.5	480 Mbps

Notes:
(1) Gbps: gigabits per second; Mbps: megabit per second.
(2) The LVDS I/O standard specifications are derived from the TIA/EIA-644 standard and the IEEE 1596.3 standard.
(3) Emitter-coupled logic (ECL) and positive emitter-coupled logic (PECL) are differential I/O standards used for low skew clock networks and for transferring data.
(4) Pseudo current mode logic (PCML) is a differential I/O standard that is used for low power applications.
(5) Universal serial bus (USB) is a differential I/O standard used in PC peripherals.

Compared to other differential I/O standards, LVDS has the fastest data transfer speed and the lowest power consumption, which makes it the best solution for physical layer interfaces.

APEX 20KE devices support the LVDS standard via the True-LVDS™ I/O interface. The True-LVDS interface supports up to 16 data channels at high-speed data transfer rates as fast as 840 Mbps. The True-LVDS interface also supports a differential LVDS clock input to synchronize data transfers. APEX 20KE devices have built-in True-LVDS receivers and True-LVDS transmitters that are coupled to LVDS receivers and LVDS drivers. By using internal phase-locked loops (PLLs), the True-LVDS receivers and True-LVDS transmitters offer 1×, 4×, 7×, or 8× data transfer modes. Additional deskew circuitry corrects board-level skew between the data and the clock for accurate data capture.

For more information, see the *Using LVDS in APEX 20KE Devices White Paper*.

Four Xilinx application notes, *XAPP230: The LVDS I/O Standard*, *XAPP231: Multi-Drop LVDS with Virtex-E FPGAs*, *XAPP232: Virtex-E LVDS Drivers & Receivers Interface Guidelines*, and *XAPP233: Multi-channel 622 MHz LVDS Data Transfer with Virtex-E Devices*, describe LVDS emulation in Virtex-E devices. However, an analysis of LVDS capability in Virtex-E devices shows that the LVDS implementation can only support medium speed LVDS data transfer rates; unlike APEX devices, Virtex-E devices cannot support high speed LVDS data transfer rates.

Overview of LVDS Features

This section describes and compares LVDS features for APEX 20KE devices and Virtex-E devices.

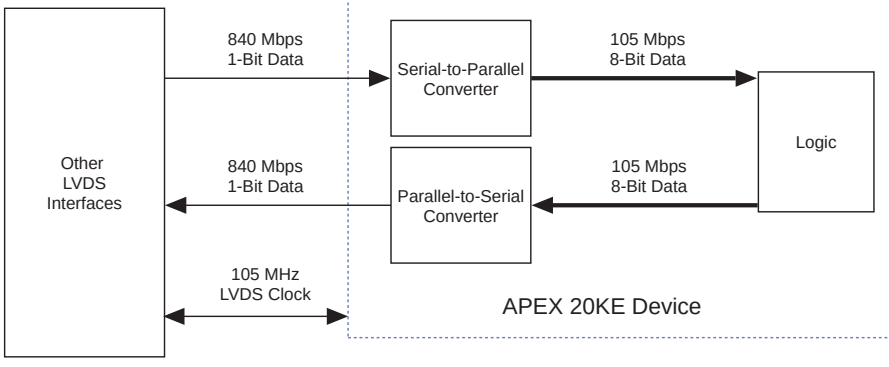
True-LVDS Features in APEX 20KE Devices

APEX 20KE devices include the following LVDS features:

- Dedicated True-LVDS circuitry incorporated at the silicon level
  - Facilitates LVDS implementation
  - Ensures that complex timing issues are met with minimal design efforts
- Dedicated True-LVDS receiver circuitry and True-LVDS transmitter circuitry
  - Supports multiple channels
  - Performs the critical serial-to-parallel and parallel-to-serial conversions required to convert high-speed LVDS signal rates to system speeds
- Special-purpose PLLs
  - Supports several LVDS data transfer modes, including the 1×, 4×, 7×, and 8× data transfer modes
  - Allows APEX 20KE devices to interface with the industry-standard 78-MHz clock
- Deskew Circuitry
  - Implements the deskew feature to ensure accurate data capture and to compensate for board-level skew

Together, these features combine to create a robust LVDS solution. Figure 1 shows a True-LVDS interface example in an APEX 20KE device that operates at 840 Mbps.

Figure 1. APEX 20KE True-LVDS Interface Example



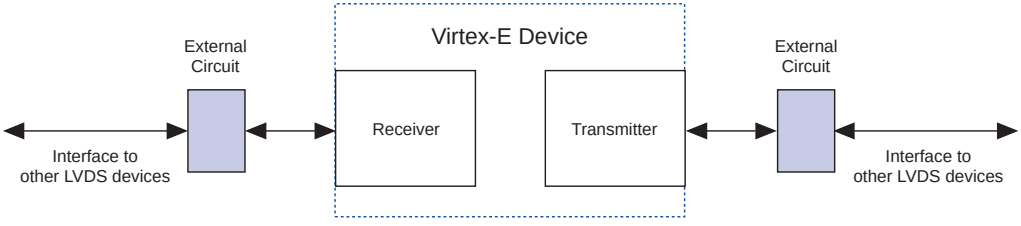
LVDS in Virtex-E Devices

Virtex-E devices include the following LVDS features:

- Emulated LVDS
  - No dedicated LVDS circuitry at the silicon level
- Emulated LVDS receiver and LVDS transmitter
  - Consumes device resources, such as block RAMs
  - Reduces Virtex-E device capacity
- 311-MHz LVDS clock
  - No direct interface with other standard LVDS devices because standard devices require a 78-MHz LVDS clock
- Delay-locked loops (DLLs)
  - Supports only 1× and 4× data transfer modes
  - Needs an external device, such as the XCV50E device, for the 8× mode
  - Needs to derive a 4× clock by cascading two DLLs inside the XCV50E device
  - Increases clock jitter due to the DLLs
- Does not support the 7× data transfer mode
  - Cannot interface with industry-standard devices, such as the National Semiconductor LVDS interface that use 7× mode

Figure 2 shows an LVDS interface example in a Virtex-E device.

Figure 2. Virtex-E LVDS Interface Example



Comparison of Available Data Transfer Modes

Table 2 compares the available data transfer modes in APEX 20KE devices and Virtex-E devices.

Table 2. Comparison of Available Data Transfer Modes

Data Transfer Mode	APEX 20KE	Virtex-E *(1)*
1×	✓	✓
4×	✓	✓
7×	✓	–
8×	✓	Requires external circuitry

Note:
(1) Data transfer modes are based on the Virtex-E LVDS implementation described in the Xilinx *Application Note XAPP233: Multi-channel 622 MHz LVDS Data Transfer with Virtex-E Devices*.

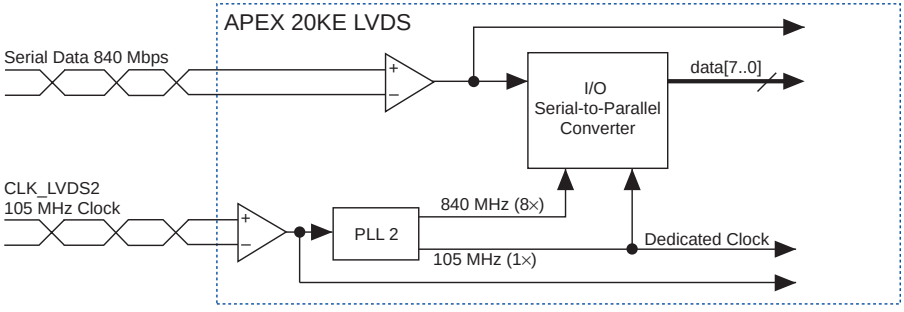
LVDS Receiver Implementation

This section compares LVDS receiver implementation for APEX 20KE devices and Virtex-E devices.

APEX 20KE True-LVDS Receiver Implementation

The APEX 20KE True-LVDS receiver is implemented in dedicated LVDS circuitry. Figure 3 shows an example of a True-LVDS receiver in an APEX 20KE device operating at 840 Mbps, in 8× transfer mode.

Figure 3. True-LVDS Receiver Circuit in an APEX 20KE Device



The True-LVDS receiver accepts a 105-MHz clock. This clock is multiplied with a PLL to create an internal 840-MHz clock. This 840-MHz clock samples data and converts the serial data to parallel data by using a dedicated serial-to-parallel converter circuit. Internal logic can access the parallel data. The LVDS PLL can be configured for 4×, 7×, or 8× clock multiplication, allowing the receiver to support the 4×, 7×, or 8× transfer modes. The True-LVDS receiver can support up to 16 data channels that each run at speeds of up to 840 Mbps.

Virtex-E LVDS Receiver Implementation

Because Virtex-E devices do not have dedicated LVDS circuitry at the silicon level, the LVDS receiver and the LVDS transmitter must be designed separately. *XAPP233: Multi-channel 622 MHz LVDS Data Transfer with Virtex-E Devices* describes an LVDS receiver implementation that has been validated only by software emulation. Analysis of the LVDS receiver implementation suggests that it would have difficulty operating at 622 Mbps in a real design.

The LVDS receiver implementation described in *XAPP233* requires an on-board clock running at 311 MHz to achieve a data rate of 622 Mbps. Each data channel requires two registers that are clocked by the rising edges and the falling edges of the 311-MHz clock. The data captured by these two registers is passed on to two 4-bit registers that act as a serial-to-parallel converter. A prescaler, consisting of two cascaded multiplexers, steps the clock frequency down to 155 MHz. Then the 155-MHz clock clocks the parallel data that will be stored in a block RAM. The receiver also requires an external clock running at 77.75 MHz to shift data out of the block RAM.

To achieve a 622-Mbps data rate in Virtex-E devices, the signal routing between the configurable logic block (CLB) registers and the block RAM must be tightly controlled by placing the block RAM as close as possible to the CLB. This implementation requires both hand routing and hand placement and only applies to the 8× data transfer mode. Both the 1× and the 4× data transfer modes require separate implementations with different constraint files and guide files for each implementation.

Timing Issues with the Virtex-E Receiver Implementation

To equalize path delays to different registers, a dummy load is required. According to *XAPP233*, if the dummy load is placed in appropriate locations, the delays can be reduced to within a few picoseconds (ps). However, lab results show that Virtex-E devices cannot generate repeatable delays with ps accuracy.

Furthermore, since timing parameters vary with the operating conditions, dummy load placement will vary. A dummy load placement that works under one set of operating conditions may not work under different operating conditions. Therefore, the Virtex-E LVDS implementation cannot function throughout the device's operating range.

Because the Virtex-E LVDS implementation requires that the clock not use a global line, the LVDS clock is routed via the local interconnects inside the Virtex-E device. This non-global clock will have clock skew problems. *XAPP233* specifies that the maximum clock skew is 10 ps. This skew number is solely derived from software and not from any characterization data. Considering the behavior of silicon, it is very difficult to guarantee clock skew values of exactly 10 ps.

XAPP233 identifies the worst-case delay for the data captured by the 4-bit registers as 2,925 ps and the worst-case delay for the clock as 2,166 ps. This indicates a potential race condition between the clock and the data. To work correctly, the LVDS receiver implementation requires that the data and the clock delays match and adjust by using similar routing for the clock paths and the data paths. However, timing for these routing resources depends upon the operating voltage, the temperature, and the fan-out. Therefore, for valid LVDS operations, the design has to be re-routed for different devices and different operating conditions.

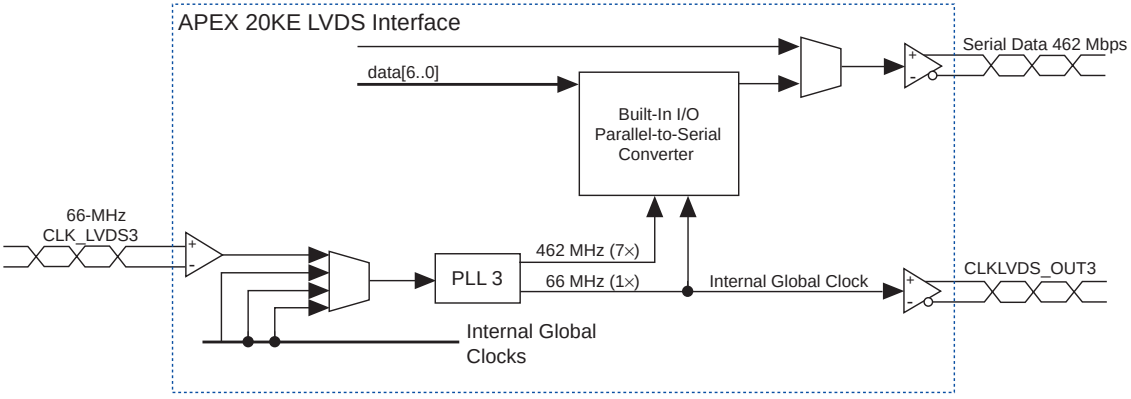
LVDS Transmitter Implementation

This section compares LVDS transmitter implementation for APEX 20KE devices and Virtex-E devices.

APEX 20KE True-LVDS Transmitter Implementation

The APEX 20KE True-LVDS transmitter is implemented in dedicated LVDS circuitry. Figure 4 shows an example of a True-LVDS transmitter circuit in an APEX 20KE device operating in the 7× data transfer mode.

Figure 4. LVDS Transmitter Circuit in an APEX 20KE Device

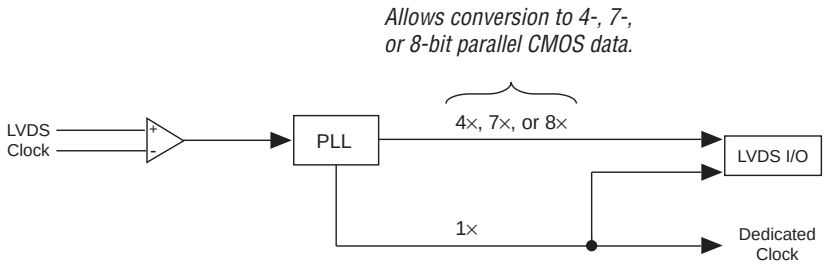


In Figure 4, the built-in parallel-to-serial converter serializes the data that will be transmitted through the differential channels.

A user can configure the APEX I/O drivers as true differential LVDS drivers that drive out the true and the complement signals for each channel. Like the True-LVDS receiver, the True-LVDS transmitter utilizes an internal PLL that offers 1×, 4×, 7×, or 8× clock multiplication.

Figure 5 shows an example of PLL functionality in an APEX 20KE device.

Figure 5. Example of PLL Functionality in an APEX 20KE Device



PLL usage ensures that both critical setup times and hold times are met. To create the LVDS clock signal, the non-multiplied output of the PLL is routed to the pins. PLL usage also minimizes skew between the data transmitted and the LVDS clock.

Virtex-E LVDS Transmitter Implementation

Like the LVDS receiver, the LVDS transmitter must be implemented with hardware emulation in the Virtex-E device. *XAPP233* describes an LVDS transmitter implementation using CLBs and block RAMs.

To transfer data at 622 Mbps, the transmitter must have an on-board clock operating at 77.75 MHz. Two cascaded DLLs are used to increase the clock frequency to 311 MHz. The parallel data is then fed to two internal shift registers, SR A and SR B, that act as a parallel-to-serial converter network. Using these shift registers and two more internal registers, A and B, alternate bits of data are fed to a multiplexer.

The 311-MHz clock, with a 3.2-ns period, controls the select line of the multiplexer. Within each clock cycle, two consecutive bits of data are streamed out using the double data rate technique. Thus, the output of the multiplexer switches at 1.6 ns (622 Mbps). A second multiplexer generates the LVDS clock output from the transmitter. This second multiplexer balances the delays associated with the clock and data paths and reduces the skew between the clock and the data signals.

Both the data and the clock signals are then inverted near the I/O element to create true and complementary outputs. The voltage swing between any signal and its complement is 2.5 V. An external, on-board voltage divider circuit, which consists of resistor packs, is used to step down the swing from 2.5 V to an LVDS voltage (maximum of 450 mV) swing.

Timing Issues with the Virtex-E Transmitter Implementation

The implementation described in *XAPP233* only works for the 8× data transfer mode. The DLL limitations do not support the industry-standard 7× mode, and the 1× and the 4× modes require separate implementations. These modes are not described in *XAPP233* and must be user-designed.

To work correctly, the LVDS implementation requires a propagation delay of less than 1.6 ns between the internal registers and the multiplexer. The delay between the shift registers and the internal registers must also be less than 1.6 ns. The minimum and the maximum delays—both of which must be met for these paths—can be met only by hand routing and with the use of constraint files and guide files. Even if a user can successfully create the guide files, both the minimum and maximum delays cannot be simultaneously satisfied.

The implementation expects the 311-MHz clock to be routed on a global line. Furthermore, the registers and the 2-to-1 multiplexers must run at 311 MHz. This high performance clock implies that the clock setup (t_{SU}), the clock hold (t_H), and the clock-to-output (t_{CO})times must be guaranteed for every register that is used in the implementation, a task that is very difficult to achieve.

LVDS Timing Specifications

This section compares the LVDS timing specifications for APEX 20KE devices and Virtex-E devices.

For accurate data transfer in data transfer modes, data synchronization is required. Various timing parameters dictate this data synchronization as well as the overall performance of the LVDS interface.

Table 3 describes the timing parameters used with LVDS.

Table 3. LVDS Timing Parameters

Timing Parameter	Description
Sampling window (SW)	SW defines the window where the internal receiver PLL clock rising edge should be placed to capture data. The setup and hold times determine the ideal strobe position within the sampling window. The input data must be valid in the sampling window
Channel-to-channel skew (t_{CCS})	t_{CCS} is defined as the timing difference between fastest and slowest output edges, including t_{CO} variation and clock skew. Skew is the variation in arrival time of two signals specified to arrive at the same time. The skew occurs on the registered output pin because of the differences in propagation delay of the clock signal through the clock network.
Receiver input skew margin (RSKM)	RSKM is the timing margin between the clock input and the data input for user board design, which allows for LVDS cable skew and jitter on the LVDS PLL. RSKM = (Bit Time Period – t_{CCS} – SW)/2

Timing Specifications for APEX 20KE True-LVDS Circuitry

Because APEX 20KE devices have dedicated True-LVDS circuitry, the True-LVDS timing parameters in APEX 20KE devices can be quantified.

Table 4 compares the timing requirements for APEX 20KE devices and Virtex-E devices.

Table 4. LVDS Timing Requirements for APEX 20KE and Virtex-E Devices

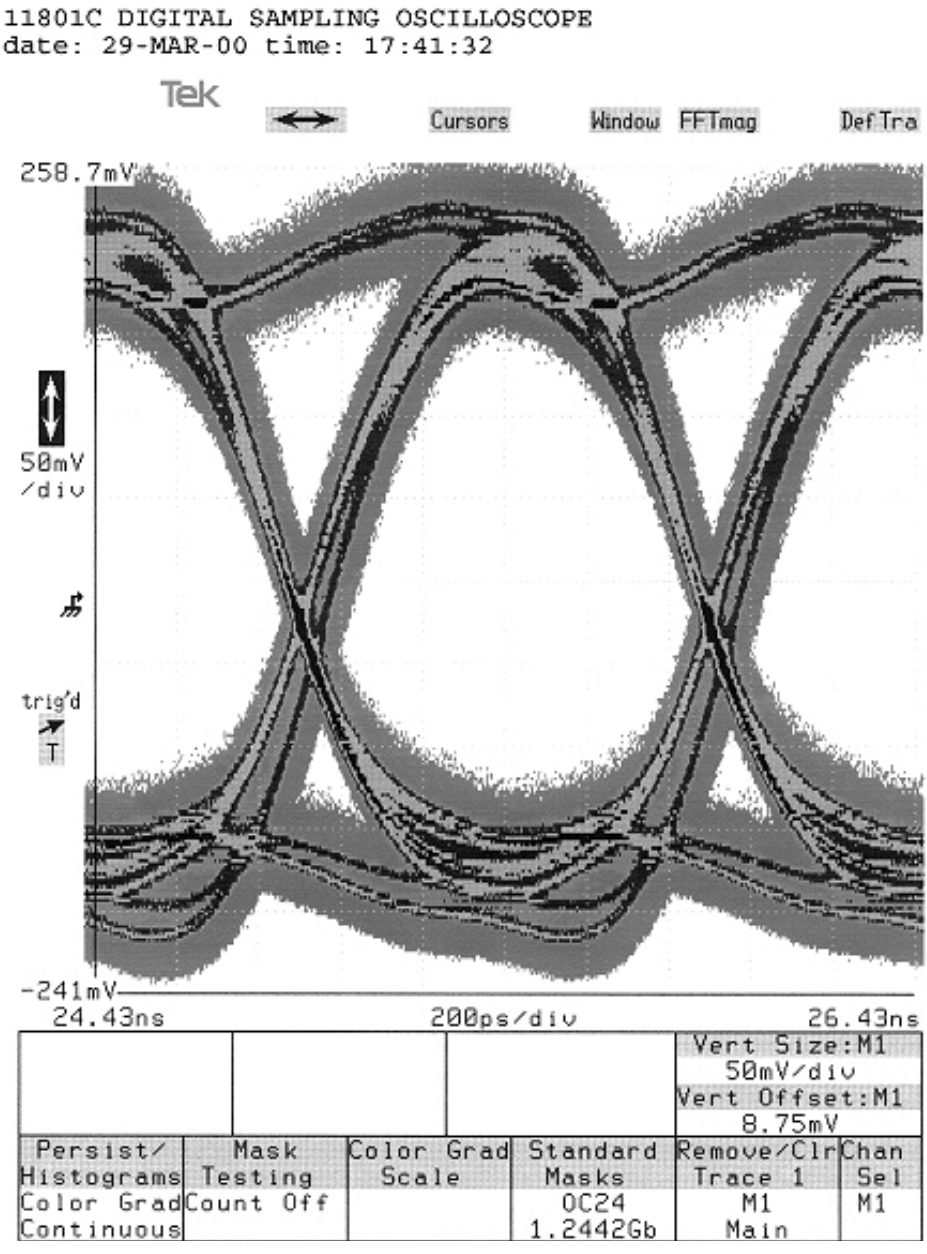
Symbol	Parameter	Mode	APEX 20KE Device (ps)		Virtex-E Device *(1)*
			Minimum	Maximum	
t_{CCS}	Transmitter output channel-to-channel skew	8×		400	N/A
		7×		400	N/A
		4×		400	N/A
RSKM	Receiver skew margin with no deskew	8× at 840 Mbps		175	N/A
		7× at 560 Mbps		343	N/A
		4× at 320 Mbps		963	N/A
RSKM	Receiver skew margin with deskew	8×		473	N/A
		7×		789	N/A
		4×		1,744	N/A
SW	Receiver input sampling window	8× at 840 Mbps	440		N/A
		7× at 560 Mbps	700		N/A
		4× at 320 Mbps	800		N/A

Note

(1) Virtex-E devices have no specified timing requirements. For more information, see the "Timing Specifications for Virtex-E LVDS" section in this document.

An "eye diagram" is a visual representation of the jitter and output driver quality of an LVDS output signal. The eye diagram is obtained by sending pseudo-random data over the LVDS channel and using a sampling oscilloscope to perform a persistence measurement. The transitions are captured and plotted over time. Horizontal eye closure is due to jitter, while vertical eye closure is due to signal attenuation or noise. Therefore a larger "eye" indicates a better quality driver. Figure 6 shows an eye diagram for an APEX EP20K400E with True-LVDS circuitry device operating at 840 Mbps in the 8× mode.

Figure 6. True-LVDS Circuitry Eye Diagram at 840 Mbps



Timing Specifications for Virtex-E LVDS

XAPP233 does not specify any timing parameters for the Virtex-E LVDS interface. Without these timing parameters, it is impossible to evaluate the LVDS performance of Virtex-E devices. The application note does mention emulation-related timings, such as setup time and hold time for different signals. However, these timing numbers are derived through a software simulation. The application note also shows waveforms that illustrate a Virtex-E LVDS operation with a 622-Mbps data transfer rate. However, these waveforms are solely derived from simulation program with integrated circuit emphasis (SPICE) simulations. These waveforms have not been verified in a Virtex-E device under lab operating conditions and do not include an eye diagram that would show I/O driver quality.

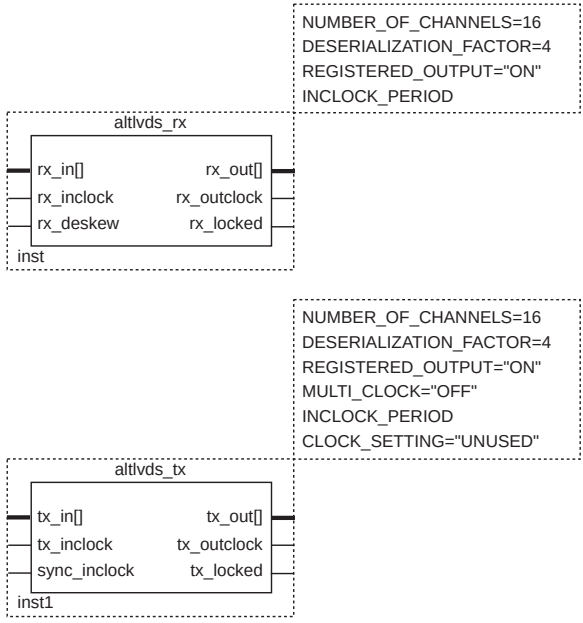
LVDS Software Support

This section compares LVDS software support for APEX 20KE devices and Virtex-E devices.

True-LVDS Software Support for APEX 20KE Devices

A user can use the Quartus™ development tool to easily implement a True-LVDS receivers and True-LVDS transmitters in APEX 20KE devices. The Quartus software features two megafunctions, `altlvds_rx` and `altlvds_tx`, that directly implement LVDS receivers and LVDS transmitters. Figure 7 shows the True-LVDS receiver and the True-LVDS transmitter megafunctions.

Figure 7. True-LVDS Receiver and True-LVDS Transmitter Megafunctions



The True-LVDS transmitter and the True-LVDS receiver megafunctions are fully customizable. The customizable parameters include the number of data channels, the deserialization factor, and the clock input frequency. Incorporating these two megafunctions within a design allows for push-button compilation of the LVDS interface and the implementation of multiple channels with data rates of up to 840 Mbps. Because True-LVDS circuits are specifically designed for and verified in silicon to satisfy all timing requirements associated with an 840-Mbps data rate, a design does not require a constraint file or a guide file. Therefore, the True-LVDS interface in APEX 20KE devices can be implemented with minimal design effort.

LVDS Software Support for Virtex-E Devices

Unlike APEX 20KE devices, Virtex-E devices do not have a drop-in solution. No LVDS software support exists, and no equivalent megafunctions are available to implement an LVDS receiver or an LVDS transmitter in a Virtex-E device. Instead, the designer must spend significant time and effort to implement the LVDS receiver and the LVDS transmitter in the software and verify that the timing meets all the specifications described in earlier sections. Because Virtex-E LVDS implementation cannot be easily scaled or modified, the software solution provided in *XAPP233* is difficult and unwieldy.

Board-Level Issues

This section compares the following board-level issues for APEX 20KE devices and Virtex-E devices:

- Deskew circuitry
- Power consumption
- DC balance
- Board layout issues
- Board level noise
- Board space

Deskew Circuitry

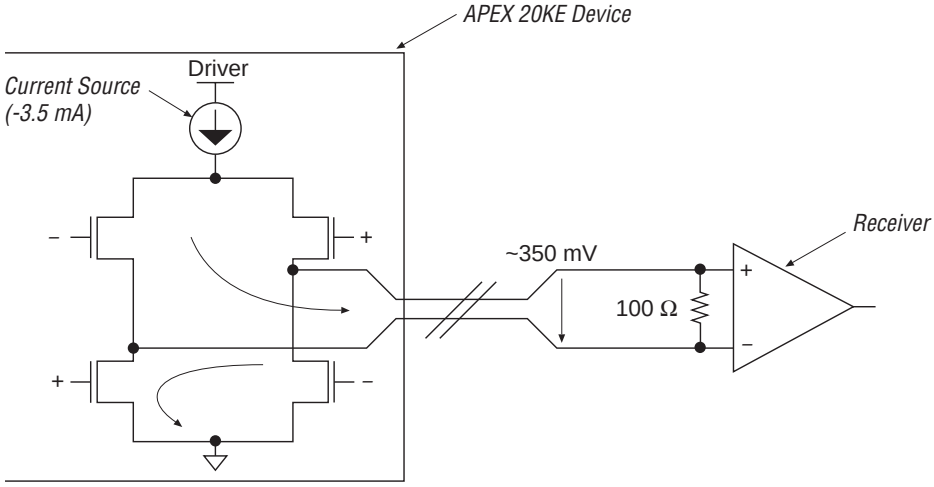
APEX 20KE devices have internal deskew circuitry that can compensate for board skew as much as ±25% of the bit time period. This deskew circuitry is an over-sampling circuit that captures the input with four separate clocks. The capture results are examined to determine which clock captured the data correctly. This clock is then used for normal operation. The deskew circuitry enables the APEK 20KE True-LVDS circuitry to work correctly and at high speeds even if there is significant board skew.

Virtex-E devices do not have any internal deskew circuitry, and therefore cannot compensate for any board-level skew. To minimize skew in Virtex-E devices, stringent board layout requirements must be applied. For example, the stringent board layout requirements will not allow timing specifications to be met and will not allow a design to be scaled easily.

Power Consumption

APEX 20KE devices have True-LVDS I/O drivers. Figure 8 shows the structure of APEX 20KE True-LVDS drivers.

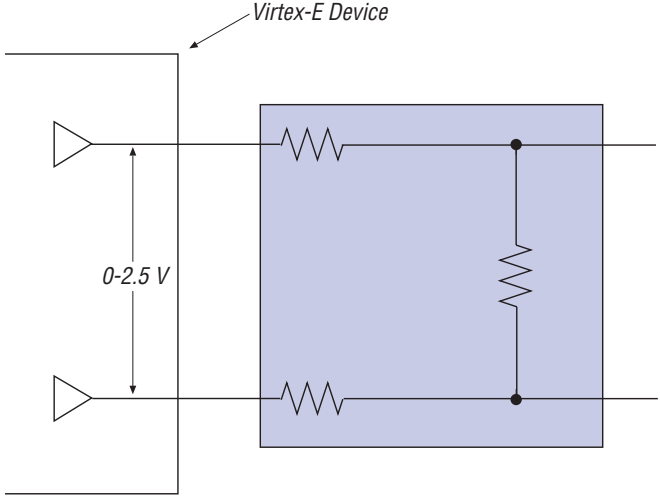
Figure 8. Structure of APEX 20KE True-LVDS Drivers



Due to the low voltage swing of 350 mV and a low DC current of 3.5 mA, the APEX 20KE True-LVDS drivers are very power-efficient.

Figure 9 shows the structure of Virtex-E LVDS drivers.

Figure 9. Structure of Virtex-E LVDS Drivers



Virtex-E devices use 2.5-V drivers. The voltage swing for the 2.5-V drivers is 2.5 V, with a typical DC current of 12 mA. In *XAPP233*, the Virtex-E LVDS implementation uses an on-board resistor divider network that consumes a minimum DC current of 8.5 mA. The on-board resistor divider network makes the Virtex-E devices consume two times more power than APEX 20KE devices. Table 5 compares the DC power consumption of APEX 20KE devices and Virtex-E devices.

Table 5. DC Power Consumption Comparison

Number of Channels	APEX 20KE (mW)	Virtex-E (mW)
1	11.2	21.2
2	22.4	42.4
4	44.8	86.8
8	89.6	169.6
16	179.2	339.2

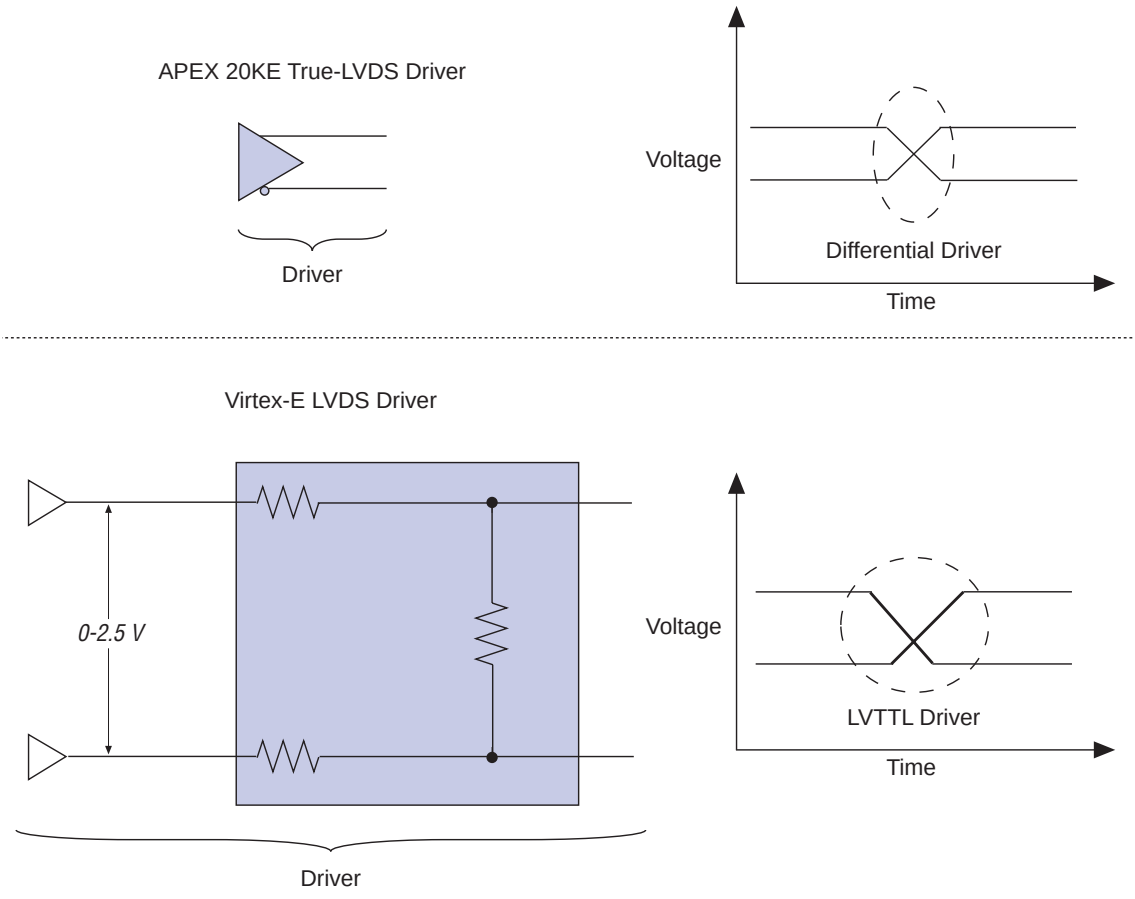
The increased power consumption in Virtex-E devices compromises the low-power advantages of the LVDS I/O standard. In addition, the high 2.5-V swing of the Virtex-E LVDS drivers produces more electromagnetic interference (EMI) than the low voltage swing of the APEX 20KE devices.

DC Balance

The I/O drivers in APEX 20KE devices are differential drivers. When using differential drivers, the DC balance determines the common mode noise and skew margins. Therefore, APEX 20KE I/O drivers have an excellent DC balance, which leads to a high common-mode rejection ratio (CMRR) increase and better noise immunity.

Instead of using differential drivers, Virtex-E devices use low-voltage transistor-transistor logic (LVTTL) drivers in combination with an on-board resistor network. LVTTL drivers do not have DC balance and can generate common mode noise when used differentially. The use of LVTTL drivers and the on-board resistor network reduces the LVDS interface's CMRR and introduces extraneous noise into the LVDS signal. Figure 10 shows the DC balance in LVDS drivers for APEX 20KE devices and Virtex-E devices.

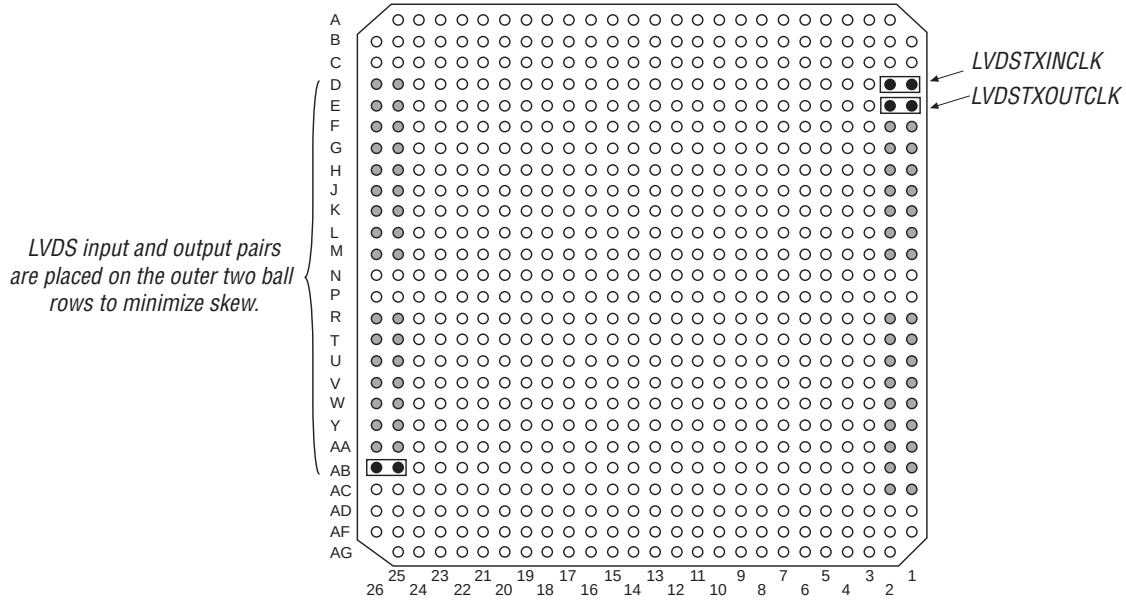
Figure 10. DC Balance in LVDS Drivers



Board Layout Issues

LVDS pins in APEX 20KE devices are placed along the outer edge of the device. The positive and negative pins of each channel are adjacent to each other. This close proximity minimizes board-level skew between the two pins and simplifies trace layout. Figure 11 shows a True-LVDS pin placement example in an APEX 20KE device.

Figure 11. Example of True-LVDS Pin Placement in an APEX 20KE Device



LVDS pins in Virtex-E devices are placed up to 6 mm from each other. To minimize skew, a user must compensate for this distance by adjusting the trace lengths for the positive channels and the negative channels on the board.

According to *XAPP233*, the 311-MHz clock must be delayed on board by 1.1 ns relative to the data by using additional trace lengths or a driver with a well characterized propagation delay. A user has to adjust the trace lengths to create an exact delay. Depending on the operating conditions—which includes voltage, temperature, noise on other signals, and other operating conditions—trace delays vary significantly. Therefore, if a user is able to achieve the required 1.1-ns delay under ideal conditions, the changing operating conditions do not guarantee that a design will work in the field.

Figure 12 shows that a Virtex-E LVDS transmitter needs a 1.1 ns on board delay on the clock line.

Figure 12. On-Board Delay Required by Virtex-E LVDS Transmitter

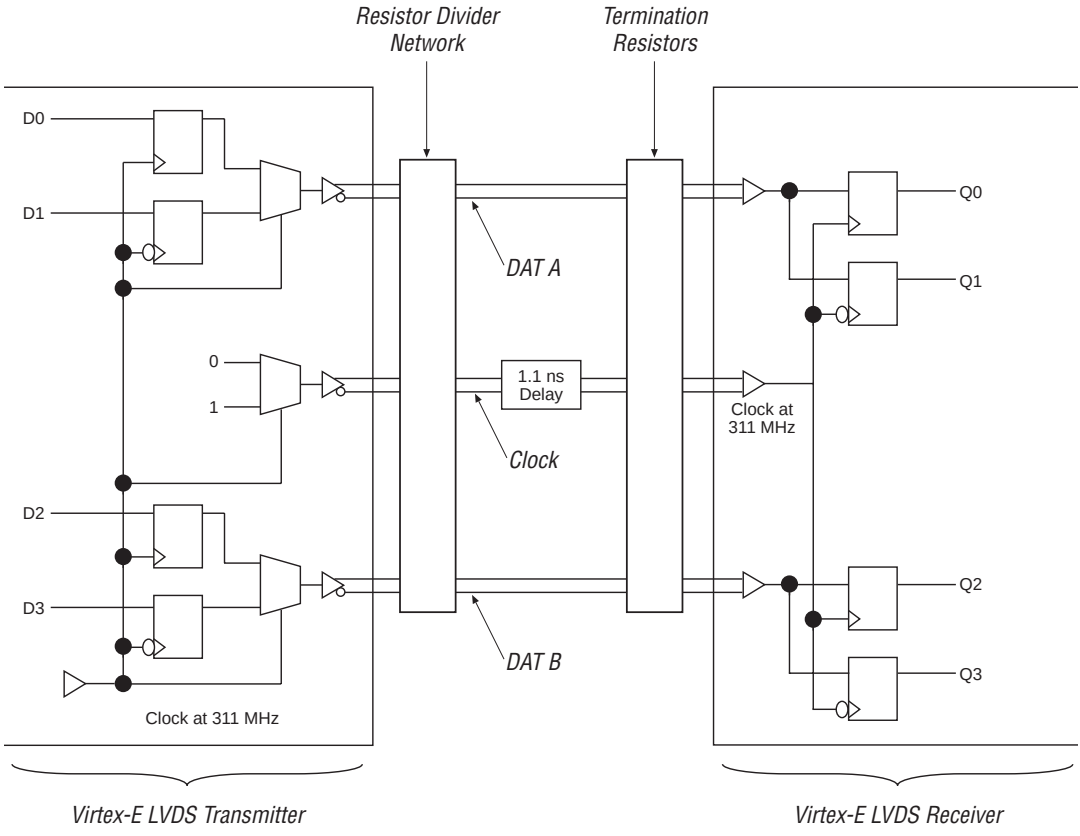
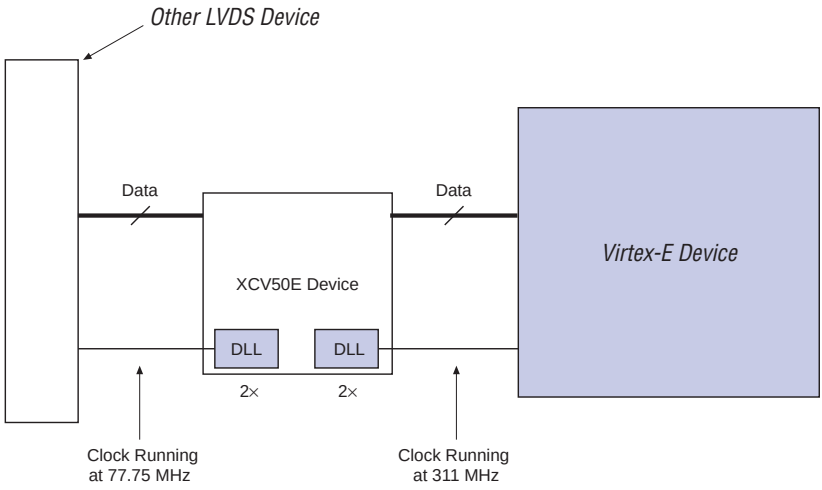


Figure 13 shows the proposed interface for Virtex-E LVDS in 8× data transfer mode.

Figure 13. Proposed Interface for Virtex-E LVDS



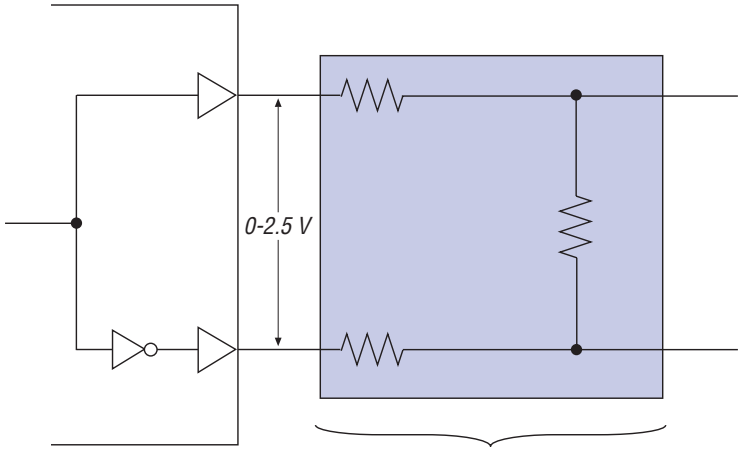
Board-Level Noise

Virtex-E devices have board-level noise problems. In the Virtex-E LVDS implementation, a derived clock running at 311 MHz is fed to an output pin. Switching an I/O pin at such a high frequency can lead to ground bounce issues and results in ground-bounce problems on adjacent pins. More importantly, the LVDS outputs do not have any dedicated power pins, which adds noise to the signals.

Board Space

As described in earlier sections, the Virtex-E I/O drivers are not LVDS drivers, but LVTTL drivers. By using costly on-board resistor divider networks, a user must convert the LVTTL drivers to LVDS drivers. These on-board resistors increases board space utilization, a problem that will escalate quickly with an increasing number of data channels. Figure 14 shows how on-board resistor packs compromise board space in Virtex-E devices.

Figure 14. On-Board Resistor Packs & Board Space in Virtex-E Devices



APEX 20KE device drivers do not need any external board-level components. This saves board space, simplifies board layout, and offers more flexibility and freedom for board design.

Conclusion

Virtex-E devices have no dedicated LVDS circuitry, no drop-in compilation support, stringent board layout requirements, higher power consumption, and require extensive design efforts.

The APEX 20KE True-LVDS solution offers an LVDS interface that is robust, flexible, and easy-to-use. APEX 20KE devices outperform Virtex-E devices on many levels: APEX 20KE devices have dedicated LVDS circuitry, built-in deskew circuitry, drop-in compilation support in the Quartus software, better on-chip LVDS pin placement, increased noise immunity, simple board-level design requirements, and improved power efficiency.

The APEX 20KE True-LVDS solution offers a clear advantage over the Virtex-E LVDS solution.

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