Convolutional Interleaver Megafunction

Solution Brief 16 **March 1997, ver. 1**

Target Applications:
Digital Signal Processing
Digital Communication Receiver
Wireless Communications

Family:
FLEX® 10K, FLEX 8000 & MAX® 9000

Vendor:

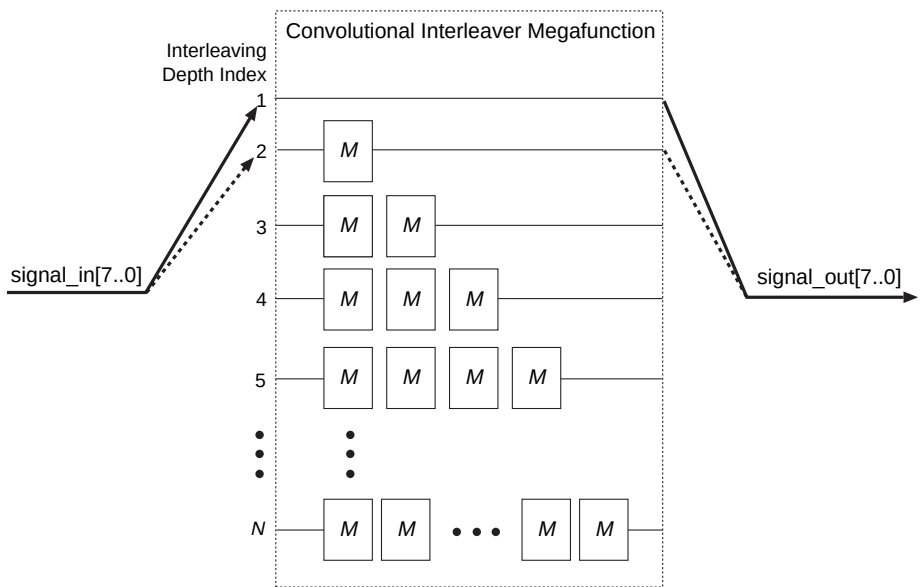
KTech Telecommunications, Inc.
15501 San Fernando Mission Blvd.
Suite 100
Mission Hills, CA 91345
Tel. (818) 361-2248
Fax (818) 270-2010
E-mail skuh@ktechtelecom.com
WWW www.ktechtelecom.com

- Implements a convolutional interleaver function
- Accepts a byte at the input with each clock cycle
- Produces a convolutional-interleaved byte at the output with each clock cycle
- Applications include digital receivers for personal communication systems (PCS) and cable modems

General Description

The convolutional interleaver megafunction implements a convolutional interleaving design that is optimized for PCS and cable modem applications. In FLEX 10K devices, the megafunction uses embedded array blocks (EABs) to support interleaving depth for most convolutional interleaving applications, such as PCS and cable modems. The FLEX 10K EABs support a maximum interleaving size ($N \times M$) of 3,072 bytes, where N is the final index of the interleaving depth and M is the bit memory stage first-in first-out (FIFO) shift register size. For larger interleaving depth, the megafunction requires an external dual-port RAM. A convolutional interleaver megafunction that uses external RAM can be efficiently optimized for FLEX 10K, FLEX 8000, or MAX 9000 device architectures. Figure 1 shows a functional block diagram of the convolutional interleaver megafunction.

Figure 1. Convolutional Interleaver Megafunction Functional Block Diagram



Functional Description

The convolutional interleaver megafunction accepts the input data signal 8 bits at a time. At each byte clock cycle, the `signal_in[7..0]` and `signal_out[7..0]` buses shift to the next row of delay elements. When the maximum depth N is reached, the `signal_in[7..0]` and `signal_out[7..0]` buses go back to the initial index 1 and continue with each cycle of the byte clock. After a delay is introduced by the interleaver, the `signal_out[7..0]` bus produces 8 bits at each byte clock.

Ports

Table 1 describes the ports for the convolutional interleaver megafunction.

Table 1. Convolutional Interleaver Megafunction Ports

Name	Type	Size (Bits)	Description
signal_in[7..0]	Input	8	Signal data input
byteclk	Input	–	Byte clock
reset	Input	–	Asynchronous global reset
signal_out[7..0]	Output	8	Signal data output

Parameters

The three EABs in the EPF10K10 device can hold a maximum of 768 bytes. Larger FLEX 10K devices or external memory can support larger interleaving dimensions (e.g., the EPF10K100 can support a maximum of 3,072 bytes). KTech Telecommunications can customize the megafunction's interleaving depth and bit memory stage FIFO shift register size to meet specific user requirements.

Performance & Implementation

The convolutional interleaver megafunction operates at the byte clock rate. The megafunction performance ranges from 52 MHz in FLEX 10K devices to 85 MHz in MAX 9000 devices. Table 2 shows the performance and density information for a typical convolutional interleaver megafunction in FLEX and MAX device architectures. A downstream path in a quadrature phase shift keying (QPSK) cable modem requires an interleaving size of $N \times M = 11 \times 10$. In this implementation, the megafunction's memory structure can easily fit into a single FLEX 10K EAB, or it can be expanded to use all of the device's EABs. The MAX 9000 implementation requires external memory.

Table 2. Performance & Implementation of the Convolutional Interleaver Megafunction

Device Family	Smallest Target Device	Speed Grade	Logic Cells	EABs	Performance (f_{MAX})	Maximum Interleaving Size of Target Device ($N \times M$)
FLEX 10K	EPF10K10	-4	252	3	52 MHz	768 bytes
FLEX 8000	EPF8452A	A-2	244	–	66 MHz	–
MAX 9000	EPM9320	-12	185	–	85 MHz	–

2610 Orchard Parkway
San Jose, CA 95134-2020
(408) 894-7000
http://www.altera.com