EC210 PCI Bus Master/Target Megafunction

Target Applications:

Bus Interface

Family: FLEX 10K

Vendor:

Eureka Technology

Features

- Fully compliant with peripheral component interconnect Special Interest Group's (PCI-SIG) *PCI Local Bus Specification*
- Implements full PCI bus master/target functionality
- Optimized for the Altera® FLEX® 10K device architecture
- Optimized for devices with a slow output enable control
- Supports all PCI-specific configuration registers
- Efficient back-end device interface for different types of PCI bus masters
- Provides target functions that allow control register programming
- Supports target-retry, disconnect, and target-abort signals
- Automatic transfer restart on target-retry and disconnect signals

General Description

The EC210 PCI bus master/target megafunction is a bus interface unit designed for efficiently interfacing between the PCI bus and a simple, X86-style back-end device. The megafunction operates as a bidirectional PCI bus translator, and it performs all data transfers necessary for the back-end device to access the PCI memory or I/O interface. Megafunction access is initiated by a PCI bus master (e.g., a video coprocessor or DMA controller) via the back-end device.

The megafunction performs all data transfers necessary for the bus master to access the PCI bus. To provide maximum memory bandwidth, the megafunction supports both single and burst data transfers, including zero-wait states, in both directions. All data transfers on the PCI bus are accessed through the back-end device.

Figure 1 shows a block diagram of the megafunction and its bidirectional operation.

Figure 1. Block Diagram of the EC210 PCI Bus Master/Target Megafunction
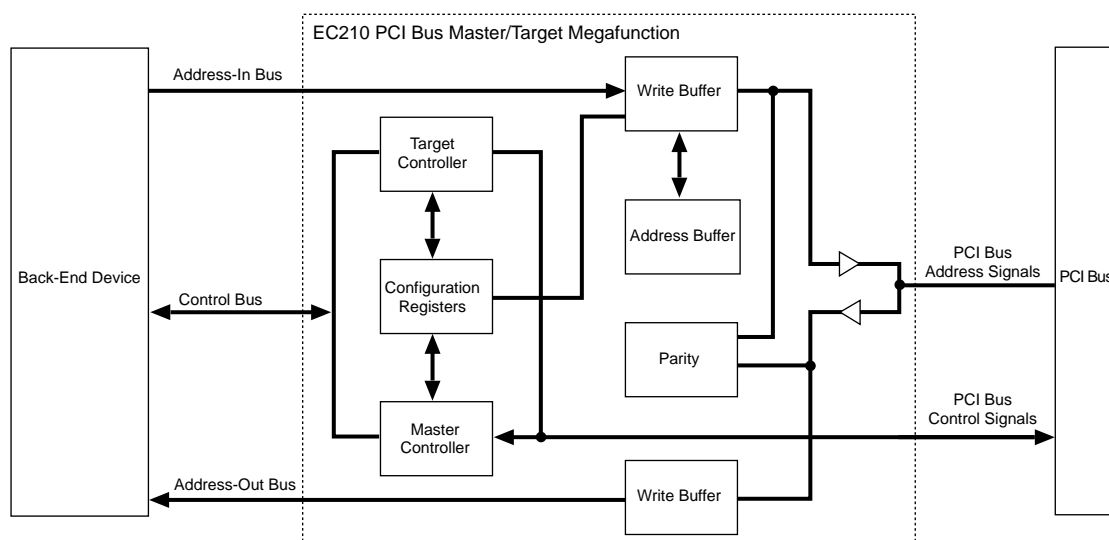
Functional Description

As a bidirectional translator, the EC210 PCI bus master/target megafunction allows another master (or the host) to read or write data in the opposite direction to the back-end device and perform procedures such as programming the DMA control registers. A bus master such as a DMA controller, residing on the back-end device, can easily initiate data transfers to the PCI bus. With the DMA controller on the back-end device, the megafunction can minimize transfer latency by supporting high-speed bus requests and arbitration.

Figure 2 shows the functional grouping of signals for the EC210 PCI bus master/target megafunction.

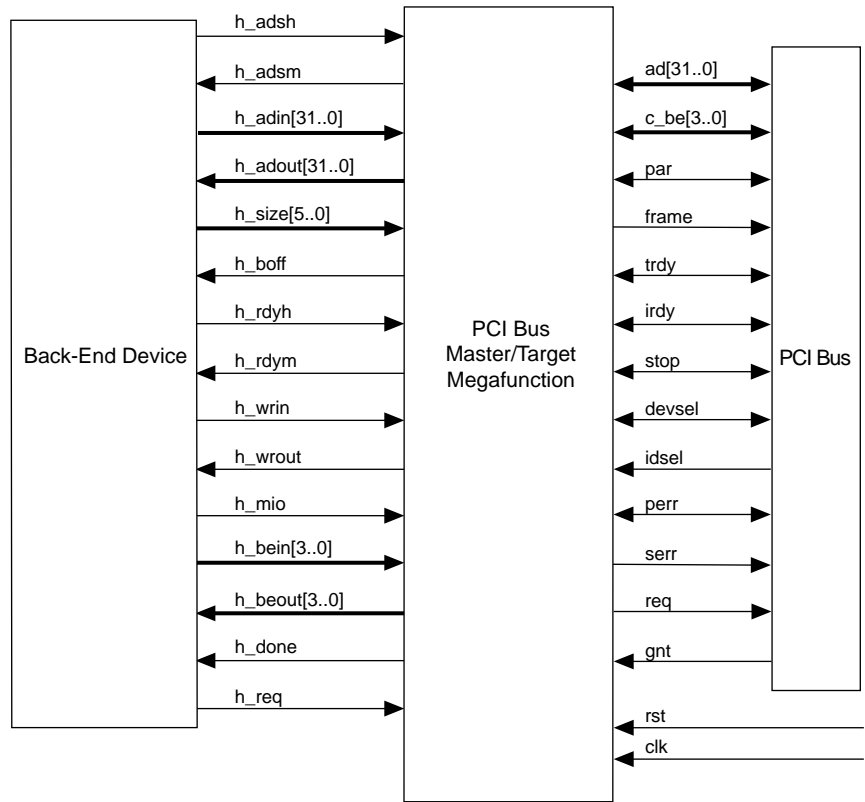*Figure 2. Signals for the EC210 PCI Bus Master/Target Megafunction*

Table 1 describes the signals that interface the EC210 PCI bus master/target megafunction to the PCI bus.

Table 1. Signals Interfacing the EC210 PCI Bus Master/Target Megafunction to the PCI Bus		
Name	**Type**	**Description**
gnt	Input	Grant signal. This signal indicates that the master has been granted access to the PCI bus.
idsel	Input	Initialization device input select. This signal is used as a chip select during configuration read and write transactions.
clk	Input	System clock.
rst	Input	System restart.
req	Output	PCI bus request signal. The master asserts this signal to request mastership of the PCI bus.
serr	Output	System error signal. This signal reports address parity errors and special cycle data parity errors, and it can be asserted by the master or the target only if allowed by the configuration command.
frame	Output	Cycle frame signal. The master drives this signal to indicate the start and duration of a transaction. When frame is asserted, data transfer is in progress; when frame is deasserted, the data transfer is in its final phase.
ad[31..0]	I/O	Address and data signals are multiplexed on the same PCI bus pin. A PCI bus transaction consists of an address phase followed by one or more data phases. The megafunction supports both read and write burst data transfers.
c_be[3..0]	I/O	Bus command and byte enable signals are multiplexed on the same PCI bus pin. During the address phase of a transaction, c_be[3..0] issues the bus command; during the data phase of a transaction, c_be[3..0] issues byte enables.
devsel	I/O	Device select signal. The target asserts this signal when the master decodes its address. As an input signal, devsel indicates whether any device on the PCI bus is selected.
irdy	I/O	Initiator ready signal. This signal indicates that the master can complete the current data transaction. The irdy signal is used with the trdy signal to indicate the completion of a data transfer.
par	I/O	Parity signal. This signal ensures even parity across the ad[31..0] and c_be[3..0] signals. This signal can be driven by either the master for address and write transactions, or by the target for all read transactions.
perr	I/O	Parity error signal. The master or target asserts this signal when a parity error is detected during address or data transaction.
stop	I/O	This signal is asserted by the target to stop a master transaction.
trdy	I/O	Target ready signal. This signal indicates that the target can complete the current data phase transaction. The trdy signal is used with the irdy signal to indicate the completion of a data transfer.

Table 2 describes the signals that interface the EC210 PCI bus master/target megafunction to the back-end device.

Table 2. Signals Interfacing the EC210 PCI Bus Master/Target to the Back-End Device Signals (Part 1 of 2)		
Name	**Type**	**Description**
h_adin[31..0]	Input	Address/data multiplexed PCI bus signal. This signal is driven by the target to the master. The signal indicates address/data transfers during a PCI bus write transaction, and data transfers during a control register read transaction.
h_adsh	Input	Address strobe signal. The target asserts this signal to request a read/write transfer on the PCI bus.
h_bein[3..0]	Input	Byte enable bus signal. This signal indicates the active bytes for PCI bus read/write cycles.
h_mio	Input	Memory and I/O select signal. This signal selects between the memory (high) and I/O (low) address space.
h_rdyh	Input	For a write transaction, this signal indicates that the target control registers have accepted data on the PCI bus. For a read transaction, the signal indicates that the target control registers have processed the data transfer.
h_req	Input	Host request signal. The target can assert this signal one cycle before the h_asdh signal is asserted to indicate that a transfer will start with the next clock cycle. This assertion will cause the PCI interface to assert its request signal to minimize PCI bus delay. The PCI interface can also assert its request signal.

Table 2. Signals from the EC210 PCI Bus Master/Target Megafunction to the Back-End Device Signals (Part 2 of 2)		
Name	**Type**	**Description**
`h_size[5..0]`	Input	This signal indicates the length of the burst transfer. If the signal has a value of 000001, it indicates a single transfer. If the signal has a value of all 0s, then `h_size` has a transfer length of 64 bits. If it has other values, then `h_size` is the length of the transfer. The designer must ensure that the transfer length does not cross the target address boundary.
`h_wrin`	Input	The back-end device generates this signal to indicate a read (low) or write (high) transaction to the PCI bus master.
`h_adsm`	Output	The master asserts this signal to request access to a control register for a read/write transaction.
`h_adout[31..0]`	Output	Address/data multiplexed PCI bus signal. This signal is driven by the master to the target. The signal indicates address/data transfers during a control register write transaction, and data transfers during a PCI bus read transaction.
`h_beout[3..0]`	Output	Byte enable bus signal. This signal indicates access to the control register.
`h_boff`	Output	Back off signal. If this signal is simultaneously asserted with the `h_done` signal, an abnormal termination has occurred on the PCI bus and the current transfer is aborted. If the `h_boff` signal is asserted without the `h_done` signal, it indicates that an incoming PCI bus request is pending or the master is busy. The target must abort its transfer request if a PCI bus request is pending.
`h_done`	Output	Done output. This signal is asserted when a PCI bus transaction is complete. During a write operation, the `h_rdym` signal is asserted as soon as the last data is written to the write buffer, and `h_done` is asserted when the PCI bus data transfer is complete.
`h_rdym`	Output	For a write transaction, this signal indicates that the megafunction has accepted data on the PCI bus. For a read transaction, the signal indicates that the megafunction has processed the data transfer.
`h_wrout`	Output	This signal is valid for the control register access cycle. The PCI bus master generates this signal to indicate if the control register access is a read (low) or write (high) transaction.

Optional Features

Several PCI bus master options are available from Eureka Technology: a direct first-in first-out (FIFO) interface, memory or I/O mapping, a 64-bit bus extension, and host bridge capability. Contact Eureka Technology for information on these options.

Utilization

Table 3 shows the typical device utilization of the EC210 PCI bus master/target megafunction.

Table 3. Typical Device Utilization			
Implementation	**Clock (f_{MAX})**	**Logic Cells**	**Embedded Array Blocks (EABs)**
Master/target	33 MHz	650	0

Reference

PCI Special Interest Group. *PCI Local Bus Specification*. Rev. 2.1. Hillsboro, Oregon: PCI Special Interest Group, 1995.

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