# a8259 Programmable Interrupt Controller MegaCore Function

Solution Brief 21 August 1997, ver. 1

Target Application:
Computers

Family:
FLEX 10K, FLEX 8000, FLEX 6000, MAX 9000 & MAX 7000

Vendor:

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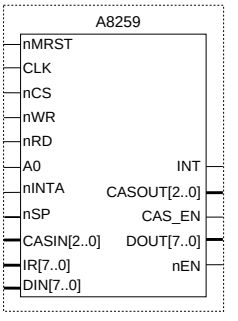
## Features

- Optimized for the Altera® FLEX® and MAX® device architectures
- Risk-free evaluation with the OpenCore™ feature available with MAX+PLUS® II
- Functionally based on the Intel 8259 device

## General Description

The Altera a8259 MegaCore™ function implements a programmable interrupt controller. The a8259 can be initialized by a microprocessor through eight data bus lines (din[7..0] and dout[7..0]), and the ncs, nrd, nwr, int, and ninta control signals. Figure 1 shows the symbol for the a8259.

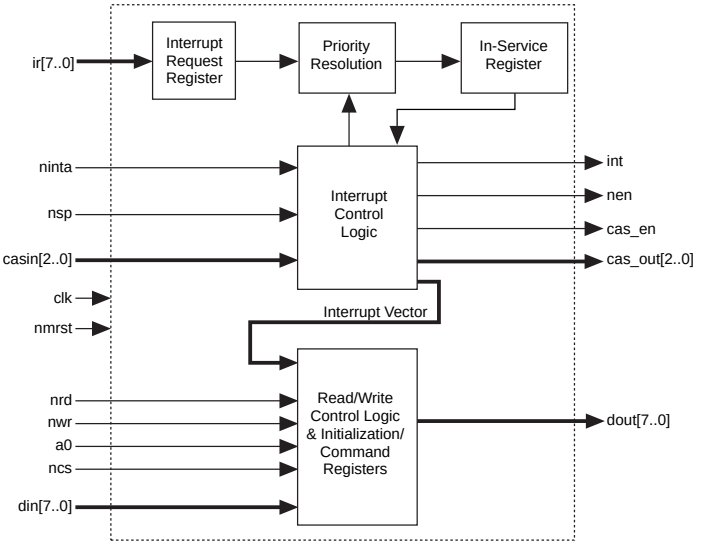
*Figure 1. a8259 Symbol*




## Functional Description

Figure 2 shows the a8259 block diagram.

*Figure 2. a8259 Block Diagram*






MegaCore™

The int and ninta signals provide the handshaking mechanism for the a8259 to signal the microprocessor. The a8259 requests service via the int signal and receives an acknowledgment of acceptance from the microprocessor via the ninta signal. The int signal is applied directly to the microprocessor's interrupt input. When the a8259 receives a valid interrupt request on an ir[7..0] pin, the int signal goes high.

The ninta input is connected to the microprocessor's interrupt acknowledgment signal. The microprocessor pulses the ninta signal twice during the interrupt acknowledgment cycle, which tells the a8259 that the interrupt request has been received. Then, the a8259 sends the highest priority active interrupt type number onto the din[7..0] bus for the microprocessor to acknowledge.

The ir inputs are used by external devices to request service, and they can be configured for level-sensitive or edge-sensitive operation.

The casin[2..0]and casout[2..0] buses, and nsp and cas_en pins are used to implement the cascade interface. These pins are used when more than one a8259 functions are interconnected in a master / slave configuration, expanding the number of interrupts from 8 up to 64.

The a8259 supports several operational commands: priority rotation, end of interrupt (EOI), special mask mode (SMM), trigger modes, and poll command. The a8259 can operate in four different modes: fully nested mode, cascade mode, special fully nested mode, and buffered mode.

For more information, refer to the *a8259 Programmable Interrupt Controller Data Sheet* in the *Microperipheral MegaCore Function Data Book, version 2.*

## Utilization

Table 1 describes the logic cell requirements for MAX and FLEX architectures.

*Table 1. a8259 Logic Cell Requirements*

| Function | MAX | FLEX |
|---|---|---|
| a8259 programmable interrupt controller | 335 | 399 |

## Variations & Clarifications

The following characteristics distinguish the Altera a8259 function from the Intel 8259A device:

- A master clear is provided with the a8259 function.
- A clock signal has been added, and synchronous design rules have been incorporated to improve operation and reliability. All input signals except nmrst and ir[7..0] should be synchronous to the clock signal. All inputs must be asserted for one clock cycle to ensure reliable operation.
- Bidirectional I/O pins are split into separate inputs, outputs, and corresponding tri-state control lines. This features makes the a8259 compatible with the bus or multiplexer scheme used internally in a design.
- The dout[7..0], casout[2..0], int, cas_en, and nen outputs are driven by complex logic structures and are prone to glitches. These signals should be registered in most applications.
- Automatic EOI in slave mode is implemented within the a8259.

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