PCI Bus Master / Target Interface Megafunction

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Target Application:
Buses & Interfaces

Family:
FLEX 10K

Vendor:

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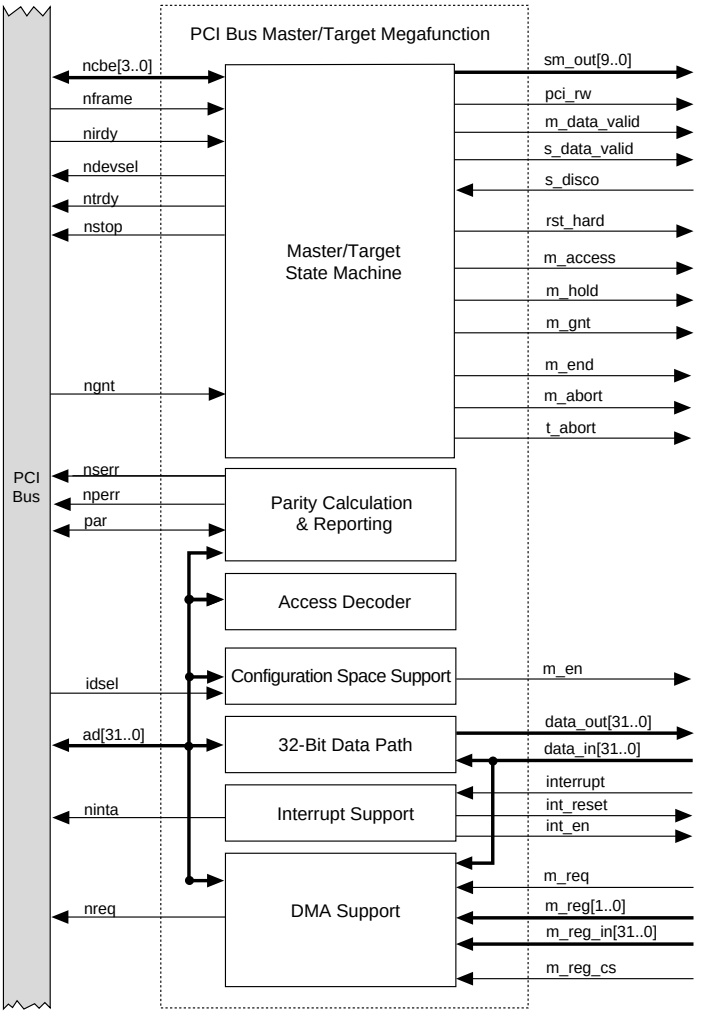
Features

- Optimized for the Altera® FLEX® 10K device architecture
- Fully compliant with peripheral component interconnect Special Interest Group (PCI-SIG) *PCI Local Bus Specification*, Rev. 2.1
- Fully synchronous design
- Fully hardware tested
- Supports full-speed burst support up to 132 Mbytes / second
- Supports a zero-wait state data transfer rate

General Description

The PCI bus master / target interface megafunction is a 32-bit PCI bus interface that is used for high-speed data transfers and real-time computing applications such as fast data-intensive projects and the migration of ISA-based designs to PCI bus designs. Figure 1 shows a block diagram of the megafunction.

Figure 1. Block Diagram of the PCI Bus Master / Target Interface Megafunction



Functional Description

The PCI bus master / target interface megafunction provides a simple and flexible interface between a PCI bus and a user-developed design. The megafunction comes with a set of Altera Hardware Description Language (AHDL™) reference designs that designers can customize for their own projects. These reference designs include an interface that uses FLEX 10K embedded array blocks (EABs) as a synchronous SRAM buffer and another interface that is based on an external SRAM buffer.

In addition, the megafunction has a built-in direct-memory access (DMA) controller that interfaces with either internal EAB memory or external memory. DMA operations can be programmed through software or by the user's application logic. The megafunction can also support alternative back-end interfaces, such as an external first-in first-out (FIFO) buffer.

Performance

The megafunction operates at 33 MHz. Table 1 provides the typical utilization results for the megafunction.

Table 1. Typical Utilization Results for the PCI Bus Master / Target Interface Megafunction

Implementation	Target Device	Clock (f_{MAX})	EABs	Logic Cells	% of Logic Cells Used
32-bit PCI bus master/target	EPF10K20-3	33 MHz	0 / 6	810 / 1,152	70%
	EPF10K30-3	33 MHz	0 / 6	810 / 1,728	45%
	EPF10K40-3	33 MHz	0 / 8	810 / 2,304	35%
32-bit PCI bus master/target with internal SRAM	EPF10K20-3	33 MHz	4 / 6	980 / 1,152	85%
	EPF10K30-3	33 MHz	4 / 6	980 / 1,728	55%
	EPF10K40-3	33 MHz	4 / 8	980 / 2,304	40%

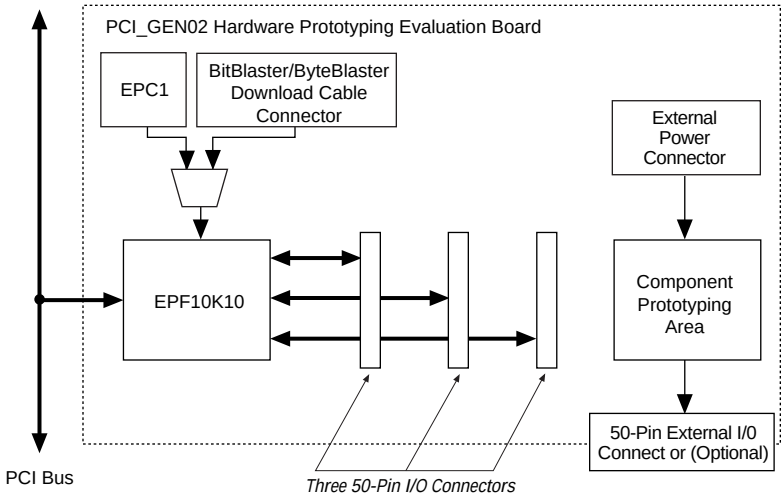
Customization

The PCI bus master / target interface megafunction is fully parameterizable, allowing the designer to customize the memory space location and size (between 16 bytes and 64 Mbytes); the device, vendor, class code, and revision ID registers; and the `MAX_LAT` and `MIN_GNT` master registers.

Hardware Testing

The PCI bus master / target interface megafunction has been developed and tested using the PCI_GEN02 PCI bus evaluation board (available from PLD Applications). The PCI_GEN02 contains either an EPF10K20 or EPF10K30 device that implements the megafunction. Because the megafunction uses 55% of an EPF10K30, the remaining logic and EABs in the device are available for user-defined custom logic. Figure 2 shows a block diagram of the PCI_GEN02 PCI bus evaluation board.

Figure 2. Block Diagram of the PCI_GEN02 PCI Bus Evaluation Board



The FLEX 10K device can be configured using an EPC1™ Configuration EPROM, a BitBlaster™ download cable, or a ByteBlaster™ download cable. These options allow the designer to choose between a variety of configuration techniques. Three 50-pin headers are provided for a daughter card, and the 50-pin off-card connector is supported by the PCI_GEN02 solder mask.

Reference

PCI Special Interest Group. *PCI Local Bus Specification*. Rev.2.1 Hillsboro, Oregon: PCI Special Interest Group, 1995.

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