USB Host Controller Megafunction

Solution Brief 28 **June 1997, ver. 1**

Target Applications:
Buses & Interfaces

Family: FLEX® 10K & FLEX 8000

Vendor:

Sapien Design, Inc.
45335 Potawatami Dr.
Fremont, CA 94539
Tel. (510) 668-0200
Fax (510) 668-0200
E-mail sapien@pacbell.net
WWW http://www.sapiendesign.com

Features

- Fully compliant with universal serial bus (USB) 1.0 Specification
- Automatic hardware-managed protocol
- Supports suspend, resume, and reset signaling
- Status and error reporting
- Applications
  - Embedded system USB host
  - USB host hardware prototyping

General Description

The USB host controller megafunction implements the complete USB 1.0 Specification for host controllers and is suitable for embedded system applications that drive USB devices. The megafunction automatically manages all USB protocol requirements in hardware. It offers a fast, low-risk method to implement a USB connection that can be integrated into any application. The megafunction is available in netlist, Verilog HDL, or VHDL RTL format.

Functional Description

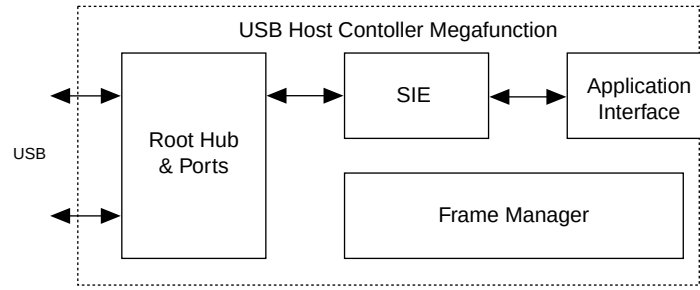
The megafunction is comprised of several logic blocks, as shown in Figure 1. The root hub is the interface to the USB, and it supports two ports, which can be used for LS and FS signaling.

The Serial Interface Engine (SIE) performs receiver and transmitter functions, including packet formation and serialization. The SIE also supports low-level USB protocol operations, such as bit-stuff, NRZI, packet identifier (PID), and cyclic redundancy check (CRC). The SIE decodes incoming packets, checks the CRC, and detects bit errors, which are all reported to the frame manager. The SIE formats outgoing packets, adding the appropriate header CRC and other protocol requirements.

The frame manager generates start of frame (SOF) packets, schedules periodic and non-periodic packets into frames, and manages data and handshake packets.

The system processor queues packets, which contain headers with direction, size, and destination information, into memory. Packet locations are written to channel registers, and subsequent packets are chained together. Packets that time out or return a `nack` signal are automatically retried. Packet sizes are used as a criteria for inclusion into a frame.

Figure 1. USB Host Controller Megafunction Block Diagram



The FLEX 10K implementation uses the embedded array blocks (EABs) for storage buffers, and in some applications, as FIFOs.

The megafunction is verified to operate at either full- or low-speed transfer rates. A 4X over-sample phase-locked loop (PLL) in the receiver block synchronizes the data to the megafunction clock. The application side can be operated synchronously or asynchronously to the USB clock.

Performance

Table 1 lists the typical device utilization for the USB host controller megafunction in EPF10K30 and EPF81500 devices.

Table 1. Typical Device Utilization

Family	Smallest Device	Speed	Logic Cells	EABs	Performance	Availability
FLEX 10K	EPF10K30	-4	1,250	3 to 6	12 MHz	Now
FLEX 8000	EPF81500	A-4	1,250	–	12 MHz	Call Vendor

The USB host controller megafunction can be delivered as a netlist or in source code format. Sapien Design supplies user guide and synthesis scripts and offers telephone, e-mail, and on-site technical support.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com