IDR Deframer Megafunction

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Target Applications:
Digital Signal Processing (DSP)
Digital Video Broadcast (DVB)
Satellite Communications

Family:
FLEX® 10K

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Features

- Frame and multi-frame synchronization signals
- Four backward alarm signals
- Single voice channel of 8 Kbits/second
- Two voice channels of 32 Kbits/second
- Compatible with the INTELSAT Earth Station Standard (IESS)-308 specification

General Description

The ISS IDR deframer megafunction is an IESS-308-compatible deframer, capable of extracting overhead data from a composite data stream. It supports the full range of overhead signals, including:

- Frame and multi-frame synchronization
- Four backward alarm signals
- Single data channel of 8 Kbits/second
- Two voice channels of 32 Kbits/second each

The IESS-308 specification details several IDR carrier frequencies; the IDR deframer megafunction supports the carrier frequencies shown below:

- 2.048 Mbits/second
- 8.448 Mbits/second
- 16.896 Mbits/second, *Note (1)*
- 34.368 Mbits/second

Note:
(1) Although the 16.896 Mbits/second carrier frequency is not defined by the IESS-308 specification, it is similar to the 34.368 Mbits/second carrier frequency except each sub-frame carries only 176 data bits.

Figure 1 shows the symbol for the IDR deframer megafunction.

Figure 1. IDR Deframer Symbol

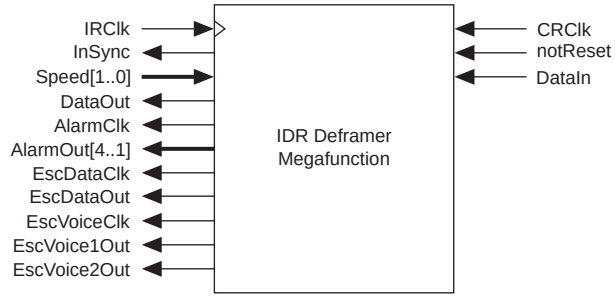
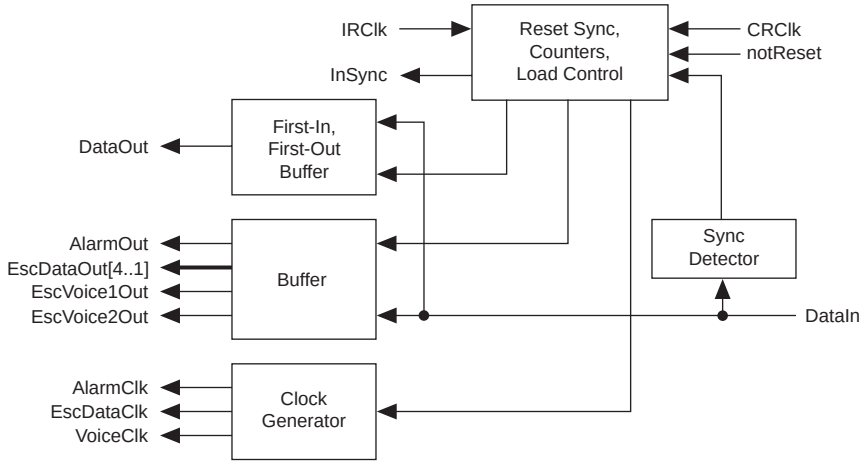


Figure 2 shows the block diagram for the IDR deframer megafunction.

Figure 2. IDR Deframer Megafunction Block Diagram



Functional Description

The IDR deframer megafunction performs engineering service circuit (ESC) channel data, voice, and alarm extraction, together with frame synchronization signal detection. The recovered data streams are buffered and then clocked out at different rates. The megafunction generates clock signals for the slower data rate signals and supports four clock rate combinations. Designers must supply both the input data rate and composite data rate clocks at the exact frequency ratios defined by the IESS-308 specification.

Sync Detection

The incoming data stream is sampled a bit at a time over a succession of frames. If a synchronized pattern is not detected at that bit position within 16 frames, a bit is skipped and synchronization detection moves on to the next bit position. Once a valid synchronization is detected, frame data extraction begins on the next superframe. The `InSync` signal will be asserted when the initial data appears on the `DataOut` pin. In the absence of transmission bit errors, synchronization will be achieved within a time specified by the following formula.

Synchronization Time = `CrClk` period × 16 × (Total Bits Per Frame)^2

First-In, First-Out (FIFO) Buffer

Input data is loaded into an asynchronous FIFO buffer for data rate conversion. Data is not loaded when frame overhead bits are being received. Data bits are extracted from the FIFO buffer at the intermediate rate, and output to the `DataOut` pin.

ESC Data Clocks & Buffers

The composite rate clock, `CRClk`, derives the clock signals for the ESC voice channels, ESC data channel, and ESC alarm signals. These signals have defined frequencies. Data for the relevant channel is loaded into small buffers on receipt from the composite stream. Data is removed from the buffers a maximum of two frames later, on the rising edge of the relevant clock signal, and driven onto the appropriate output pin.

Counters & Buffer Load Control

A number of counters keep track of the frame, subframe, and bit number, and control the input stream disassembly. IESS-308 does not specify a relationship between the content of the data streams and the framing signals. The equipment connected to the data streams must be synchronized to the data carried in those streams.

Ports

Table 1 describes the ports for the IDR deframer megafunction.

Table 1. IDR Deframer Megafunction Ports (Part 1 of 2)

Name	Type	Description
CRClk	Input	Composite rate clock. This signal drives the bulk of the megafunction activity. The supplied signal must have the exact frequency required by the IESS-308 specification in the frame clock section. Output clocks are derived from this input. The required frequency is 8.554 MHz or 34.464 MHz.
notReset	Input	Core reset (active low). Initializes the megafunction to a known state. This signal is clocked by IRClk and requires a 5-ns setup before the clock edge on deassertion to ensure that all signals reset simultaneously.
Speed[1..0]	Input	IDR speed select. This signal is used to inform the megafunction of the IDR clock's speed. This signal should only be changed when the core reset signal is asserted; otherwise, unpredictable results may occur. Table 2 shows the Speed[1..0] values for each IDR clock speed.
DataIn	Input	Composite data stream input. This signal is latched on the rising edge of CRClk and requires 15 ns of setup time.
IRClk	Input	Intermediate rate clock. This signal is an input at the IDR frequency (i.e., 8.448 MHz or 34.368 MHz).
InSync	Output	Synchronization achieved. This signal is asserted when the megafunction has detected and locked onto a multiframe synchronization signal in the input composite stream. This signal is clocked out by IRClk and will be valid within 10 ns of the rising edge of the IRClk input.
DataOut	Output	Main data stream output. This signal is clocked out by IRClk and will be valid within 10 ns of the rising edge of the IRClk input. Main stream data is extracted from the composite stream in accordance with the IESS-308 specification and presented on this output.
AlarmClk	Output	Main data stream output. This signal has only 50% duty cycle at the alarm clock frequency (1 kHz).
AlarmOut[4..1]	Output	Backward alarm signals. These outputs are updated on the falling edge of the AlarmClk output and are stable around the rising edge of that clock. These signals are extracted from the composite data stream, A1 to A4 bits, as shown in the IESS-308 specification.
EscDataClk	Output	ESC data clock. This signal has 50% duty cycle at the ESC data channel clock frequency (8 kHz).
EscDataOut	Output	ESC data input. This signal is updated on the falling edge of the EscDataClk output, and is stable around the rising edge of that clock. The signal is extracted from the composite data stream, d1 to d8 bits, as shown in the IESS-308 specification.

Table 1. IDR Deframer Megafunction Ports (Part 2 of 2)

Name	Type	Description
EscVoiceClk	Output	ESC voice clock. This signal has approximately 50% duty cycle at the ESC voice channel clock frequency (32 kHz). It is used for both voice channels.
EscVoice1Out	Output	ESC voice channel 1 input. This signal is updated on the falling edge of the EscVoiceClk output, and is stable around the rising edge of that clock. The signal is extracted from the composite data stream, P1 bits, as shown in the IESS-308 specification.
EscVoice2Out	Output	ESC voice channel 2 input. This signal is updated on the falling edge of the EscVoiceClk signal, and is stable around the rising edge of that clock. The signal is extracted from the composite data stream, P2 bits, as shown in the IESS-308 specification.

Table 2 shows the Speed[1..0] values for each IDR clock speed.

Table 2. Speed[1..0] Values

IDR Clock Speed (Mbits/Second)	Speed[1]	Speed[0]
2.048	0	0
8.448	0	1
16.896	1	0
34.368	1	1

Utilization

Table 3 describes the logic cell requirements for the IDR deframer megafunction.

Table 3. IDR Deframer Megafunction Logic Cell Requirements

Device	Speed Grade	Utilization		f_{MAX} (MHz)	Availability
		Logic Cells	EABs *(1)*		
EPF10K30A	-1	265	0	83	Now

Note:
(1) EABs = embedded array blocks.

Deliverables

The ISS IDR deframer megafunction includes the following items:

- Encrypted Altera-specific netlist file, **deframer.tdf**
- Megafunction compilation constraints file, **deframer.acf**
- Symbol file, **deframer.sym**, for use in MAX+PLUS® II schematics
- Simulation model for the megafunction, **deframer.snf**
- Text-only readme file (**readme.txt**) explaining the function of all four files

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