# I²C Slave Interface Megafunction

**Solution Brief 40** **June 1999, ver. 1**

**Target Applications:**
Bus & Interfaces
Processor & Peripherals

**Family:**
FLEX® 10K, FLEX 6000 & MAX® 9000

**Vendor:**

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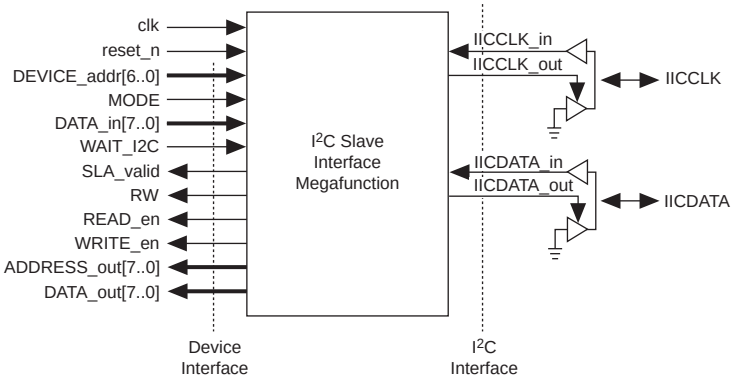
## Features

- Supports system clocks up to 50 MHz
- Supports inter integrated circuit (I²C) standard (100 kHz) and fast mode (400 kHz)
- Reads and writes data bursts
- Supports special mode for I²C read and write access to a dedicated register address
- Filters spikes from the I²C bus
- Generates wait states
- Fully synchronous design

## General Description

The I²C slave interface megafunction interfaces a device with an I²C bus. This megafunction is essentially a parallel-to-serial/serial-to-parallel converter, converting a device's parallel data into serial format for transfer over the I²C bus, and vice versa. Thus, a host CPU controls a device through the I²C master interface megafunction, the I²C bus, and the I²C slave interface megafunction. Figure 1 shows the symbol for the I²C slave interface megafunction.

***Figure 1. I²C Slave Interface Megafunction Symbol***




## Functional Description

The I²C slave interface megafunction is a synchronous slave that can receive or transmit data. The megafunction also allows the device to hold `IICCLK` low to force the master into a wait state.

For noisy environments, you can apply a spike filter to the incoming I²C data and clock signals. The spike filter evaluates the signals for a programmed number of clock cycles (up to a maximum of eight clock cycles). During this time, the spike filter removes any spikes in the signals.

The I²C slave interface megafunction supports four operating modes. See Table 1.

*Table 1. I²C Slave Interface Operating Modes*

| Mode | Description |
|---|---|
| Direct write | Writes a burst of data. |
| Direct read | Reads a burst of data. |
| Random access write | Writes one data byte to a specified address. |
| Random access read | Reads one data byte from a specified address. |

Tables 2, 3, and 4 describe the megafunction's global signals, interface signals to the device, and interface signals to the I²C bus, respectively.

*Table 2. I²C Slave Interface Megafunction Global Signals*

| Name | Type | Description |
|---|---|---|
| clk | Input | Device clock signals. |
| reset_n | Input | Low active asynchronous reset signal. |

*Table 3. Interface Signals to the Device*

| Name | Type | Description |
|---|---|---|
| DEVICE_addr[6..0] | Input | 7-bit device address. |
| MODE | Input | Mode select. A 0 indicates a random access read or random access write mode. A 1 indicates a direct read or direct write mode. |
| DATA_in[7..0] | Input | 8-bit data bus from the device to the megafunction. |
| WAIT_I2c | Input | High active wait state signal. |
| SLA_valid | Output | Slave address valid. |
| RW | Output | Read/write select. A 0 indicates a write, and a 1 indicates a read. |
| READ_en | Output | Read enable. |
| WRITE_en | Output | Write enable. |
| ADDRESS_out[7..0] | Output | 8-bit address bus to the device (random access read or random access write modes only). |
| DATA_out[7..0] | Output | 8-bit data bus to the device. |

*Table 4. Interface Signals to the I²C Bus*

| Name | Type | Description |
|---|---|---|
| IICCLK_in | Input | Clock input to the megafunction. |
| IICDATA_in | Input | Data input to the megafunction. |
| IICCLK_out | Output | Clock output for the megafunction. |
| IICDATA_out | Output | Data output for the megafunction. |

## Performance

Table 5 describes the megafunction's logic cell requirements for FLEX 10K, FLEX 6000, and MAX 9000 devices.

*Table 5. I²C Slave Interface Megafunction Logic Cell Requirements*

| Device | Speed Grade | Utilization | | Performance (MHz) |
|---|---|---|---|---|
| | | Logic Cells | EABs *(1)* | |
| EPF10K10 | -3 | 166 | 0 | 31 |
| | -4 | 166 | 0 | 26 |
| EPF10K10A | -1 | 166 | 0 | 47 |
| | -2 | 166 | 0 | 39 |
| | -3 | 166 | 0 | 29 |
| EPF10K30E | -1 | 166 | 0 | 66 |
| EPF6010A | -1 | 202 | – | 28 |
| EPF6016 | -2 | 202 | – | 24 |
| | -3 | 202 | – | 20 |
| EPM9320 | -15 | 131 | – | 45 |
| | -20 | 131 | – | 32 |
| EPM9560 | -10 | 131 | – | 52 |

*Note:*
(1) EABs = embedded array blocks.

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