64-Bit PCI Master/Target MegaCore Function

Solution Brief 44 **June 1999, ver. 1**

Target Applications:
All PCI-based systems

Family:
APEX™ 20K, FLEX® 10K

Ordering Code:
PLSM-PCI/C

Vendor:

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Features

- A flexible, general-purpose 64-bit peripheral component interconnect (PCI) interface that can be customized for specific peripheral requirements
- 66-MHz compliant in APEX 20K and FLEX 10KE devices
- Fully compliant with the PCI Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2*** timing and functional requirements
- Dramatically shortens design cycles
- Verified using industry-proven Phoenix Technologies test bench
- Hardware tested using the following hardware and software (see the "Compliance Summary" in the ***pci_c MegaCore Function User Guide*** for details)
  - HP E2928A PCI Bus Analyzer and Exerciser
  - HP E2920 Computer Verification Tools, PCI series
  - Altera's FLEX 10KE PCI development board
- Optimized for the APEX 20K and FLEX 10K architectures
- No-risk OpenCore™ feature allows designers to instantiate and simulate designs in the Quartus™ and MAX+PLUS® II software prior to purchase
- PCI master features:
  - Infinite zero-wait state cycles of PCI read/write operation (up to 528 Mbytes per second)
  - Initiates 64-bit addressing, using dual-address cycles (DACs)
  - Initiates 64-bit and 32-bit transactions
  - Dynamically negotiates 64-bit transactions and automatically multiplexes data on the local 64-bit data bus
  - Functions in host bridge applications
- PCI target features:
  - Zero-wait state PCI read/write (up to 528 Mbytes per second)
  - Capabilities list pointer support
  - Up to six base address registers (BARs) with adjustable memory size and type
  - Expansion ROM BAR support
  - Abnormal target terminations
  - Supports 64-bit addressing
  - Automatically responds to 32- or 64-bit transactions
  - Local-side interrupt request
- Configuration registers:
  - Parameterized registers: device ID, vendor ID, class code, revision ID, BAR0 through BAR5, subsystem ID, subsystem vendor ID, maximum latency, minimum grant, capabilities list pointer, expansion ROM BAR
  - Non-parameterized registers: command, status, header type, latency timer, cache line size, interrupt pin, interrupt line

General Description

The `pci_c` MegaCore™ function (ordering code: PLSM-PCI/C) is a hardware-tested, high-performance, flexible implementation of the 64-bit PCI master/target interface. This function handles the complex PCI protocol and stringent timing requirements internally, allowing designers to focus their engineering efforts on value-added custom development, significantly reducing time-to-market.

To guarantee robustness and strict compliance, hardware is tested using the HP E2928A PCI Bus Exerciser and Analyzer. The HP E2928A PCI Bus Exerciser and Analyzer simulates random behavior on the PCI bus by randomizing transactions with variable parameters.

Optimized for Altera® APEX 20K and FLEX 10KE devices, the pci_c function supports configuration, I/O, and memory transactions. With the high density of APEX and FLEX devices, designers have ample resources for custom local logic after implementing the PCI interface. The pci_c function can run at either 33-MHz or 66-MHz PCI bus clock speeds, thus achieving 264 Mbytes per second throughput in a 64-bit, 33-MHz PCI bus system, or 528 Mbytes per second throughput in a 64-bit, 66-MHz PCI bus system.

As a parameterized function, pci_c has configuration registers that can be modified upon instantiation. These features provide scalability, adaptability, and efficient silicon implementation. As a result, the same MegaCore function can be used in multiple PCI projects with different requirements. For example, the pci_c function offers up to six base address registers (BARs) for multiple local-side devices. However, some applications require only one contiguous memory range. PCI designers can choose to instantiate only one BAR, which reduces logic cell consumption. After designers define the parameter values, the Quartus and MAX+PLUS II software automatically and efficiently modifies the design and implements the logic. For high-end systems that require more than 2 Gbytes of memory space, the pci_c function also supports a 64-bit BAR. Additionally, the pci_c function can initiate 64-bit addressing using DACs.

This solution brief should be used in conjunction with the latest PCI user guide. Users should be fairly familiar with the PCI standard before using this function. Figure 1 shows the pci_c functional block diagram.

Figure 1. pci_c Functional Block Diagram

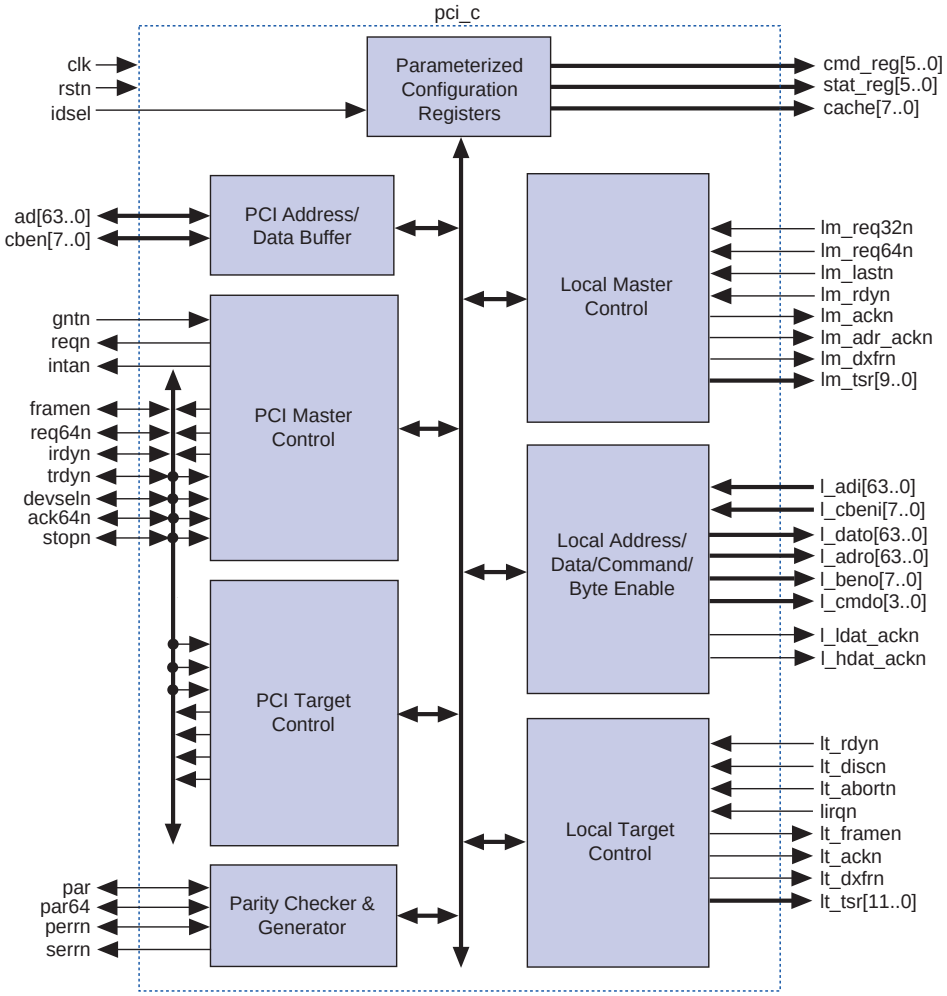

Table 1 shows the PCI bus commands that can be initiated or responded to by the pci_c MegaCore function.

Table 1. PCI Bus Command Support Summary

cben[3..0] Value	Bus Command Cycle	Master	Target
0000	Interrupt acknowledge	Ignored	Ignored
0001	Special cycle	Ignored	Ignored
0010	I/O read	Yes	Yes
0011	I/O write	Yes	Yes
0100	Reserved	Ignored	Ignored
0101	Reserved	Ignored	Ignored
0110	Memory read	Yes	Yes
0111	Memory write	Yes	Yes
1000	Reserved	Ignored	Ignored
1001	Reserved	Ignored	Ignored
1010	Configuration read	Yes	Yes
1011	Configuration write	Yes	Yes
1100	Memory read multiple *(1)*	Yes	Yes
1101	Dual address cycle	Yes	Yes
1110	Memory read line *(1)*	Yes	Yes
1111	Memory write and invalidate *(1)*	Yes	Yes

Note:

(1) The memory read multiple and memory read line commands are treated as memory reads. The memory write and invalidate command is treated as a memory write. The local side sees the exact command on the l_cbeni[3..0] bus with the encoding shown in Table 1.

Configuration Registers

Table 2 shows the defined 64-byte configuration space. The registers within this range are used to identify the device, control PCI bus functions, and provide PCI bus status. The shaded areas indicate registers that are supported by the `pci_c` function.

Table 2. PCI Bus Configuration Registers

Address	Byte			
	3	2	1	0
00H	Device ID		Vendor ID	
04H	Status Register		Command Register	
08H	Class Code			Revision ID
0CH	BIST	Header Type	Latency Timer	Cache Line Size
10H	Base Address Register 0			
14H	Base Address Register 1			
18H	Base Address Register 2			
1CH	Base Address Register 3			
20H	Base Address Register 4			
24H	Base Address Register 5			
28H	Card Bus CIS Pointer			
2CH	Subsystem ID		Subsystem Vendor ID	
30H	Expansion ROM Base Address Register			
34H	Reserved			Capabilities Pointer
38H	Reserved			
3CH	Maximum Latency	Minimum Grant	Interrupt Pin	Interrupt Line

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