System-on-a-Programmable-Chip (SOPC) Development Board

Target Applications:
Embedded microprocessor-based
solutions

Family:
APEX™ 20K

Ordering Code:
SOPC-BOARD/A4E

Vendor:

ALTERA®
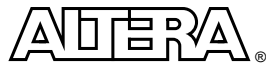
101 Innovation Drive
San Jose, CA 95134
http://www.altera.com
Tel. (408) 544-7000

Features

- Powerful development board for system-on-a-programmable-chip designs
  - Features an APEX™ EP20K400E device
  - Supports microprocessor intellectual property (IP)-based designs
- Industry-standard interconnects (requires the appropriate AMPP^SM or MegaCore™ function for operation)
  - 10/100 Ethernet with full and half duplexing
  - Peripheral component interconnect (PCI) mezzanine connector
  - High- and -low-speed universal serial bus (USB) host supporting the *Universal Serial Bus Specification, Revision 1.0*
  - IEEE Std. 1394A at 100, 200, and 400 megabits per second (Mbps)
  - IEEE Std. 1284 parallel interface
  - Two RS-232 ports data capture equipment (DCE) and data transfer equipment (DTE)
  - Two PS/2 ports for a mouse and a keyboard
- Memory subsystem
  - Two banks of 1-Mbyte synchronous SRAM cache memory
  - 64-Mbyte SDRAM in a DIMM socket
  - 4-Mbyte FLASH memory
  - 256-Kbyte EPROM
- Multiple clocks for communications systems design
- Multiple debugging ports
  - SignalTap™ embedded logic analyzer
  - IEEE Std. 1149.1 Joint Test Action Group (JTAG)
  - Extended JTAG (EJTAG)
- General-purpose connectors supporting 50 user I/O lines for custom daughter cards
- Additional features
  - VGA monitor interface (drivers required for operation)
  - Four user-defined switches and six light-emitting diodes (LEDs)
  - Liquid crystal display (drivers required for operation)
  - Application LEDs
- Applications and functions
  - Embedded systems rapid prototyping
  - Real-time hardware execution for full-speed debugging and testing
  - PCI mezzanine card (PMC) provides access to A/D and D/A converters for developing a variety of applications, including digital signal processing (DSP) and communications
  - Custom logic can be reconfigured via a programming download cable to enable fast design iteration and verification cycles
  - Rapid verification of audio, video, and data communications systems with real-time operation in a real-world environment

General Description

The Altera® System-on-a-Programmable-Chip (SOPC) Development Board is a development and prototyping platform that provides system designers with an economical solution to hardware verification. The Altera development board supports a variety of microprocessor-based designs by incorporating memory, debugging, and interface resources.

The SOPC board is primarily designed for implementing microprocessor functions and other standard IP functions in the on-board APEX device. The board includes interfaces for widely used standard interconnects. To use interconnect functions on the board, you must implement control logic into the APEX device.

The development board also supports EJTAG, which develops and debugs MIPS-like microprocessor functions, and JTAG for other system testing. For additional analysis, the JTAG port can be used with the SignalTap embedded logic analyzer, available with the Altera Quartus™ development software. Figure 1 shows a picture of the development board.

Figure 1. System-on-a-Programmable-Chip Development Board
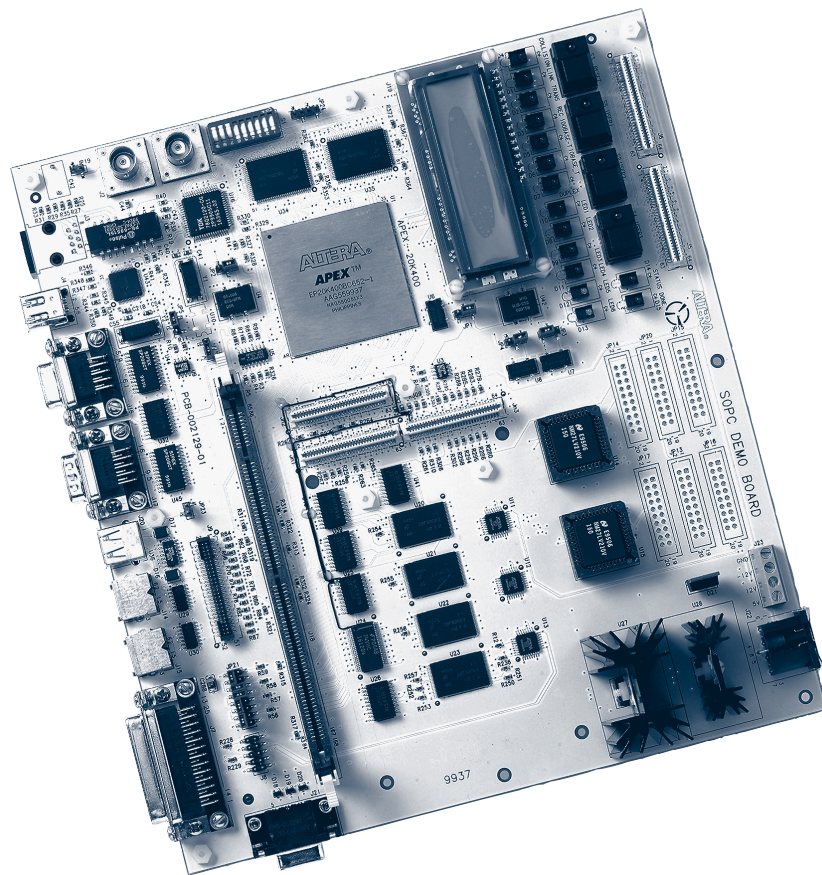
APEX EP20K400E-1 Device

The EP20K400E-1 device featured on the development board has 16,640 logic cells, 212,992 RAM bits, and 423,000 ASIC-equivalent gates in a 652-pin ball-grid array (BGA) package.

Power

The eight-layer bench-top board features four signal layers, a full 3.3-V power plane, and a split 2.5-V/5.0-V power plane. The APEX device's core power is driven at 2.5 V, and the IEEE Std. 1394A physical layer is driven at 3.3 V. An external 5.0-V power supply is required to power the board; the 5.0-V power supply regulates the 3.3-V and 2.5-V power supplies.

Clocks

The development board features ten unique clocks; the user can select up to six. The board also has two barrel nut connectors (BNC) to support communications systems design. The APEX global clock input can be driven by a 66-MHz oscillator or by an external clock via a BNC connector. The second global clock signal is connected to an oscillator that can drive an IP function at either 33 MHz or 66 MHz.

Memory

To support processor functions within the APEX device, the board includes a memory system of the following parts:

- Volatile memory: 64 Mbytes of synchronous DRAM, organized as 8 Mbytes $\times$ 64
- Non-volatile memory: 4 Mbytes of FLASH memory and a 256-Kbyte EPROM
- Pipelined cache memory with burst SRAM organized as 256 Kbytes $\times$ 32

Benefits

The SOPC board offers the user a variety of hardware and software benefits.

Hardware & Software Verification

The integration of firmware and applications software with hardware has been the traditional bottleneck in complex system designs. The development board allows both software and firmware engineering to employ a proven hardware platform early in the design cycle. Having access to a platform early in the design cycle facilitates software debugging and integration, allowing the software and hardware to evolve in parallel and enabling a shorter verification cycle.

Real-Time Hardware Execution

Hardware testing speeds the design cycle by replacing weeks of software simulation time. For complex applications involving audio, video, or high-bandwidth Internet access devices, real-time operation and debugging are essential. The SOPC board facilitates the testing process very early in the design cycle to avoid costly surprises later.

Hardware Debugging

The Altera SignalTap embedded logic analyzer allows you to find bugs rapidly. The SignalTap logic analyzer simplifies the design and debugging process by integrating the functionality of the logic analyzer into the Quartus development software, providing access to signals inside the APEX device. The SignalTap logic analyzer offers the following features:

- Provides test access to internal device nodes and I/O pins
- Captures signals while the device is running at system speeds
- Included in the Quartus software
- Does not require external probes
- Does not require changes to user design files

The development board features multiple debug ports for debugging hardware, including the JTAG and EJTAG ports used for microprocessor debugging. The SOPC board also provides connection pins for external logic analyzer use.

Flexibility & Expansion

You can operate the development board in stand-alone mode, or you can expand it through numerous general-purpose and industry-standard connectors. You can expand the system using mezzanine cards, for example, to include analog converters for targeting communications or DSP applications. A PCI mezzanine connector allows expansion via a standard off-the-shelf daughter card with the PMC form factor.
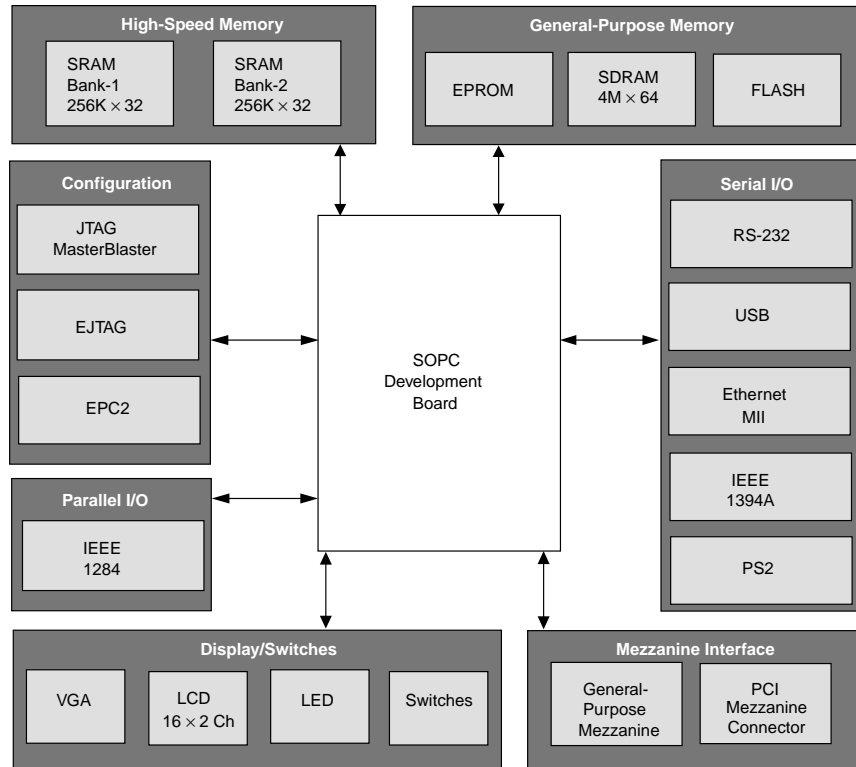
Interfaces

Table 1 describes the interfaces supported by the SOPC Development Board.

Table 1. Development Board Interfaces

Interface	Description
PCI mezzanine connector IEEE Std. 1386	This mezzanine connector supports 32 bits and 64 bits, and 33 MHz and 66 MHz. It is compliant with the **PCI Local Bus Specification, Revision 2.1**. The designer can use the connector to interface with any standard PMC daughter card.
10/100 Ethernet with full and half duplexing	The Ethernet interface consists of a transceiver and associated discrete devices. It supports implementation of an Ethernet media access controller (MAC) in the APEX device.
IEEE Std. 1394A interface	The IEEE Std. 1394A FireWire interface consists of a transceiver/arbiter and associated discrete devices. The physical interface provides a fully IEEE Std. 1394A-compliant cable port at 100, 200, and 400 Mbps for a link layer controller (LLC) function inside the APEX device.
USB host interface	The USB interface consists of a single host connection with a type-A socket. The interface supports both low-speed and high-speed operation without changing the configuration. The interface also supports a USB host interface core that can be integrated within the APEX device.
User I/O pins	The general-purpose mezzanine interface provides 50 user I/O pins that connect directly to the APEX device to support custom interfaces.
IEEE Std. 1284 parallel interface	The parallel interface is an IEEE Std. 1284-compatible transceiver. The transceiver has eight bidirectional data buffers and can be used in the extended capabilities port (ECP) mode. The designer can implement the IEEE Std. 1284 control logic in the APEX device.
Debugging ports	■ JTAG—The development board supports in-circuit debugging with the SignalTap embedded logic analyzer, which can be configured in the APEX device using the MasterBlaster™ cable. ■ EJTAG—The board has a 50-pin EJTAG header for debugging MIPS-like processors implemented in the APEX device. ■ Logic Analyzer Connection—Test connectors are provided for debugging using a logic analyzer.
VGA monitor interface	The VGA interface is only a connection and does not include the video D/A converter.
PS/2 interface	There are two PS/2 interfaces for a mouse and a keyboard connection.
RS-232C	Two RS-232C interfaces are provided: DTE and DCE. All hardware handshaking lines are supported by each interface.
MasterBlaster cable	The APEX device can be programmed directly from the Quartus development system using the MasterBlaster download cable.

The development board supports the various interfaces shown in Figure 2.

Figure 2. Block Diagram of Interfaces Supported by the SOPC Development Board

High-Speed Memory
- SRAM Bank-1 256K × 32
- SRAM Bank-2 256K × 32

General-Purpose Memory
- EPROM
- SDRAM 4M × 64
- FLASH

Configuration
- JTAG MasterBlaster
- EJTAG
- EPC2

SOPC Development Board

Serial I/O
- RS-232
- USB
- Ethernet MII
- IEEE 1394A
- PS2

Parallel I/O
- IEEE 1284

Display/Switches
- VGA
- LCD 16 × 2 Ch
- LED
- Switches

Mezzanine Interface
- General-Purpose Mezzanine
- PCI Mezzanine Connector

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com