Component Selector Guide

October 2000

Altera Corporation, The Programmable Solutions Company®, is a world leader in one of the semiconductor industry's fastest growing segments: high-density programmable logic devices (PLDs). Today's high-density PLDs, used in concert with Altera's desktop software design tools and optimized intellectual property (IP) building blocks, allow electronic systems manufacturers to execute on a single chip the same functionality that previously consumed an entire printed circuit board. From simple glue logic to complex system-on-a-programmable-chip (SOPC) solutions, Altera's devices, development tools and megafunctions ensure you get to market first.

System-on-a-Programmable-Chip Solutions

In today's changing marketplace, time-to-market is the key to success. Altera's product offerings help companies get to market first by addressing a wide range of needs from simple glue logic requirements to the challenges of system-level integration.

Altera offers a range of programmable logic device (PLD) families to fit your needs, including the APEX™, Excalibur™, FLEX®, MAX®, and ACEX™ families. Altera® devices are the fastest high-density PLDs available, with in-system speeds of over 335 MHz, clock rates up to 840 MHz, and pin-to-pin delays as fast as 3.5 ns. In addition, Altera devices offer advanced system-level features such as embedded system blocks (ESBs). ESBs can be configured as logic or several different types of memory: dual-port RAM, ROM, first-in first-out (FIFO) buffers, or content-addressable memory (CAM).

Altera products can also achieve more complex system integration tasks, such as the inclusion of processor cores. The configurable Nios™ soft core processors and high-speed ARM®- and MIPS-based™ hard core processors cut through the complexities of processor integration, allowing designers to more easily create a fully integrated SOPC.

Altera devices support changing design needs with features such as high-bandwidth, low-voltage I/O standards–e.g., the APEX True-LVDS™ circuitry with I/O performance up to 840 Mbps, and MultiVolt™ I/O, which allows easy interfacing between devices in 5.0-V, 3.3-V, 2.5-V, and 1.8-V hybrid systems. Phase-locked loops (PLLs) improve I/O performance while enhancing the ability of Altera devices to handle system-level clock management.

As a technology leader, Altera utilizes the most advanced CMOS processes as they become available to support reliable manufacturing. This process migration enhances performance and reduces manufacturing costs, enabling Altera to offer faster and more cost-effective devices. Additionally, each process advancement allows for lower power dissipation at a given device density.

Altera devices are available in a broad range of space-saving package options, including thin quad flat pack (TQFP), the innovative, area-efficient, 1.0-mm ball-pitch FineLine BGA™ packages, and 0.8-mm ball-pitch Ultra FineLine BGA packages. To complete your design solution, Altera also offers powerful development tools.

Altera's Quartus™ development software offers state-of-the-art features—such as block-level editing, integration with standard source-control software, and expanded support for megafunctions to shorten design cycles. The Quartus software also features SignalTap® logic analysis, which reduces verification time by enabling engineers to see internal chip signal values during a specified time interval while the system is running at speed. The Quartus software interfaces seamlessly with third-party EDA software tools via NativeLink™ EDA integration. As the industry's first "Internet-aware" development tool, the Quartus software provides up-to-the-minute information and file exchanges, including software updates, license file deliveries, and support services across the Internet.

Altera's MAX+PLUS® II software provides an integrated, easy-to-use development tool that supports Altera FLEX, MAX, and ACEX device families. The MAX+PLUS II software is compatible with industry-standard EDA tools and provides direct VHDL, Verilog HDL, and EDIF interfaces.

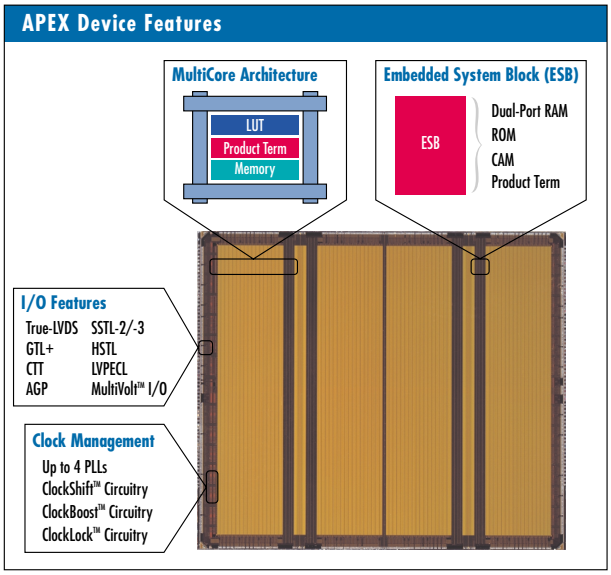
To further enhance productivity, a variety of MegaCore® and Altera Megafunction Partners Program (AMPP℠) megafunctions are available. Megafunctions are ready-made, parameterized, pre-tested blocks of intellectual property that are optimized to make efficient use of the architecture of the targeted programmable device.

APEX Devices

With densities from 30 thousand to 1.5 million gates (112 thousand to 2.5 million maximum system gates) and clock rates up to 840 MHz, the Altera APEX programmable logic family truly offers complete system-level integration on a single device. Designed to be 64-bit, 66-MHz PCI-compliant, the innovative MultiCore™ architecture combines and enhances the strengths of previous PLD architectures, delivering the ultimate in design integration and efficiency for high performance, system-on-a-programmable-chip applications.

APEX devices enable system integration at unprecedented levels, providing system designers with extensive cost and performance advantages. For example, a single EP20K400E device can integrate all of the components required to build a 1-gigabit Ethernet 8-port switch, including a MIPS-compatible processor core, MAC interfaces, FIFOs, PLLs, memory, CAM, cache memory, and all associated interfaces.

The APEX MultiCore architecture combines logic and embedded memory into a single integrated architecture, eliminating the need for multiple devices, saving board space, and simplifying the implementation of complex designs. The MultiCore architecture features embedded system blocks (ESBs) that can implement logic on several types of memory structures, including dual-port RAM, CAM, FIFOs, and ROM. The direct implementation of CAM in embedded silicon provides significant performance improvements for any pattern matching or data searching applications. Signal interconnections are provided by the FastTrack® Interconnect routing structure, which ensures fast, predictable delays.



APEX devices meet the demand for ever-increasing system performance and lower supply voltages by supporting multiple I/O interfacing standards, including LVTTL, LVCMOS, GTL+, SSTL -2/-3, AGP, HSTL, CTT, and LVPECL as well as LVDS with performance up to 840 Mbits/second. True-LVDS support has been specifically incorporated as a key high-performance I/O interface solution, and is supported via the use of dedicated serial-to-parallel conversion circuitry and LVDS-optimized PLLs. True-LVDS differential signaling also provides high board-level noise immunity and very low power consumption. Whether your design requires a high-speed interface to the PCI bus, high-performance backplane, or fast SDRAM, APEX devices can meet your performance needs. To ensure low power and maintain I/O voltage-level flexibility, APEX devices are offered at supply voltages of 2.5 V and 1.8 V, and all APEX devices support Altera's MultiVolt I/O operation.

APEX Highlights

FEATURE	BENEFIT
True-LVDS circuitry	For ultra high-speed interface capability
MultiCore architecture	Integrates LUT logic, product-term logic, and memory into a single architecture
Embedded system blocks (ESBs)	Implements logic, dual-port RAM, FIFO, ROM, and CAM functions
PCI compliance	Meets all specifications for 64-bit, 66-MHz PCI compliance and PCI-X support
Support for emerging I/O standards	Supports LVDS, LVPECL, LVTTL, LVCMOS, GTL+, CTT, AGP, HSTL, and SSTL-2/-3 I/O standards
SignalTap logic analysis	Improves verification of chip functionality
Density up to 1.5 million gates (2.5 million maximum system gates)	Addresses system-level density needs
1.8-V and 2.5-V operation	Reduces power consumption
Up to four phase-locked loops (PLLs)	Supports ClockLock, ClockBoost, and ClockShift circuitry, and 1x to 160x clock multiplication with an extended frequency range
MultiVolt I/O operation	Ideal for mixed-voltage systems
FineLine BGA packaging	Area-optimized, high-pin-count BGA offerings and packaging migration flexibility
Vertical migration	Addresses changing density and I/O needs without the need to re-spin the board

To increase system clock rates, APEX devices feature up to four PLLs with output frequencies up to 335 MHz. APEX PLLs support ClockLock™ circuitry for skew reduction, ClockBoost™ circuitry for flexible rate multiplication and division, and ClockShift™ circuitry for extended phase-shift and delay capability. These PLLs can provide improvements within an APEX device, in the interactions of an APEX device with other system components, or even serve as the clock management circuitry for an entire board-level system, providing improvements for unrelated system components.

Verification of the functionality of an APEX design is made easy with SignalTap logic analysis. The SignalTap logic analysis tool, featured in the Quartus development software and in APEX devices, integrates the functionality of a logic analyzer directly into the device, allowing a design team to perform hardware verification on a device running at actual system speed.

APEX devices are offered in a variety of packages, including space-saving 1.0-mm ball-pitch FineLine BGA packages.

Excalibur Embedded Processor Solutions

EXCALIBUR™

Combining logic, memory, and a processor core, Altera's new Excalibur embedded processor solutions allow engineers to integrate an entire system on a single PLD. The Excalibur solutions cut through the complexities of processor integration, offering the ease-of-use, fast development time, and low NRE costs needed for embedded systems development. They cover a wide range of applications, from industrial instrumentation to DSL access concentrators.

Nios Embedded RISC Processor

Nios™

The Nios soft core embedded processor family simplifies design processes and improves time-to-market. It uses as little as 2% of an APEX device, leaving most of the device's resources available for your logic functions. As the industry's first RISC-based embedded processor developed for programmable logic, it is easily parameterized, allowing you to optimize the processor and add the peripheral functions that suit your design requirements. And several Nios processors can fit onto one APEX device, giving you more design horsepower for your most demanding applications. The Nios embedded processor is available from Altera's web site at **http://www.altera.com/IPmegastore**.

ARM- and MIPS-Based Device Families

ARM® POWERED

Through partnerships with ARM® Limited and MIPS® Technologies, Altera is providing cost-effective access to advanced processor technologies to the broad marketplace. The ARM- and MIPS-based embedded processors are fast, industry-leading hard processor cores that offer unparalleled performance on a programmable chip. As with all the Excalibur solutions, designers do not need to pay royalties to use these embedded processors.

MIPS TECHNOLOGIES

Excalibur Highlights

FEATURE	BENEFIT
High-performance, RISC embedded processor architecture with speeds of up to 166 MHz and beyond	Unparalleled performance on a programmable device
Optimized integration with Altera PLD architectures	Higher system performance and access to IP blocks
Scalable	Performs powerful processing functions fast
Standard, off-the-shelf	Available without complicated licensing contracts and no royalties
Excalibur Development Kits	Everything needed to design for Excalibur embedded processors

FLEX Devices

By combining the time-to-market advantages of PLDs with the density, speed, and cost once associated exclusively with gate arrays, Altera's Flexible Logic Element MatriX (FLEX) devices are the most advanced, high-performance, and cost-effective gate array replacements available today.

FLEX 10K Family

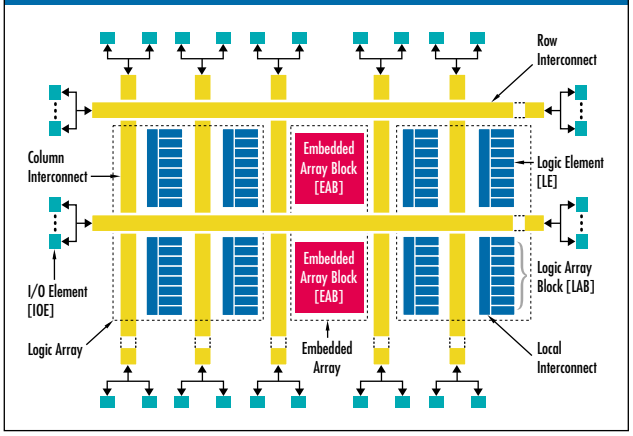
Ranging from 10,000 to 250,000 gates with up to 204-MHz system performance and 66-MHz, 64-bit PCI compliance, FLEX 10K devices combine the flexibility of programmable logic with the performance and density of embedded gate arrays. With its unique logic implementation structures—the embedded array and logic array—FLEX 10K devices revolutionize programmable logic architectures. Also, Altera's MultiVolt I/O operation and space-saving 1.0-mm ball-pitch FineLine BGA packages (featuring SameFrame™ pin-out) provide a greater level of design flexibility.

Each embedded array consists of embedded array blocks (EABs), which are ideal for ROMs, FIFOs, and asynchronous, synchronous, and dual-port RAM. Each EAB provides up to 4 Kbits of fast-access memory. The logic array contains logic-array blocks (LABs), which consist of eight enhanced logic elements (LEs) that communicate through a local interconnect. Each LE contains a four-input LUT, a programmable register, and dedicated paths for carry and cascade functions.

The 3.3-V FLEX 10KA devices extend the FLEX 10K architecture up to 250,000 gates using a 0.3-µm, four-layer-metal, CMOS SRAM process that further increases performance, lowers power consumption, and lowers costs.

FLEX 10KE devices further enhance the FLEX 10K embedded architecture. Built on a 2.5-V, 0.22-µm, five-layer-metal process, FLEX 10KE devices offer 66-MHz, 64-bit PCI performance, enhanced dual-port RAM capability, phase-locked loop (PLL) circuitry, and a programmable delay option. These enhancements provide new levels of performance and efficiency for a variety of on-chip memory requirements and complex megafunctions.

FLEX 10K Block Diagram



The FLEX 10K family is the first programmable logic device family with an embedded array.

FLEX 10K Highlights

FEATURE	BENEFIT
204-MHz system performance	Programmable solution for today's high-speed, high-bandwidth designs
66-MHz, 64-bit PCI compliance*	Meets all specifications of the PCI local bus
Density up to 250,000 gates	Addresses 90% of all gate array design starts
Dual-port RAM*	Individual read/write ports on EABs for independent read/write capability
Phase-locked loop (PLL)*	ClockLock and ClockBoost enhance device performance and provide clock multiplication
Programmable delay option*	Improves I/O performance by providing the option to adjust setup and hold times
2.5-V, 3.3-V, and 5.0-V device options	Supports multiple operating voltages
MultiVolt I/O operation	Ideal for mixed-voltage systems
FineLine BGA packaging	Area-optimized, high-pin-count BGA offering
Vertical and SameFrame migration	Addresses changing density and I/O needs without the need to re-spin the board

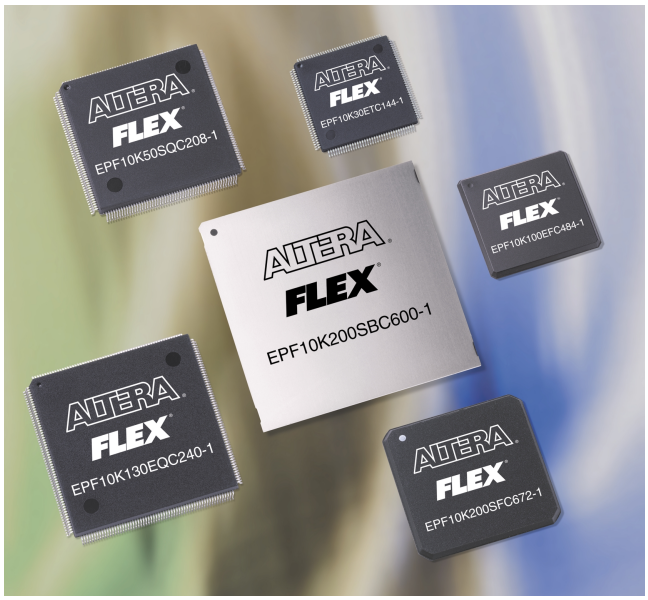
* FLEX 10KE devices only

FLEX 6000 Family

The FLEX 6000 family—which offers up to 24,000 gates and both 5.0-V and 3.3-V operation—delivers the performance, flexibility and time-to-market of programmable logic at prices that are competitive with gate arrays. FLEX 6000 devices feature the OptiFLEX® architecture—the industry's most efficient PLD architecture ever designed. Every OptiFLEX architectural feature is targeted at producing maximum performance and utilization in the smallest possible die area. This optimization, along with µPitch bond-pad technology, produces a die size that is comparable to that of a gate array and allows for a flexible and cost-effective PLD alternative to ASICs for high-volume production.

The FLEX 6000 logic array contains LABs composed of 10 LEs that communicate through a fully populated local interconnect structure. The LAB is designed to support LAB interleaving, an innovative feature that gives any LE the flexibility to access the local interconnect of its own LAB and adjacent LABs. LAB interleaving leverages the inherent speed and flexibility of local resources, while optimizing global resource usage within the FLEX architecture.

The logic array is routed through the Altera patented FastTrack Interconnect architecture. The FLEX 6000 family also supports FastFLEX™ I/O, a feature that provides a direct path from the LE to the I/O pin for fast clock-to-output times and helps meet stringent PCI timing requirements.



Today's designers know that low cost and time-to-market are critical for market success. In the past, there was an unavoidable tradeoff: use programmable logic for flexibility or use ASICs for low unit cost. The FLEX 6000 family eliminates this tradeoff by providing low-cost flexibility and high performance from initial prototyping through volume production.

FLEX 6000 Highlights

FEATURE	BENEFIT
OptiFLEX architecture	High-performance volume solution; cost-competitive with gate arrays
PCI compliance	Meets all specifications of the PCI local bus
Interleaved LABs	Leverages speed and flexibility of local interconnects
FastFLEX I/O	Maximizes I/O performance and flexibility
µPitch bond pad technology	Minimizes bond pad pitch for maximum die size reduction
3.3-V and 5.0-V device options	Supports multiple operating voltages
MultiVolt I/O operation	Ideal for mixed-voltage systems
FineLine BGA packaging	Area-optimized BGA offering
Vertical and SameFrame migration	Addresses changing design needs without the need to re-spin the board

MAX Devices

Altera's MAX device families offer solutions for high-speed applications at competitive prices. The high-performance MAX devices are based on the advanced Multiple Array MatriX (MAX) architecture and offer densities from 600 to 12,000 usable gates. These devices provide solutions for a broad array of high-performance applications, including simple PLD integration.

MAX 7000 Family

Altera's latest offering is MAX 7000B devices. Developed using a 0.22-µm process and four-layer metal, MAX 7000B devices offer the industry's first 2.5-V product-term-based devices with unprecedented pin-to-pin delays as fast as 3.5 ns. Seven high-performance, low-power MAX 7000B devices are available. These devices offer macrocell count and pin compatibility with other MAX 7000B devices. The 2.5-V MAX 7000B devices support advanced I/O standards including GTL+, SSTL-2, and SSTL-3.

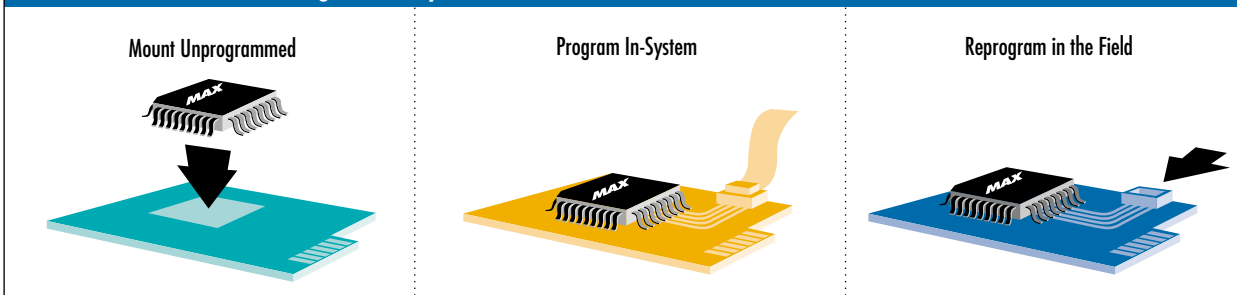
The MAX 7000 family is the fastest programmable-logic solution available in the industry. The CMOS EEPROM-based MAX 7000B devices offer propagation delays as fast as 3.5 ns, producing counter frequencies in excess of 275 MHz. With PCI-compliant, high-performance devices across the entire product line, MAX 7000 devices are ideal for a variety of high-speed applications.

The MAX 7000 family offers a wide selection of high-density devices, ranging from 32 to 512 macrocells. MAX 7000 devices are well-suited for mixed-voltage environments, offering 2.5-V, 3.3-V, and 5.0-V core supply operation with MultiVolt I/O operation that interfaces between 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices.

MAX 7000B Highlights

FEATURE	BENEFIT
3.5-ns propagation delays	Supports fast, high-speed state machines and control logic
2.5-V operating voltage	Low power consumption
Support for emerging I/O standards	Supports GTL+, SSTL-2/-3 I/O standards
PCI compliance	Satisfies PCI bus requirements
600 to 10,000 usable gates (32 to 512 macrocells)	Multiple density options for simple PLD integration
In-system programmability (ISP)	Allows for easy prototyping and in-field upgrades, and simplifies manufacturing flow
Supports Jam Standard Test and Programming Language (STAPL), JEDEC Standard JESD-71	Vendor independence, faster programming, and reduced file size
Built-in JTAG support	Simplifies device and system testing
Programmable power-saving mode	Enables >50% power reduction
MultiVolt I/O operation	Ideal for mixed-voltage systems
Ultra FineLine BGA packaging	Area-optimized BGA offering
Vertical and SameFrame migration	Addresses changing density and I/O needs without the need to re-spin the board

ISP Increases Manufacturing Efficiency



MAX 7000A, MAX 7000S, MAX 7000B, MAX 3000A, and MAX 9000 devices provide an industry-standard four-pin JTAG ISP interface for programming a device after it has been mounted on a printed circuit board.

MAX 7000B, MAX 7000A, and MAX 7000S devices offer ISP and support the vendor-independent JEDEC–approved Jam STAPL, JEDEC Standard JESD-71. MAX 7000B devices provide 2.5-V ISP, while MAX 7000A and MAX 7000S devices provide 3.3-V and 5.0-V ISP, respectively. ISP enables designers to program a device after it is mounted on a printed circuit board. ISP benefits a manufacturing environment by reducing the risk of lead damage, and benefits a design environment by allowing designers to make enhancements to a system after it has been manufactured. Jam STAPL is useful in both embedded processor and automated test equipment (ATE) applications, allowing ISP-capable devices to be programmed with smaller file sizes and in less time. MAX 7000A, MAX 7000B, and MAX 7000S devices also have built-in Joint Test Action Group (JTAG) boundary-scan test circuitry.

Features common to all MAX 7000 devices include global clocking, fast input registers, and programmable slew-rate control. These features allow MAX 7000 devices to address a broad range of system-level applications. High-speed global clocks coupled with 3.5-ns propagation delays and fast setup times create superior system performance with high-speed, device-to-device communication. The programmable slew-rate control allows system noise to be reduced by slowing the switching time of outputs that are not speed-critical. A programmable power-saving feature allows for 50% or greater power reduction in each macrocell.

MAX 3000A Family

The 3.3-V product-term-based MAX 3000A device family targets high-volume, low-cost designs. The family has an enhanced Jam STAPL, ISP, feature set, supports MultiVolt I/O operation, and ranges in density from 32 to 256 macrocells. With propagation delays as fast as 4.5 ns, MAX 3000A devices provide customers with exceptional performance at the lowest price per macrocell among Altera MAX devices.

MAX 3000A Highlights

FEATURE	BENEFIT
Low price	Ideal for low-cost, high volume applications
4.5-ns propagation delays	Provides fast system performance
600 to 5,000 usable gates	Multiple density offerings
In-system programmability (ISP)	Allows for easy prototyping and in-field upgrades, and simplifies manufacturing flow
MultiVolt I/O operation	Ideal for mixed-voltage systems
Supports Jam Standard Test and Programming Language (STAPL)	Ease-of-use for embedded processor and in-circuit testers programming applications

ACEX Devices

The LUT-based ACEX PLD family provides value and performance for cost-sensitive, volume-driven applications. These devices are ideal for the communications and consumer marketplaces, in applications such as cable modems, xDSL modems, low-cost switches, and routers.

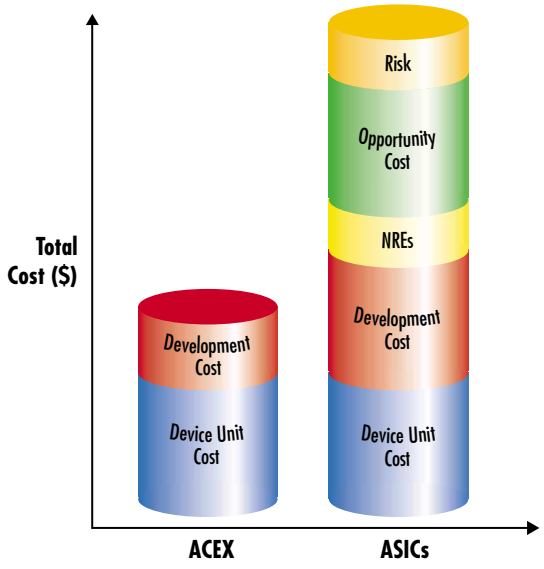
ACEX devices have the low-cost advantages of application specific integrated circuits (ASICs) and application-specific specialized products (ASSPs), with the added benefits of fast time-to-market and programmable flexibility. ACEX devices reduce time-to-market and eliminate costly delays by allowing designers to implement complete design revisions quickly, and feature in-circuit reconfiguration, powerful development software, and pre-optimized, drop-in intellectual property cores. Products can be designed, revised, released, and updated with minimal complications or delays, strengthening overall market positioning and increasing market share.

ACEX Families

The ACEX 1K family features devices based on the 0.22-µm/0.18-µm hybrid process, ranging from 10,000 to 100,000 gates. The next-generation ACEX family, the ACEX 2K family, will offer densities ranging from 20,000 to 150,000 gates. Additionally, the ACEX 2K family will support a wide range of specialized I/O standards, enabling effective high-speed, board-level communications. ACEX devices are fully 64-bit, 66-MHz compliant and feature embedded dual-port RAM and advanced packaging technologies. ACEX devices support PLL circuitry and can drive two separate ClockLock- and ClockBoost-generated signals for extensive clock management capability.

High performance, integral to volume-driven telecommunications end-user products, requires a product family that strikes the delicate balance between performance and price. ACEX devices meet these requirements. Despite their low price points, typical system performance in ACEX devices can reach speeds of 160 MHz with minimal intervention. Advanced software fitting techniques place and route designs, achieving accelerated design performance within the ACEX interconnect architecture.

ACEX Cost Performance



With the ACEX family, Altera has achieved a high level of technological innovation. ACEX 1K devices are fabricated on a hybrid 0.22-µm/0.18-µm, five-layer-metal SRAM process. This advanced process technology minimizes die size while maintaining a 2.5-V core operating voltage. Future ACEX devices will continue this trend of process innovation with smaller die sizes and lower operating voltages. Altera's patented redundancy feature is incorporated into the ACEX process, further suppressing production costs and eliminating silicon impurities. The result is significant yield improvement leading to a fully optimized process technology with lower production costs.

ACEX Highlights

FEATURE	BENEFIT
Low cost	Lowest cost-per-function in the PLD industry
High-volume solution	Ideal for price-sensitive high-volume applications
High performance	High-performance capabilities to support your most challenging application
Targeted at the communications market	Supports features and performance needed in the communications marketplace

Configuration Devices

Altera's configuration devices store configuration data for the SRAM-based APEX, Excalibur, FLEX, and ACEX devices. These devices feature ISP, MultiVolt I/O, operation over a wide density range, small form-factor packages, and fast programming times to support the APEX, Excalibur, FLEX, and ACEX device families.

Configuration Device Family

These devices are manufactured on either an EEPROM or a flash process. Altera's flash-based devices offer ISP, providing an extra level of flexibility during the prototyping stage.

With density ranges from a 500-Kbit device to the upcoming 4-Mbit device, Altera provides the widest range of configuration devices in the industry, allowing for a single-chip configuration solution for almost all APEX, Excalibur, FLEX, and ACEX devices.

All APEX, Excalibur, FLEX, and ACEX devices can control the entire configuration process and retrieve data from the configuration devices without the need for an external intelligent controller. Through the MultiVolt interface, Altera configuration devices offer operating voltage support from 1.8 V to 5.0 V. No matter how specific your system needs, an appropriate configuration device solution is available from Altera.

Configuration Device Highlights

FEATURE	BENEFIT
High density	Up to 4-Mbit, single-device configuration solutions for the high-density APEX, Excalibur, FLEX, and ACEX devices
Low cost	Lowest cost-per-bit solution available in the industry
Operating voltage support for 1.8-V to 5.0-V	Supports multiple operating voltages
In-system programmability (ISP)	Allows for easy prototyping and in-field upgrades, and simplifies manufacturing flow

APEX 20K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS[2]	I/O PINS[2]	SUPPLY VOLTAGE	LOGIC ELEMENTS	RAM BITS
EP20K30E	30,000	144-Pin TQFP, 144-Pin BGA[1], 208-Pin PQFP, 324-Pin BGA[1]	92, 93, 125, 128	1.8 V	1,200	24,576
EP20K60E	60,000	144-Pin TQFP, 144-Pin BGA[1], 208-Pin PQFP, 240-Pin PQFP 324-Pin BGA[1], 356-Pin BGA	92, 93, 148, 151 196, 196	1.8 V	2,560	32,768
EP20K100	100,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP 324-Pin BGA[1], 356-Pin BGA	101, 196, 159, 189, 252, 252	2.5 V	4,160	53,248
EP20K100E	100,000	144-Pin TQFP, 144-Pin BGA[1], 208-Pin PQFP, 240-Pin PQFP 324-Pin BGA[1], 356-Pin BGA	92, 93, 151, 183, 246, 246	1.8 V	4,160	53,248
EP20K160E	160,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 356-Pin BGA 484-Pin BGA[1]	88, 143, 175, 271, 316	1.8 V	6,400	81,920
EP20K200	200,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[1]	144, 174, 277, 382	2.5 V	8,320	106,496
EP20K200E	200,000	208-Pin PQFP, 240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[1] 652-Pin BGA, 672-Pin BGA[1]	136, 168, 271, 376, 376, 376	1.8 V	8,320	106,496
EP20K300E	300,000	240-Pin PQFP, 652-Pin BGA, 672-Pin BGA[1]	152, 408, 408	1.8 V	11,520	147,456
EP20K400	400,000	652-Pin BGA, 655-Pin PGA, 672-Pin BGA[1]	502, 502, 502	2.5 V	16,640	212,992
EP20K400E	400,000	652-Pin BGA, 672-Pin BGA[1]	488, 488	1.8 V	16,640	212,992
EP20K600E	600,000	652-Pin BGA, 672-Pin BGA[1], 1020-Pin BGA[1]	488, 508, 588	1.8 V	24,320	311,296
EP20K1000E	1,000,000	652-Pin BGA, 672-Pin BGA[1], 1020-Pin BGA[1]	488, 508, 708	1.8 V	38,400	327,680
EP20K1500E	1,500,000	652-Pin BGA, 1020-Pin BGA[1]	488, 808	1.8 V	51,840	442,368

Notes: [1] Space-saving FineLine BGA package.
[2] Preliminary. Contact Altera for latest information.

Configuration Devices for APEX, Excalibur, FLEX, and ACEX Products*

DEVICE	PIN/PACKAGE OPTIONS	SUPPLY VOLTAGE	DESCRIPTION
EPC1441	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	3.3 or 5.0 V	441-Kbit serial configuration device designed to configure all FLEX and ACEX devices
EPC1	8-Pin PDIP, 20-Pin PLCC	3.3 or 5.0 V	1-Mbit serial configuration device designed to configure APEX, Excalibur, and FLEX, and ACEX devices
EPC2	20-Pin PLCC, 32-Pin TQFP	3.3 or 5.0 V	In-system programmable 2-Mbit serial configuration device designed to configure APEX, Excalibur, FLEX and ACEX devices
EPC4	44-Pin PLCC, 100-Pin TQFP, 144-Pin FBGA	1.8 or 2.5 V	In-system programmable 4-Mbit configuration device designed to configure APEX, Excalibur, FLEX and ACEX devices

* Contact Altera for information regarding products currently under development.

Excalibur Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	LOGIC ELEMENTS	RAM BITS	EMBEDDED PROCESSOR
EPXA1	100,000	484-Pin BGA[1], 672-Pin BGA[1], 612-Pin BGA	173, 178, 178	1-8 V	4,160	53,248	ARM922T 32-bit
EPXM1	100,000	484-Pin BGA[1], 672-Pin BGA[1], 612-Pin BGA	173, 178, 178	1-8 V	4,160	53,248	MIPS32 4Kc
EPXA4	400,000	672-Pin BGA[1], 1020-Pin BGA[1], 612-Pin BGA, 864-Pin BGA	275, 360, 215, 360	1.8 V	16,640	212,992	ARM922T 32-bit
EPXM4	400,000	672-Pin BGA[1], 1020-Pin BGA[1], 612-Pin BGA, 864-Pin BGA	275, 360, 215, 360	1.8 V	16,640	212,992	MIPS32 4Kc
EPXA10	1,000,000	1020-Pin BGA[1], 864-Pin BGA	521, 365	1.8 V	38,400	327,680	ARM922T 32-bit
EPXM10	1,000,000	1020-Pin BGA[1], 864-Pin BGA	521, 365	1.8 V	38,400	327,680	MIPS32 4Kc

Notes: [1] Space-saving FineLine BGA package.
[2] Preliminary. Contact Altera for latest information.

FLEX 10K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	LOGIC ELEMENTS	RAM BITS
EPF10K10	10,000	84-Pin PLCC, 144-Pin TQFP, 208-Pin PQFP	59, 102, 134	5.0 V	-3, -4	576	6,144
EPF10K10A	10,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	66, 102, 134, 150	3.3 V	-1, -2, -3	576	6,144
EPF10K20	20,000	144-Pin TQFP, 208-Pin RQFP, 240-Pin RQFP	102, 147, 189	5.0 V	-3, -4	1,152	12,288
EPF10K30	30,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	147, 189, 246	5.0 V	-3, -4	1,728	12,288
EPF10K30A	30,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1], 356-Pin BGA, 484-Pin BGA[1]	102, 147, 189, 191, 246, 246	3.3 V	-1, -2, -3	1,728	12,288
EPF10K30E	30,000	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1], 484-Pin BGA[1]	102, 147, 176, 220	2.5 V	-1, -2, -3	1,728	24,576
EPF10K40	40,000	208-Pin RQFP, 240-Pin RQFP	147, 189	5.0 V	-3, -4	2,304	16,384
EPF10K50	50,000	240-Pin RQFP, 356-Pin BGA, 403-Pin PGA	189, 274, 310	5.0 V	-3, -4	2,880	20,480
EPF10K50V	50,000	240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[1]	189, 274, 291	3.3 V	-1, -2, -3, -4	2,880	20,480
EPF10K50E	50,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1], 484-Pin BGA[1]	102, 147, 189, 191, 254	2.5 V	-1, -2, -3	2,880	40,960
EPF10K50S	50,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1], 356-Pin BGA, 484-Pin BGA[1]	102, 147, 189, 191, 220, 254	2.5 V	-1, -2, -3	2,880	40,960
EPF10K70	70,000	240-Pin RQFP, 503-Pin PGA	189, 358	5.0 V	-2, -3, -4	3,744	18,432
EPF10K100	100,000	503-Pin PGA	406	5.0 V	-3, -4	4,992	24,576
EPF10K100A	100,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[1], 600-Pin BGA	189, 274, 369, 406	3.3 V	-1, -2, -3	4,992	24,576
EPF10K100B	100,000	208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1]	147, 189, 191	2.5 V	-1, -2, -3	4,992	24,576
EPF10K100E	100,000	208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1], 356-Pin BGA, 484-Pin BGA[1]	147, 189, 191, 274, 338	2.5 V	-1, -2, -3	4,992	49,152
EPF10K130V	130,000	599-Pin PGA, 600-Pin BGA	470, 470	3.3 V	-2, -3, -4	6,656	32,768
EPF10K130E	130,000	240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[1], 600-Pin BGA 672-Pin BGA[1]	186, 274, 369, 424, 413	2.5 V	-1, -2, -3	6,656	65,536
EPF10K200E	200,000	599-Pin PGA, 600-Pin BGA, 672-Pin BGA[1]	470, 470, 470	2.5 V	-1, -2, -3	9,984	98,304
EPF10K200S	200,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[1], 600-Pin BGA, 672-Pin BGA[1]	182, 274, 369, 470, 470	2.5 V	-1, -2, -3	9,984	98,304
EPF10K250A	250,000	599-Pin PGA, 600-Pin BGA	470, 470	3.3 V	-1, -2, -3	12,160	40,960

Notes: [1] Space-saving FineLine BGA package.

FLEX 6000 Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS
EPF6010A	10,000	100-Pin TQFP, 144-Pin TQFP	71, 81[2], 102, 139[2]	3.3 V	-1, -2, -3	880	880
EPF6016	16,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA	117, 171, 199, 204	5.0 V	-2, -3	1,320	1,320
EPF6016A	16,000	100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	81, 81, 117, 171, 171	3.3 V	-1, -2, -3	1,320	1,320
EPF6024A	24,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA, 256-Pin BGA[1]	117, 171, 199, 218, 218	3.3 V	-1, -2, -3	1,960	1,960

Notes: [1] Space-saving FineLine BGA package.
[2] Preliminary. Contact Altera for latest information.

ACEX 1K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS[2]	I/O PINS[2]	SUPPLY VOLTAGE	LOGIC ELEMENTS	RAM BITS
EP1K10	10,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	66, 102, 130, 130	2.5 V	576	12,288
EP1K30	30,000	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	102, 147, 171	2.5 V	1,728	24,576
EP1K50	50,000	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1], 484-Pin BGA[1]	102, 147, 186, 249	2.5 V	2,880	40,960
EP1K100	100,000	208-Pin PQFP, 256-Pin BGA[1], 484 Pin BGA[1]	147, 186, 333	2.5 V	4,992	49,152

Notes: [1] Space-saving FineLine BGA package.
[2] Preliminary. Contact Altera for latest information.

MAX 3000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM3032A	32	44-Pin PLCC/TQFP	34	3.3 V	-4, -7, -10
EPM3064A	64	44-Pin PLCC/TQFP, 100-Pin TQFP	34, 66	3.3 V	-4, -7, -10
EPM3128A	128	100-Pin TQFP, 144-Pin TQFP	80, 96	3.3 V	-5, -7, -10
EPM3256A	256	144-Pin TQFP, 208-Pin PQFP	116, 158	3.3 V	-6, -7, -10

MAX 7000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM7032S	32	44-Pin PLCC/TQFP	36	5.0 V	-5, -6, -7, -10
EPM7032AE	32	44-Pin PLCC/TQFP	36	3.3 V	-4, -7, -10
EPM7032B	32	44-Pin PLCC/TQFP, 49-Pin BGA[2]	36, 36	2.5 V	-3, -5, -7
EPM7064S	64	44-Pin PLCC/TQFP, 84-Pin PLCC, 100-Pin TQFP	36, 68, 68	5.0 V	-5, -6, -7, -10
EPM7064AE	64	44-Pin PLCC/TQFP, 49-Pin BGA[2], 100-Pin TQFP, 100-Pin BGA[1]	36, 40, 68, 68	3.3 V	-4, -7, -10
EPM7064B	64	44-Pin PLCC/TQFP, 49-Pin BGA[2], 100-Pin TQFP, 100-Pin BGA[1]	36, 40, 68, 68	2.5 V	-3, -5, -7
EPM7128S	128	84-Pin PLCC, 100-Pin PQFP/TQFP, 160-Pin PQFP	68, 84, 100	5.0 V	-6, -7, -10, -15
EPM7128AE	128	84-Pin PLCC, 100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 169-Pin BGA[2], 256-Pin BGA[1]	68, 84, 84, 100, 100, 100	3.3 V	-5,-7,-10
EPM7128B	128	49-Pin BGA[2], 100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 169-Pin BGA[2], 256-Pin BGA[1]	40, 84, 84, 100, 100, 100	2.5 V	-4, -7, -10
EPM7160S	160	84-Pin PLCC, 100-Pin TQFP, 160-Pin PQFP	64, 84, 104	5.0 V	-6, -7, -10
EPM7192S	192	160-Pin PQFP	124	5.0 V	-7, -10, -15
EPM7256S	256	208-Pin PQFP	164	5.0 V	-7, -10, -15
EPM7256AE	256	100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	84, 84, 120, 164, 164	3.3 V	-5, -7, -10
EPM7256B	256	100-Pin TQFP, 144-Pin TQFP, 169-Pin BGA[2], 208-Pin PQFP, 256-Pin BGA[1]	84, 120, 140, 164, 164	2.5 V	-5, -7, -10
EPM7512AE	512	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1], 256-Pin BGA	120, 176, 212, 212	3.3 V	-7, -10, -12
EPM7512B	512	144-Pin TQFP, 169-Pin BGA[2], 208-Pin PQFP, 256-Pin BGA[1], 256-Pin BGA	120, 140, 176, 212, 212	2.5 V	-6, -7, -10

Note: [1] 1.0-mm pitch FineLine BGA package.
[2] 0.8-mm pitch Ultra FineLine BGA package.

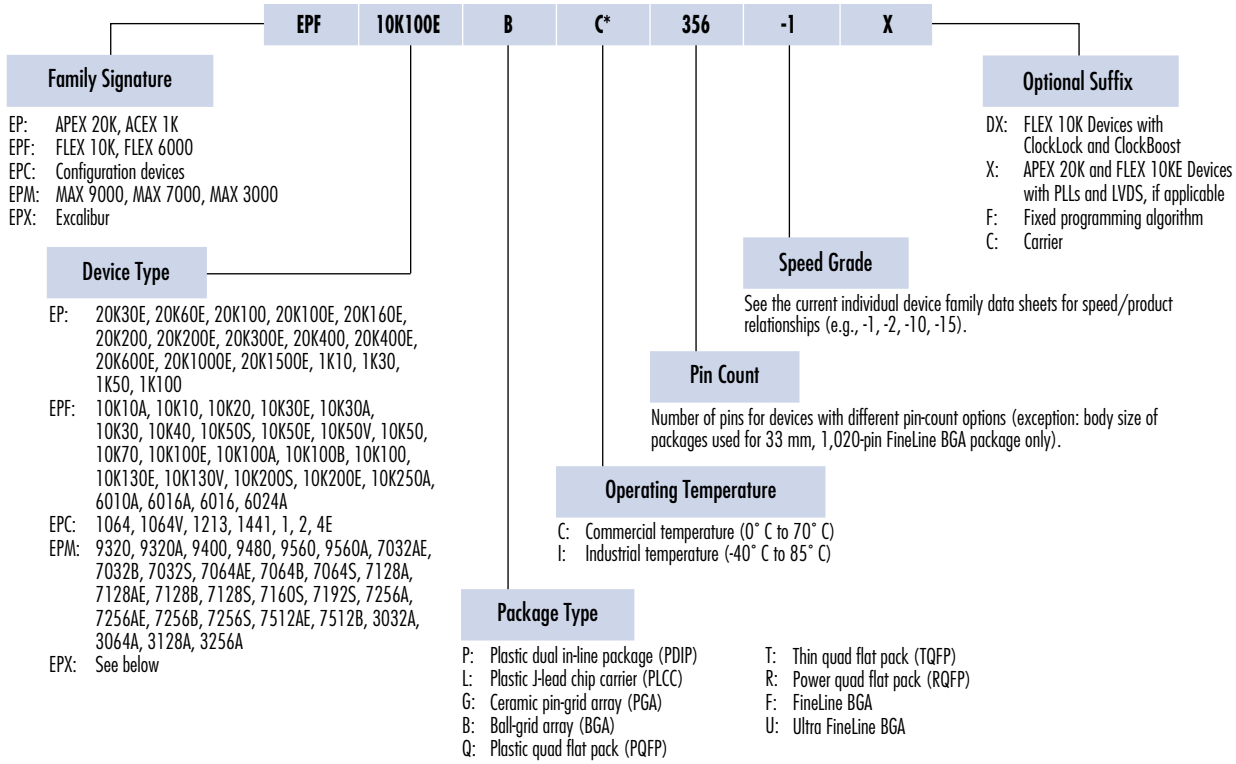
MAX 9000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM9320A	320	84-Pin PLCC, 208-Pin RQFP, 356-Pin BGA	60, 132, 168	5.0 V	-10
EPM9320	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA, 356-Pin BGA	60, 132, 168, 168	5.0 V	-15, -20
EPM9400	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	5.0 V	-15, -20
EPM9480	480	208-Pin RQFP, 240-Pin RQFP	146, 175	5.0 V	-15, -20
EPM9560A	560	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-10
EPM9560	560	208-Pin RQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP, 356-Pin BGA	153, 191, 216, 216, 216	5.0 V	-15, -20

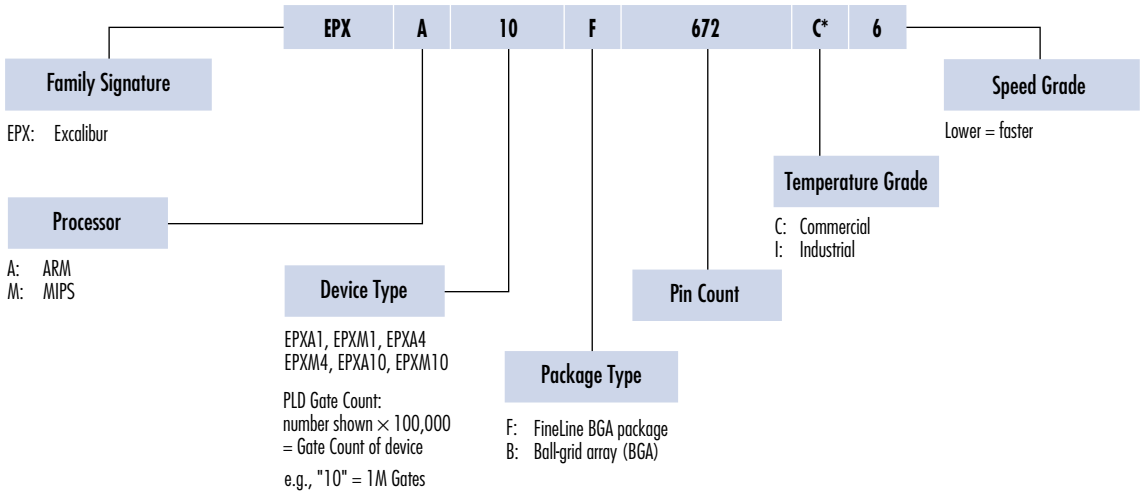
Ordering Altera Devices

The following tables list the devices available for each Altera device family as well as the configuration devices for APEX, Excalibur, FLEX and ACEX devices. The diagram below provides an explanation of Altera part numbers. Use this diagram together with the device tables to select the appropriate device, pin/package options, supply voltage, and speed grade.

Product Ordering Information



Product Ordering Information for Excalibur Devices



** Altera offers industrial packages for most of our device families. For specific device-package availability in the industrial grade, contact your local authorized Altera sales representative.*

Altera Offices

Altera Corporation
101 Innovation Drive
San Jose, CA 95134
USA
Telephone: (408) 544-7000
http://www.altera.com

Altera European Headquarters
Holmers Farm Way
High Wycombe
Buckinghamshire
HP12 4XF
United Kingdom
Telephone: (44) 1 494 602 000

Altera Japan Ltd.
Shinjuku i-Land Tower 32F
5-1, Nishi-Shinjuku, 6-Chome
Shinjuku-ku, Tokyo 163-1332
Japan
Telephone: (81) 3 3340 9480
http://www.altera.com/japan

Altera International Ltd.
Suites 908-920, Tower 1
MetroPlaza
223 Hing Fong Road
Kwai Fong, New Territories
Hong Kong
Telephone: (852) 2487 2030

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