Generating Post-Route Files in the MAX+PLUS II Software for Third-Party Verification Tools

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Introduction

Using a verification tool before device configuration or programming helps confirm the accuracy of a design. The MAX+PLUS® II software integrates seamlessly with all major EDA design tools—including tools from Cadence, Mentor Graphics, Model Technology, Synopsys, and Viewlogic—allowing designers to work with the tools they know best. This technical brief describes how to generate output files for third-party verification tools.

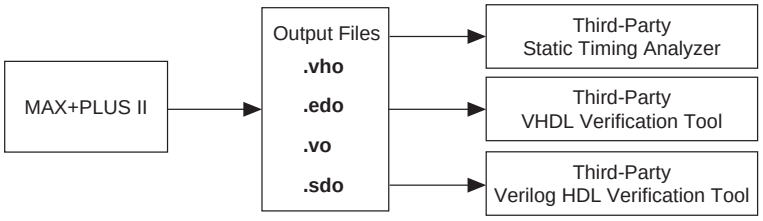
Design Flow

The MAX+PLUS II software allows you to generate an output file that can be imported into standard EDA design tools on a UNIX workstation or PC for design verification. The following formats are supported:

- EDIF Output File (**.edo**)
- VHDL Output File (**.vho**)
- Verilog Output File (**.vo**)
- Standard Delay Format (SDF) Output File (**.sdo**), which can be used with VITAL-compliant verification libraries.

Figure 1 shows a flow diagram for using Altera and third-party verification tools.

Figure 1. Altera & Third-Party Verification Tool Flow



For complete instructions on how to generate verification output files with the MAX+PLUS II software, refer to MAX+PLUS II Help. For information on using the MAX+PLUS II software with other verification tools, refer to the MAX+PLUS II Altera Commitment to Cooperative Engineering Solutions (ACCESS[SM]) Key Guidelines, which are available in the Altera Technical Support (Atlas[SM]) section of the Altera web site at **http://www.altera.com**, and on the ***MAX+PLUS II CD-ROM*** (versions 8.2 and higher).

Generating an Output File for Verification

Follow these steps in the MAX+PLUS II Compiler to compile a design and generate an output file for verification:

1. Choose **Open** (File menu), select your top-level design file, and choose **OK**.
2. Choose **Project Set Project to Current File** (File menu) to set your project for compilation.
3. Choose **Device** (Assign menu). First, specify the device family in the *Device Family* drop-down list box. Turn off the *Show Only Fastest Speed Grades* option to show all available devices in a family, and then select the target device in the *Devices* field. Choose **OK** to save your changes.

4. Set up the compilation with the appropriate Library Mapping File (**.lmf**) if your design is an EDIF file generated by a third-party synthesis tool. Refer to the MAX+PLUS II ACCESS Key Guidelines, MAX+PLUS II Help, or *Technical Brief 45 (Importing Synthesized Files from EDA Tools into the MAX+PLUS II Software for Place & Route)* for details.

5. Adjust synthesis settings and timing requirements for your design before compilation, if necessary. Refer to MAX+PLUS II Help for details.

6. Instruct the MAX+PLUS II software to generate the output file(s) for third-party verification tools by turning on the **EDIF Netlist Writer**, **Verilog Netlist Writer**, and/or **VHDL Netlist Writer** commands (Interfaces menu).

   You can specify options for the output file(s) with the **EDIF Netlist Writer Settings**, **Verilog Netlist Writer Settings**, and/or **VHDL Netlist Writer Settings** commands (Interfaces menu). The filename(s) for the output file(s) are the same as the user-defined chip name(s) for the project; if no chip names exist, the Compiler assigns filenames that are based on the project name. For a multi-device project, the MAX+PLUS II software also generates a top-level output file that is uniquely identified by "_t" appended to the project name. You can also create an EDIF Command File (**.edc**) to customize the EDIF Output File for a particular verification environment.

7. Choose **Start** in the MAX+PLUS II Compiler to begin compilation.

After the MAX+PLUS II Compiler has finished compilation, you can import the output file into a third-party verification tool. When using a Verilog Output File, you must use both the <*project name*>**.vo** file and the **alt_max2.vo** file. Refer to MAX+PLUS II Help for details.

Refer to the MAX+PLUS II ACCESS Key Guidelines or to your EDA verification tool's user guide for information on simulating EDIF, VHDL, and Verilog HDL files with a third-party verification tool.

More Information

Altera provides extensive support documentation to help you design with the MAX+PLUS II software successfully with third-party EDA simulation tools. For technical support, contact Altera Applications at (800) 800-EPLD. You can also e-mail your technical questions to Altera at **sos@altera.com**. For answers to common questions regarding the Altera/EDA software tool interface, search the Atlas Solutions on the Altera web site.

The following documents provide more detailed information:

- MAX+PLUS II ACCESS Key Guidelines
- *MAX+PLUS II Programmable Logic Development System & Software Data Sheet*
- *EDA Software Support*
- *Technical Brief 45 (Importing Synthesized Files from EDA Tools into the MAX+PLUS II Software for Place & Route)*

These documents are available by contacting Altera Literature Services at (888) 3-ALTERA; you can also download them from the Altera web site at **http://www.altera.com**.

Revision History

The information published in *Technical Brief 49 (Generating Post-Route Files in the MAX+PLUS II Software for Third-Party Verification Tools)* version 1.01 supersedes information published in previous versions.

Technical Brief 49 (Generating Post-Route Files in the MAX+PLUS II Software for Third-Party Verification Tools) version 1.01 contains the following changes:

- Corrected the filename extension for the Verilog Output File (**.vo**).
- Made minor textual and style changes.

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