Advantages of APEX PLLs Over Virtex DLLs

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Altera has enhanced the phase-locked loop (PLL) circuitry on APEX™ devices to increase device and board-level performance. PLLs minimize clock skew and clock delay and support clock synthesis applications. To support multiple-clock System-on-a-Programmable-Chip™ designs, Altera has added up to four PLLs to APEX 20KE devices. Clock delay and clock skew affect system timing and printed circuit board (PCB) reliability. To address these issues, designers can use either PLLs found in APEX devices or delay-locked loops (DLLs) found in Xilinx Virtex devices. Although both can be used to reduce the amount of skew and delay for system clocks, PLLs are more flexible than DLLs for frequency synthesis applications. This technical brief describes the performance advantages of PLLs over DLLs.

PLLs in APEX devices help meet the clock management requirements for integrating multiple system-level functions onto a single device. The APEX architecture features up to four PLLs per device and contains ClockLock™, ClockBoost™, and ClockShift™ circuitry for increased performance and flexible clock frequency multiplication and division. Table 1 describes the functions of each circuitry type.

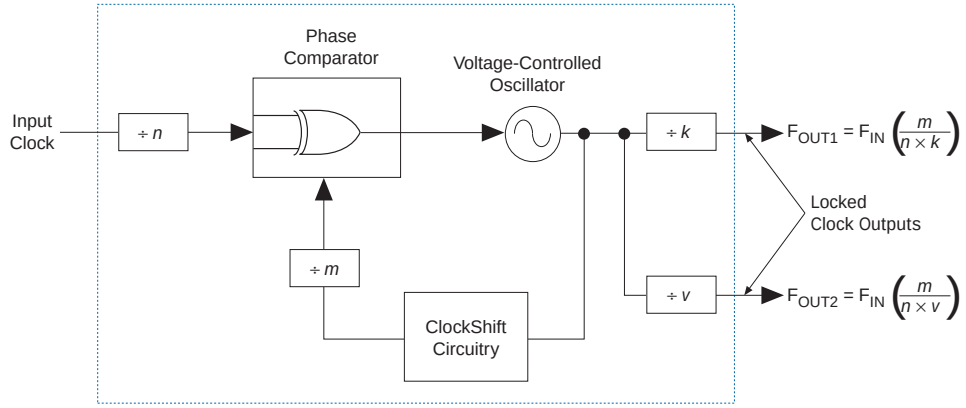
Table 1. APEX PLL Circuitry Features

Circuitry	Description
ClockLock	Reduces internal delay and clock skew between other devices on the PCB.
ClockBoost	Provides programmable clock frequency multiplication and division, and allows time domain multiplexing.
ClockShift	Provides programmable phase shift and precise clock delay management.

PLL Fundamentals

PLL circuits monitor a reference signal, such as a system clock, to manage or synthesize other clocks. In a PLL, a phase comparator measures the difference between the phase and frequency of an external reference signal and an internal feedback signal. Based on this difference, the phase comparator adjusts the voltage-controlled oscillator (VCO), which produces a timing signal clock that is fed back to the phase detector. This signal is compared with the incoming reference signal. When the reference signal and the VCO feedback signal are identical, the PLL is "locked" onto the reference signal. The PLL continues to monitor the reference signal and adjust the VCO output to compensate for any temperature or voltage fluctuations. Figure 1 shows a block diagram of an APEX PLL.

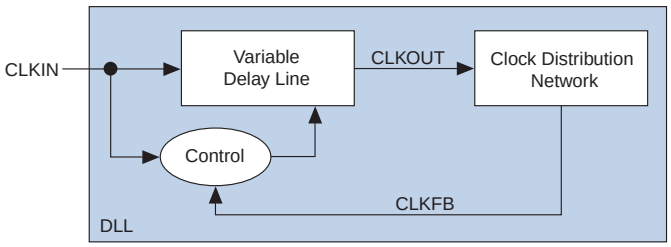
Figure 1. APEX PLL Circuitry



DLL Fundamentals

DLL circuits also monitor a reference signal for clock management. The operation of a DLL is fundamentally the same as a PLL, except that a delay line is used instead of a VCO to generate the output timing signal. The delay line inserts a given amount of delay between the input clock and the feedback clock, so that two rising edges align. Figure 2 shows a block diagram of the Virtex DLL.

Figure 2. Virtex DLL Circuitry *Note (1)*



Note:
(1) Source: Xilinx XAPP 132: Using the Virtex Delay-Locked Loop.

Advantages of APEX PLLs Over Virtex DLLs

APEX 20KE PLLs provide several advantages over Virtex-E DLLs, including:

- APEX 20KE PLLs provide full multiplication and division capabilities.
- ClockShift circuitry provides fine control of clock phase and clock delay.
- APEX 20KE PLLs support the low-voltage differential signaling (LVDS) standard with data transfer rates up to 622 Megabits per second (Mbps).
- APEX 20KE PLLs support very low input clock frequencies (as low as 1.5 MHz).
- APEX 20KE PLLs support T1/E1 rate conversions.
- APEX 20KE PLLs filter out high-frequency jitter.

Table 2 compares the features of the APEX PLL and the Virtex DLL.

Table 2. APEX PLL & Virtex DLL Comparison

Feature	APEX 20KE PLL	Virtex-E DLL *(1)*
Circuitry	Analog	Digital
Number of PLLs (DLLs)	Up to 4	8
Clock multiplication	Any number up to 133	1×, 2× *(2)*
Clock division	Any number up to 106	1.5, 2, 2.5, 3, 4, 5, 8, or 16 only
Coarse clock adjustment	90°, 180°, 270°	90°, 180°, 270° *(3)*
Fine clock adjustment	0.5 ns resolution (up to 360°)	None
Input frequency range	1.5 to 160 MHz	25 to 200 MHz
Output frequency range	1.5 to 622 MHz *(4)*	1.5 to 320 MHz
622-Mbps output for LVDS support	Yes	No
T1/E1 rate conversion	Yes	No

Notes:
(1) Source: Virtex data sheet.
(2) Xilinx claims Virtex supports 4× clock multiplication by cascading two DLLs together.
(3) 90˚ and 270˚ are not usable for higher frequencies.
(4) The maximum output frequency for 622 MHz is for LVDS. General purpose PLL maximum output frequency is 200 MHz.

ClockBoost Circuitry for Programmable Clock Synthesis

A system clock may run at a different frequency than some of the PCB components. A CPU, for example, may require an internal clock that is several times faster than the system I/O bus clock. The APEX 20KE analog PLLs provide *m/n* scaling that supports frequency multiplication of up to 133× and division by any number up to 106. This advanced feature provides designers with true programmable clock synthesis, greatly enhancing design flexibility and performance. Virtex-E digital DLLs provide only 1× and 2× multiplication and only allow division by 1.5, 2, 2.5, 3, 4, 5, 8, or 16 as shown in Table 2. This limited frequency synthesis support does not address the needs for high-performance designs.

ClockShift Circuitry for Precise Phase & Time Delay Management

APEX 20KE ClockShift circuitry provides programmable phase shift and precise time delay management. The fine clock adjustment uses incremental step delays of 0.5 to 1.0 ns, allowing the output clock to lead or lag the input clock by up to 360˚. The coarse clock adjustment allows clock phase to be adjusted by 90˚, 180˚, or 270˚. The programmable delay also lets designers implement strict timing margins that cannot be met without clock adjustment. This feature enables designers to improve t_{CO} and t_{SU} times to meet high-speed interface requirements. Virtex-E DLLs are limited to clock phase adjustments of 90˚, 180˚, and 270˚ only and do not support the fine clock adjustments required by designs with strict timing requirements.

LVDS Support

LVDS is a high-speed I/O interface standard that supports data rates at speeds up to 622 Mbps. Standard LVDS implementation currently used in discreet chips requires a 7× or 8× clock multiplicaiton. APEX 20KE devices have special deskew circuitry, dedicated parallel-to-serial circuitry, and PLLs that provide 8× and higher clock multiplication to support LVDS at 622 Mbps. Xilinx claims that DLLs have a maximum output clock rate of 320 MHz. Because of their digital circuitry, DLLs can not support 8× clock multiplicaiton, making LVDS support at 622 Mbps highly unlikely.

T1/E1 Conversion Rates

The general purpose PLLs in APEX 20KE devices include special circuitry to support T1/E1 conversion. The T1 telecommunications standard (used in the United States) uses a 1.544 MHz clock rate while the E1 telecommunications standard (used in Europe) uses a 2.048 MHz clock rate. PLLs support a special mode that allows T1 to E1 clock rate conversion and vice versa. Virtex-E DLLs do not support this conversion.

PLLs Filter Out High-Frequency Jitter

The analog circuitry of the APEX 20KE PLL translates to a time-continuous transfer function. This transfer function acts as a filter on the PLL input clock, attenuating high-frequency jitter. The discrete delay line architecture of a digital DLL is not capable of filtering the jitter on the input clock. For DLLs, the input jitter accumulates to the output. The Xilinx DLL output jitter specification (cycle to cycle) of $\pm$ 60 ps is for 0 input jitter. All input jitter is passed through to the outupt. For example, if the input clock has $\pm$ 200 ps of jitter going into a DLL, the DLL output clock will have a jitter of $\pm$ 260 ps.

Conclusion

APEX PLLs, supported by advanced ClockLock, ClockBoost, and ClockShift circuitry, provide significant improvements in system performance and design versatility by minimizing clock skew and clock delay. The flexible clock synthesis and robust clock shift capabilities of APEX PLLs provide precise phase and delay adjustment. Designers can increase system performance by minimizing t_{SU} and t_{CO}. PLLs allow support for high-performance I/O standards such as LVDS and provide the flexibility and the capability unattainable by Virtex-E DLLs. With these advantages, APEX PLLs dramatically increase system performance.

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