Advanced Synthesis with FPGA *Express*

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Introduction

Altera now provides all customers who have an active subscription with a full-featured version of the Synopsys FPGA *Express*™ software. This world-class synthesis tool increases and enhances designer productivity.

All customers who have an active subscription will receive the FPGA *Express* software version 3.4 with their Quartus™ software version 2000.03 and MAX+PLUS® II software version 9.6 upgrade shipment.

FPGA *Express* Software Version 3.4 Features

The FPGA *Express* software is a powerful synthesis tool with a host of advanced features:

- Integrated schematic viewer enables the Register Transfer Language (RTL) code and the synthesized design to be viewed as a schematic
- Constraint table for entering constraints and displaying results
- Fault tolerant or safe implementation of state machines
- Integrated scripting tool supports Tool Command Language (Tcl) scripting
- Support for library of parameterized module (LPM) components without setting attributes to black box the component
- Multiple-device design flow
- Architecture-specific optimization for Altera® APEX™ 20K and FLEX® 10K devices
- Support for Windows 98/NT operating systems

Increased Performance & Greater Flexibility

With the FPGA *Express* software, Altera customers now have access to a world-class synthesis tool that provides optimized synthesis for Altera devices.

Easy Access to Information Using the Integrated Schematic Viewer & Constraint Tables

The FPGA *Express* software offers an integrated schematic viewer for designers to view RTL code as a schematic and inspect a design for inferred operators. The schematic viewer also allows designers to verify that the hardware description language (HDL) code was inferred as expected and view the optimized design after targeting an Altera device. Features such as carry and cascade chains, look-up tables (LUTs), and ATOMs can also be viewed with the schematic viewer.

Designers can enter constraints in easy-to-use constraint tables. Options such as I/O register implementation, skew rate and clock constraints can be specified in the constraint tables. If the design is hierarchal, modules can be individually optimized for speed or area.

After a device is optimized, results are displayed in the constraint table with additional information, including logic elements (LEs) used, and flip-flop and timing met/not met information on a module-by-module basis. Path timing is reported in a three-level table with the level of detail increasing from `table1` to `table3`. Results are tightly integrated with the schematic viewer for cross probing.

Fault-Tolerant & Fault-Safe State Machine Operation

The FPGA *Express* software provides designers with the option of fault-tolerant or fault-safe implementation of state machines. Fault-tolerant synthesis increases performance and decreases area utilization. Safe implementation ensures that all states, legal and illegal, have legal transitions as specified by the "When Others' Construct" field, but may have a negative impact on area and timing quality or results (QOR).

Tcl Scripting Functionality

The FPGA *Express* software also has an integrated FPGA scripting tool (FST) which supports Tcl-based commands. All of the functionality of the FPGA *Express* software can be accessed with the scripting tool in either batch mode, or interactively from the shell command line.

Automatic Black Boxing

Designers can use LPM components in the FPGA *Express* software without setting any attributes to black box the component. The FPGA *Express* software will automatically black box it. Thus, component wrappers generated by the MegaWizard™ Plug-In Manager in the Quartus and MAX+PLUS II design systems can be used to declare and instantiate components in the design source code. Designers can also declare and instantiate components for APEX 20KE device megafunctions like the `ALTCLKLOCK`, `ALTLVDS` and `ALTCAM`. See the white paper at **http://www.synopsys.com/products/fpga/altera_megawiz_white.html** for an example. The FPGA *Express* software can also infer operators as "+" etc. and map them to LPM components directly.

Multiple Device Design Flow

Designers can now take advantage of a multiple-device design flow. Designers can target a single design to different Altera devices within the same project. Constraints remain the same, allowing the designer to simply select a new device for the project. This allows the designer to compare performance between different device families and speed grades.

Conclusion

The advanced features of the FPGA *Express* software allow designers to quickly perform synthesis and optimize designs for use with Altera devices. Powerful features such as an integrated schematic viewer, constraint table input, and safe implementation of state machines provide for easy system-on-a-programmable-chip designs.

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