System-on-a-Programmable-Chip Development Board

July 2000, ver. 1.1 User Guide

Features

- Powerful development board for system-on-a-programmable-chip (SOPC) designs
  - Features an APEX™ EP20K400E 652-pin device
  - Supports microprocessor intellectual property (IP)-based design
- Industry-standard interconnects
  - 10/100 Ethernet with full and half duplexing
  - Peripheral component interconnect (PCI) mezzanine connector
  - High- and low-speed universal serial bus (USB) host supporting the ***Universal Serial Bus Specification, Revision 1.0***
  - IEEE Std. 1394a at 100, 200, and 400 megabits per second (Mbps)
  - IEEE Std. 1284 parallel interface
  - Two RS-232 ports (DCE and DTE)
  - Two PS/2 ports for mouse and keyboard
- Memory subsystem
  - Two banks of 1-Mbyte cache memory
  - 64-Mbyte SDRAM in a DIMM socket
  - 4-Mbyte Flash memory
  - 256-Kbyte EPROM
- Multiple clocks for communications systems design
- Multiple debugging ports
  - SignalTap™ embedded logic analyzer
  - IEEE Std. 1149.1 Joint Test Action Group (JTAG)
  - Extended JTAG (EJTAG)
- Supports 50 user I/O lines
- Additional features
  - VGA monitor interface
  - Four user-defined switches and six LEDs
  - Liquid crystal display
  - Application LEDs
- Applications
  - Embedded systems prototyping
  - Communications systems design
  - IP development and debugging

Introduction

This user guide provides information on the development board and includes the following topics:

General Description

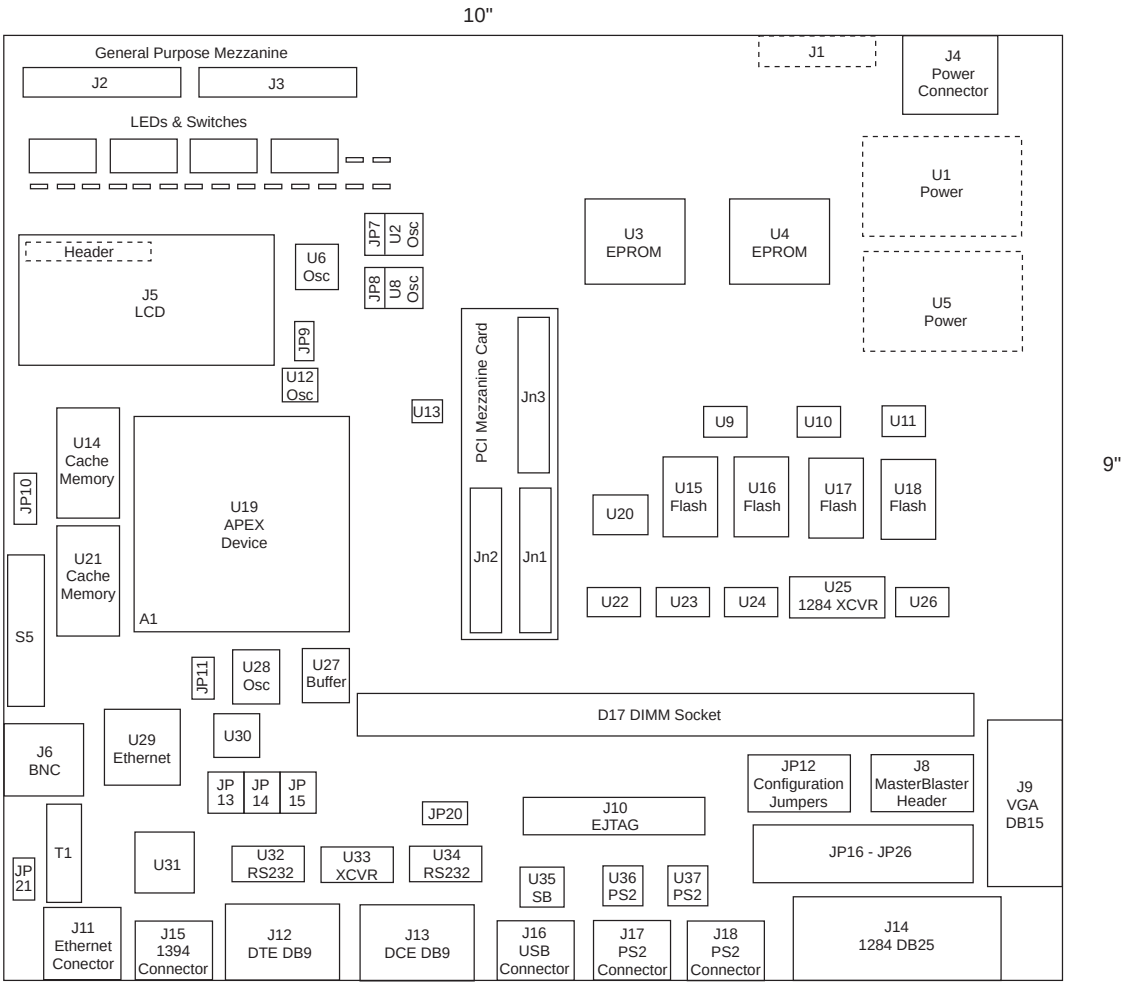
The Altera® system-on-a-programmable-chip board is a development and prototyping platform that provides system designers with an economical solution for hardware verification. The system-on-a-programmable chip board supports a variety of microprocessor-based designs, incorporating memory, debugging, and interface resources.

The development board is primarily designed for implementing microprocessor functions and other standard IP functions in the on-board APEX device. The board includes physical interfaces for widely used standard interconnects. Control logic for the interconnects can be implemented in the device. Some of the available IP solutions include:

- Processor cores (MIPS, RISC, and Harvard)
- Peripheral and I/O cores (PCI, SDRAM controllers, UART, USB, ethernet, IEEE1394, IEEE 1284)
- Other cores developed by Altera and Altera Megafunction Partners Program (AMPP™) partners

The board also supports EJTAG for development and debugging of MIPS-like microprocessor functions, as well as JTAG for system testing. For additional analysis, the JTAG port can be used with the SignalTap embedded logic analyzer available with the Quartus™ development software. Figure 1 shows a layout diagram of the development board.

Figure 1. System-on-a-Programmable-Chip Board Layout Diagram



APEX Device

The EP20K400E device features 423,000 ASIC-equivalent gates in a 652-pin FineLine BGA™ package. The device has 16,640 logic cells and 212,992 RAM bits.

Power

The eight-layer development board has four signal layers: a full 3.3-V power plane, and a split 2.5-V, 5.0-V power plane. The APEX device's core power is driven at 2.5 V, and the IEEE Std. 1394 physical layer is driven at 3.3 V. An external 5.0-V power supply provides power to the board and regulates the 3.3-V and 2.5-V supplies.

Tables 1 through 3 list the estimated power requirements for the development board.

Table 1. 12.0-V Supply Requirements

Module	mA (12.0 V)	mA (–12.0 V)	Power (W)
PMC	100	100	2.5 Maximum
General Purpose Mezzanine	100	100	2.5 Maximum

Table 2. 5.0-V Supply Requirements

Module	mA (5.0 V)	mA (–5.0 V)	Power (W)
PMC	1,000	–	5.0 Maximum
General Purpose Mezzanine	1,000	–	5.0 Maximum
P/S2 Keyboard	50	–	0.25
P/S2 Mouse	50	–	0.25
DTE UART	50	–	0.25
DCE UART	50	–	0.25
USB	100	–	0.5
Ethernet	–	–	–
Parallel	70	–	0.4
VGA	–	–	–
Configuration	20	–	1.0
LCD	20	20	0.2
Two red LEDs	10	–	0.1
Two yellow LEDs	10	–	0.1
Two green LEDs	10	–	0.1

Table 3. 3.3-V Supply Requirements

Module	mA (3.3 V)	Power (W)
APEX DC current for VCCIO	1,500	5.0
PMC	1,500	5.0 Maximum
General Purpose Mezzanine	1,500	5.0 Maximum
SSRAM A	600	2.0
SSRAM B	600	2.0
SDRAM	600	2.0
Flash	300	1.0
EPROM	300	1.0
FireWire (1394)	115	0.4
Ethernet	150	0.5
Configuration	0	0

Table 4. 2.5-V Supply

Module	mA (1.8 V)	Power (W)
APEX DC current for VCCINT	6,000	15

The total power requirement for the development board is about 60 W. The 5.0-V, 12.0-V, and –12.0-V supplies are provided externally, while the 1.8-V and 3.3-V supplies are derived from the board. Only the 5.0-V supply needs to be provided unless you are using mezzanines that require a 12.0-V or –12.0-V supply.

The board includes reverse voltage and status LEDs. Connectors are also included to support both laboratory bench supplies and commercially available PC-style power supplies.

Environmental Requirements

The development board must be stored between 40 °C and 100 °C. Operational temperatures must fall between 0 °C and 55 °C. The development board also requires commercial grade components and must be convection cooled.

Clocks

The board supports up to six unique clocks that can be selected by the designer for a total of ten. The board has two BNC connectors to support communications systems design. The APEX global clock input is driven by a 66-MHz oscillator or by an external clock via a BNC connector. The second global clock signal is connected to an oscillator that can drive a PCI function at either 33 or 66 MHz.

Memory

To support processor functions implemented in the APEX device, the board includes a memory system consisting of the following:

- Volatile memory: 64 Mbytes of synchronous DRAM, organized as 8 Mbytes × 64 Mbytes
- Non-volatile memory: 4 Mbytes Flash memory and a 256-Kbyte EPROM memory
- Pipelined cache memory with burst SRAM organized as 256 Kbytes × 32 Kbytes

Interfaces

Table 5 describes the interfaces supported by the board.

Table 5. Development Board Interfaces

Interface	Description
PCI PMC IEEE Std. 1386 connector	This mezzanine connector supports 32 and 64 bits and operates at 33 and 66 MHz. It is compliant with the ***PCI Local Bus Specification, Revision 2.1***. The connector can be used by designers to build an interface to PCI functions in the APEX device.
10/100 ethernet with full- and half-duplexing	The 10/100 ethernet interface consists of a transceiver and associated discrete devices and allows implementation of an ethernet media access controller (MAC) in the APEX device.
IEEE Std. 1394a interface	The IEEE Std. 1394a FireWire interface consists of a transceiver/arbiter and associated discrete devices. The physical interface provides an IEEE Std. 1394a-compliant cable port at 100, 200, and 400 Mbits per second for a link layer controller (LLC) implemented as a function inside the APEX device.
USB host interface	The USB host interface consists of a single host connection with a type A socket. The interface supports both low-speed and high-speed operation without changing the configuration.
User I/O pins	The general-purpose mezzanine interface provides 50 user I/O pins that connect directly to the APEX device, supporting custom interfaces.
IEEE Std. 1284 parallel interface	The parallel interface is a IEEE Std. 1284-compatible transceiver. The transceiver has eight bidirectional data buffers and can be used in extended capabilities port (ECP) mode. The designer can implement the IEEE Std. 1284 control logic in the APEX device.
Debugging ports	The board supports in-circuit debugging with the SignalTap embedded logic analyzer, which can be configured in the APEX device and the MasterBlaster™ communications cable. The board also has a 50-pin EJTAG header for debugging MIPS-like processors implemented in the APEX device.

General Information

Once power is applied to the board, the LCD display reads "SOPC DEMO BOARD." This message indicates that the EP20K400E device has successfully configured itself and is functional. The development board status program is contained within the EPC2 Flash PROM devices provided on the development board.

☞ Before handling the card, you should take proper anti-static precautions. The board can be easily damaged without proper anti-static handling.

Initial Setup

To begin using the board, a complete initial setup must be performed by following these steps:

1. Complete the assembly and inspect the board.
2. Apply power.
3. Program the APEX device.
4. Reset the board.

Inspecting the Board

Place the board on an anti-static surface and inspect the board to ensure that it has not been damaged during shipping. Make sure that all components are on the board and appear intact. To complete the board assembly, insert the SDRAM module (shipped separately) into the DIMM slot.

Applying Power

You can apply power to the board using either the eight-pin power supply connector (J22) or the terminal block (J1) with a bench power supply. If you choose to power the board using the terminal block, you must provide a 5.0-V supply and a ground connection. All of the board components are powered directly from the 5.0-V supply. The 12.0-V and –12.0-V inputs are used to provide the required voltages to the PMC mezzanine as required by the specification.

If you apply power through the terminal block (J1), use a power supply, which is capable of providing 5.0 A to the 5.0-V input. This value meets the typical maximum requirements for the board. To ensure that adequate power is provided, monitor the input current and voltage using the power supply or a digital multimeter.

If you apply power through the 8-pin power supply connector (J4), then you must purchase the power cord. You can directly connect the Total Power International Inc. HES100-30 power supply to the board at J4. The supply is capable of providing the maximum required power.

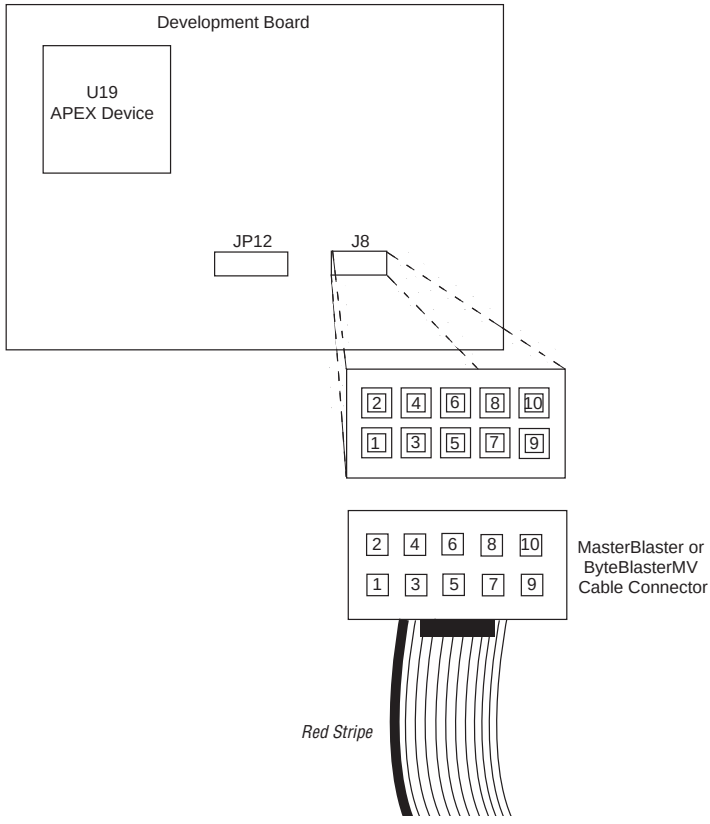
Depending on testing conditions, the maximum power required by the board is 100 W. This condition occurs if both mezzanine interfaces are used at the same time, in addition to the devices on the board.

Programming the APEX Device

The APEX 20K device is programmed via the JTAG interface. During initial power up, the APEX 20K device receives configuration data from the EPC2 configuration devices if the configuration devices contain data. If the configuration devices are not programmed, the APEX device will remain unconfigured.

You can program the APEX device directly using the Quartus software version 2000.02 and higher or the MAX+PLUS® II software version 9.5 and higher using either the MasterBlaster™ or ByteBlasterMV™ cable. Figure 2 shows how to connect the MasterBlaster or ByteBlasterMV cable to the development board.

Figure 2. Connecting the MasterBlaster & ByteBlasterMV Cables



☞ The development board may be damaged if the MasterBlaster or ByteBlasterMV cables are not plugged in correctly.

Refer to Quartus Help for instructions on how to configure devices using the MasterBlaster cable.

The green LED D2 will illuminate after the APEX 20K device is successfully configured indicating that the configuration is complete. At this point, press the Reset switch. If an error occurred during configuration, the red LED D1 will illuminate, indicating that the APEX 20K device was not successfully configured. The APEX 20K device must be reprogrammed each time the board is powered down, but retains its programming information if the board is reset.

The EPC2 configuration device may also be programmed using the MAX+PLUS II software and a MasterBlaster, ByteBlasterMV, or BitBlaster™ download cable. EPC2 configuration devices are accessible using the JTAG interface. The APEX 20K device only attempts to load configuration data from an EPC2 device on initial power up. If configuration data is changed while the board is turned on, new data is not loaded into the APEX 20K device until the board is turned off and on.

EPC2 configuration devices contain a small program that configures the LCD display to read "SOPC DEMO BOARD" on power up.

Resetting the Board

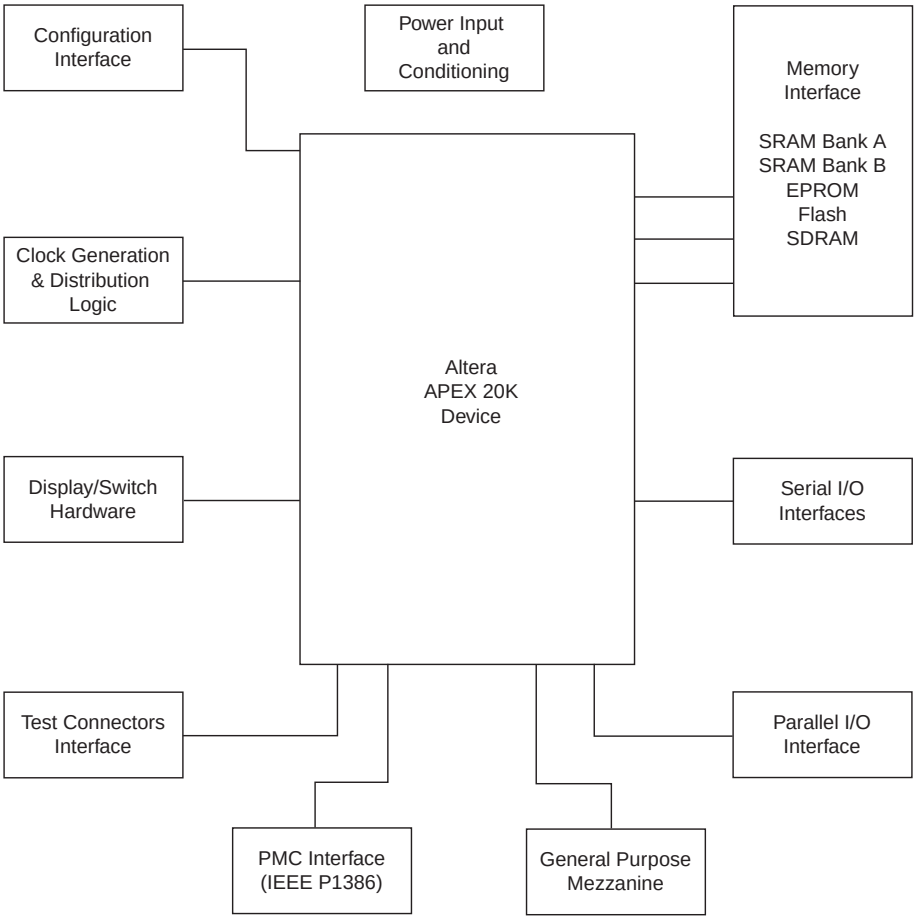
A master reset switch (S1) resets the APEX 20K device through the DEV_CLRn input signal. This is not a board-level reset. Any devices that need to be reset are driven from the APEX device, and the signals must be connected to the reset switch internally. This allows devices on the board to be reset independently from the global reset without requiring additional hardware to prevent contention.

A second switch (S2) is connected to a dedicated low-skew input pin (B17) and is provided as an alternative reset option if the DEV_CLRn input signal is not used. This may be configured internally in the APEX device.

Functional Overview

This section provides a brief overview of the development board components. Figure 3 shows a functional block diagram of the development board.

Figure 3. Development Board Block Diagram



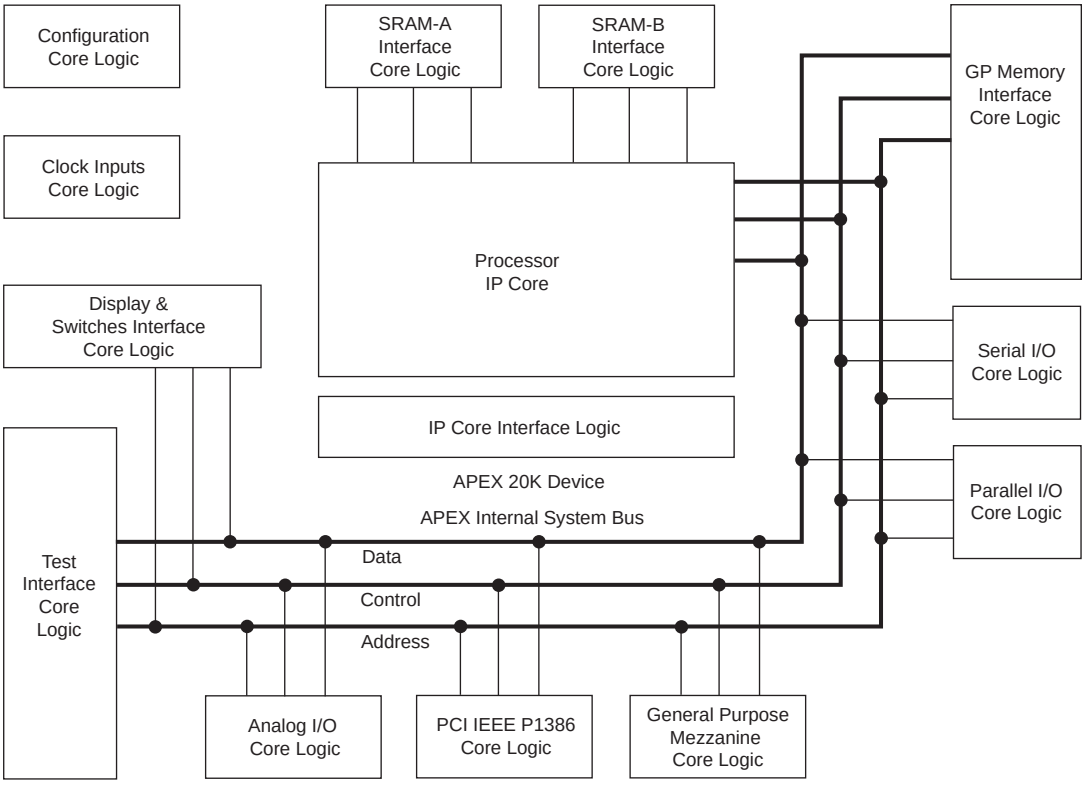
APEX Device

The main component of the development board is the EP20K400EBC652-1 device. The APEX device's package is a 652-pin FineLine BGA package. Table 6 lists the features of the APEX device and Figure 4 is a block diagram of the APEX device interface.

Table 6. APEX 20K400E Device Features	
Feature	**Specification**
Maximum gates (logic and RAM)	1,052,000
Typical gates	213,000 to 423,000
Logic elements (LEs)	16,640
Embedded system blocks (ESBs)	104
Maximum RAM bits	212,992
Maximum macrocells	1,664
Maximum user I/O pins	502
Internal supply voltage	2.5 V
MultiVolt™ I/O interface voltage levels	3.3, 2.5 V
Dedicated power inputs	150
Package	652 BGA
I/O count	496
Dedicated clock inputs	6

For more information about the EP20K400E or other APEX devices, see the *APEX 20K Programmable Logic Device Family Data Sheet*.

Figure 4. APEX Device Block Diagram



Memory Interfaces

Three memory buses interface with the APEX 20K device. These interfaces include a general-purpose memory bus, a Flash memory bus, and an EPROM memory bus. Two synchronous SRAM (SSRAM) memory buses are also connected to the APEX device. The buses provide the development board with four types of memory.

Two SSRAM banks provide cache memory for a processor core, and are accessed using dedicated buses to optimize performance. The SDRAM and non-volatile memory share common general-purpose data and address buses while maintaining separate control signals. Figure 5 illustrates the architecture of the development board memory system.

Figure 5. APEX Device Memory Architecture

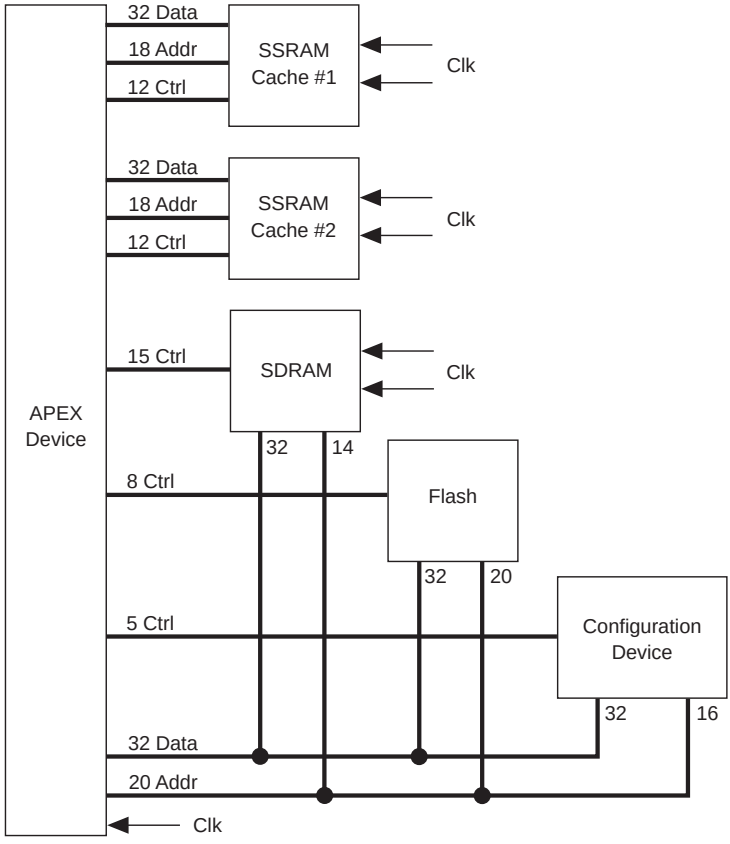


Table 7 lists the memory characteristics for the development board.

Table 7. Development Board Memory Characteristics

Type	Address Lines	Data Lines	Control Lines	Memory Organization	Size	I/Os Used	Power Budget
SSRAM A	18	32	14	256 × 32	1 Mbyte	64	2.0 W
SSRAM B	18	32	14	256 × 32	1 Mbyte	64	2.0 W
SDRAM	20	32	16	8Mb × 32	64 Mbytes	79	2.0 W
Flash	20	32	8	64k × 32	4 Mbytes	79	1.0 W
EPROM	20	32	3	64k × 32	256K	79	1.0 W

SDRAM Memory

The SDRAM memory configuration is compliant with the *PC SDRAM Unbuffered DIMM Specification, Revision 1.0*. The development board supports configuration types 8 and 9 from this specification. Refer to Table 62 on page 59 for a list of SDRAM control lines.

The address and data lines are shared by all devices connected to the general-purpose memory bus. The SDRAM module does not use all of the address lines, because memory is accessed through both a row and a column address.

SDRAM memory is connected to the general-purpose address bus, as defined in the *PC SDRAM Unbuffered DIMM Specification Revision 1.0* for 8Mbyte × 64 modules. Module address bits 0 to 11 are connected to the corresponding bits of the general-purpose address bus. Module address bit 12 is unused. Module bank address bits 0 and 1 are connected to general-purpose address bits 13 and 12, respectively.

The SDRAM module is 64 bits wide, while the general-purpose memory data bus is 32 bits wide. To accommodate this, the data bus is doubly loaded. Bit 0 of the general-purpose data bus is connected to both bit 0 and bit 32 of the module data bus, and so on.

Improper handling of the data byte mask bits during SDRAM reads can cause contention on the data bus.

The SDRAM byte-enable lines control the data bus. `DQM[3..0]` accesses the lower 32 bits, and `DQM[7..4]` accesses the upper 32 bits. Ensure that two byte lanes sharing common bits are not active at the same time. For example, if `DQM[0]` is enabled, `DQM[4]` must not be enabled. Refer to Table 60 on page 57 and Table 61 on page 58 for a list of general-purpose data and address lines.

SDRAM is clocked from the same clock source as the APEX device's processor clock for the APEX device to ensure that the interface remains synchronous. This can be either the 66-MHz clock crystal, the variable crystal, or the external input. The SDRAM interface has been tested up to 66 MHz. Table 8 shows the SDRAM module control signals.

Table 8. SDRAM Module Control Signals		
Signal	**I/O**	**Description**
RAS#	1	Row address strobe
CAS#	1	Column address strobe
WE#	1	Write enable
CS[0..1]#	2	Module chip selects
DQM[0..7]	8	Data byte mask
CKE	1	Clock enable
SDA	1	Serial data
SCL	1	Serial clock

Flash Memory

A 1Mbyte × 32 Flash memory bank is connected to the general-purpose memory bus and provides four Mbytes of memory. The bank is implemented using four 1Mbyte × 8 Flash devices. Write protection can be provided by connecting WP# to a jumper block instead of, or in addition to connecting it to the APEX device. Refer to the APEX device data sheet for detailed information on how to access this device. Table 64 on page 60 provides a list of the Flash control lines.

Because of the significant loading on shared address buses, the Flash and EPROM memory devices are separated from the other address bus by transceivers. These devices are always enabled so additional control is not required; however, the propagation delay through the transceiver should be taken into account for timing analysis. Table 9 provides information on the devices used to implement the Flash memory.

Table 9. Flash Memory Interface Device Reference			
Reference Designator	**Part Number**	**Manufacturer**	**Description**
U15, U16, U17, U18	MT28F800B3WG-10T	Micron	1Mbyte × 32 Flash Memory
U23, U22, U20	SN74LV245BDW	Texas Instruments	Bus Transceiver

The 1Mbyte × 32 Flash memory is implemented using four 1Mbyte × 8 devices. Table 10 lists the Flash memory control signals.

Table 10. Flash Control Signals

Signal	I/O	Description
CS#	1	Chip select
OE#	1	Output enable
RP#	1	Reset pulse
WP#	1	Write protect
WE[0..3]#	4	Byte write enable

EPROM Memory

The 64Kbyte × 32 EPROM memory is implemented using two EPROM devices, each organized as 64Kbyte × 16. The bus transceivers used to isolate the EPROM and Flash devices must be considered for the timing of the EPROM interface. Refer to Table 63 on page 59 for a list of the EPROM control lines. Table 11 lists information on the devices used to implement the EPROM memory. The EPROM memory devices are installed in 44-pin PLCC sockets to allow for easy replacement. The EPROM devices are not configured upon delivery. Table 12 lists the EPROM control signals.

Table 11. EPROM Memory Interface Device Reference

Reference Designator	Part Number	Manufacturer	Description
U3, U4	NM27LV21OV	Fairchild Semiconductor	64K × 32 EPROM Memory

Table 12. EPROM Control Signals

Signal	I/O	Description
CS	2	Chip select
OE	1	Output enable

High-Speed Memory Interface

The board contains two synchronous 256Kbyte × 32 SRAM memory banks. Each bank is implemented with one SSRAM device and is separately connected to the APEX device. Both memory devices are synchronous with the processor clock used for the APEX device, and are intended to be used as cache memory for a processor core inside the APEX device.

Tables 65 through 67 on pages 60 and 61 contain information on the address, data, and control lines for SSRAM Bank 1. Tables 68 through 70 list information on the address, data, and control lines for SSRAM Bank 2.

All possible control lines have been connected to the APEX device to allow maximum flexibility of the memory interface. Some control lines may not be required for a particular design and these signals may be left tri-stated, because all control lines are pulled inactive on the board. The parity option for the SSRAM was not connected. Table 13 provides information on the devices used to implement the two SSRAM memory banks. Table 14 lists the SSRAM module control signals.

Table 13. SSRAM Memory Interface Device Reference

Reference Designator	Part Number	Manufacturer	Description
U21	MT8L256L32DT-10	Micron	256Kbyte × 32 SRAM Bank 1
U14	MT58L256L32DT-10	Micron	256Kbyte × 32 SRAM Bank 2

Table 14. SSRAM Module Control Signals

Signal	I/O	Description
ADV	1	Address advance
ADSC	1	Address status processor
ADSP	1	Address status controller
CE#	1	Chip enable
CE2	1	Chip enable
OE#	1	Output enable
GW#	1	Global write
BW[0..3]	4	Byte write enable
BWE#	1	Byte write enable
Mode	1	Burst mode sequence
ZZ	1	Power down enable

Design Considerations

Designs can be improved by following a few basic guidelines. To do this, perform a timing analysis, especially when specifying setup and hold constraints for SSRAM and SDRAM. High-fanout signals on the general-purpose memory buses may require buffering and is especially true of the address signals. It is likely that each synchronous memory bank will require two clock cycles at the core clock frequency. This yields a total of seven loads, including the APEX device. If all types of memory are not available with 3.3-V supply voltages, level translation buffers may be required.

Clock Generation & Distribution

The APEX device uses four global clock inputs and one low-skew dedicated input which (used as a clock input) brings the total clock input count to five. Refer to the *Jumper Configuration* section for detailed information on configuring the clock options on the development board.

The EP20K400E device has four internal phase-locked loop (PLL) circuits, which are available for use on the development board. A jumper enables the APEX PLL circuitry. For a diagram of the jumper configuration, see Figure 8 on page 40. Table 15 shows the required development board clocks.

Table 15. Required Development Board Clocks

Interface	Required Clocks
Core processor and synchronous memory	66 MHz External
1394	24.576 MHz
USB	48 MHz
Ethernet (receive clock)	25 MHz
Ethernet (transmit clock)	25 MHz
PCI mezzanine	33/66 MHz
General-purpose mezzanine	External
VGA	25.175 MHz
EJTAG	External

APEX 20KE devices provide four dedicated clock pins and four additional dedicated input pins available for broad, low-skew routing. Because three of the dedicated inputs are required for other interfaces, five inputs may be used for clocks. Some of these pins must be shared to support all 11 required clock signals.

Configuration Interface

The APEX device may be configured using the Quartus software and the MasterBlaster download cable. Alternatively, the three EPC2 configuration devices configure the APEX device upon power-up. Table 59 on page 56 provides a list of configuration signals.

Each time power is applied to the board, the APEX device checks for configuration information stored in the EPC2 configuration devices and loads any available information. If you change the configuration device's programming information, you must turn the board off and on before new information can be loaded into the APEX device.

The EPC2 devices may be programmed through the JTAG interface. Refer to the *Jumper Configuration* section for detailed information on configuring the JTAG interface. The EPC2 device can be programmed with the Quartus software version 2000.02 or later and the MAX+PLUS II software version 9.5 or later and the using either the MasterBlaster or ByteBlasterMV communication cables.

If configuration data is targeted at the EPC2 devices, start the Quartus and MAX+PLUS II software and the EPC2 device as an output option to create the required Programmer Object Files (.**pof**) files. If the EPC2 devices are not targeted, the Quartus software will generate a single file required to program the APEX device directly.

Configuration Interfaces

Table 16 shows the data sources for configuration that are available for the APEX device.

Table 16. Supported Configuration Schemes

Configuration Scheme	Data Source
Configuration devices	EPC2 configuration device
JTAG	MasterBlaster download cable

EPC2 Device Configuration

The EPC2 device section consists of three EPC2 devices with reprogrammable Flash memory. The devices are also a part of the on-board JTAG chain to allow in-system programming.

MasterBlaster Communications Cable

The MasterBlaster communications cable has a 10-pin header for use with the development board. The communications cable allows you to directly download configuration data to the APEX device. The development board supports only JTAG download mode, not passive serial download mode. The MasterBlaster cable also supports in-circuit debugging with the SignalTap embedded logic analyzer.

Two LEDs are provided on the communications cable: a green LED for use with the CONF_DONE signal and a red LED for use with the nSTATUS signal.

The board header supply voltage is 5.0 V and supplies a maximum of 1 W.

Serial I/O Interface

The development board contains several serial I/O interfaces. For each serial interface, the transceiver and any associated hardware are provided on the board. The logic controllers must be implemented inside the APEX device. The interfaces on the board include:

- RS-232C data terminal equipment (DTE) and data communications equipment (DCE)
- USB
- IEEE-1394a (FireWire)
- PS/2
- 10/100 Base-T ethernet

RS-232C Interface

Two RS-232C interfaces are provided with the development board: a DTE and a DCE interface. All hardware lines are provided for each interface. Table 17 provides information on the devices used to implement the RS-232C interface.

Table 17. RS-232C Interface Device Reference

Reference	Part Number	Manufacturer	Description
U32	SP208CT	Sipex	RS-232C DTE transceiver
U34	SP208CT	Sipex	RS-232C DCE transceiver
U33	SN74LV245BDW	Texas Instruments	Bus transceiver

The transceiver used for both interfaces requires a 5.0-V power supply. The signals going into the APEX device are beyond the maximum 3.3-V input voltage range. A 3.3-V bus and a transceiver with 5.0-V tolerant inputs are used to shift signals going into the APEX device. This feature is always enabled so no additional control is required. Since the bus transceiver is always active, the RS-232C input pins cannot be used as outputs or contention will occur. If these pins are not used as part of a design, ensure that they remain in the high-impedance (input) state. See Table 71 on page 63 and Table 72 on page 64 for information on the RS-232C DTE and DCE signals.

DTE UART Interface

The APEX device may use a UART core which is directly connected to a device to provide the RS232C interface levels. Table 18 shows the DTE UART interface characteristics.

Table 18. DTE UART Interface Characteristics

Features	I/O Pins	Voltage	Power Budget
Tx, Rx & Control	7	5.0	0.25 W

DCE UART Interface

The APEX device may use a UART core which is connected to a device on the board to provide the RS232C interface levels.

Table 19. DCE UART Interface Characteristics

Features	I/O Pins	Voltage	Power Budget
Tx, Rx & Control	7	5.0	0.25 W

USB Interface

The USB interface consists of a single host connection with a type-A socket. The interface is capable of both low- and high-speed operation without changing the configuration. A jumper allows 5.0 V to be output to the cable and can be useful when connecting a passive device, such as a mouse, to the port. Do not use this feature if it is not required, because it may cause two power supplies to be connected together. Table 20 provides information on the device used to implement the USB interface.

Table 20. USB Interface Device Reference

Reference Designator	Part Number	Manufacturer	Description
U35	SP5301CN	Sipex	USB Transceiver

Table 75 on page 65 provides information on USB control lines.

The APEX device may use a USB core that implements the USB Serial Interface Engine (SIE) and is connected to a device to provide the USB interface. Table 21 shows the USB interface characteristics.

Table 21. USB Interface Characteristics

Feature	I/O Pins	Voltage	Power Budget
USB interface	10	5.0 V	0.5 W

IEEE-1394a (FireWire) Interface

The IEEE-1394a FireWire interface consists of a transceiver/arbiter and associated components. The physical interface provides an IEEE-1394a compliant cable port at 100/200/400 Mbits per second for a link layer controller (LLC) implemented as a core inside the APEX device.

The transceiver/arbiter generates the clock for the LLC inside the APEX device, which is required to synchronize the data coming from the LLC to the transceiver. Eight data lines are provided for data transfers between the LLC and the transceiver. The number of data lines required for the LLC core depends on the transmission rate used for the FireWire bus. The local bus clock always maintains the same frequency. To transfer the data to the transceiver faster for higher transmission rates, the data bus width must increase. Table 22 shows the data bus requirements for different transmission rates.

Table 22. FireWire Data Bus Usage versus Transmission Rate

Data Rate (Mbits per Second)	Data Bus Pins	Comments
100	D[1..0]	Minimum speed for two data pins at 49.152 MHz
200	D[3..0]	Four data pins at 49.152 MHz to double the data rate
400	D[7..0]	All eight data pins used to double the data rate again

The power control pins for the FireWire interface are pulled low, providing a self ID of 0 because the interface cannot source power to the cable, nor does it require any power from the cable. Table 23 lists information on the device used to implement the FireWire interface.

Table 23. FireWire Interface Device Reference

Reference Designator	Part Number	Manufacturer	Description
U31	TSB41LV03	Texas Instruments	IEEE-1394a three port transceiver and arbiter

The APEX device can use an IEEE 1394 core, directly connected to a device to provide the 1394 interface. Table 24 shows the FireWire interface characteristics. Table 76 on page 66 provides more information on the FireWire control interface signals.

Table 24. FireWire Interface Characteristics

Feature	I/O Pins	Voltage	Clocks (MHz)	Power Budget
1394 Interface	15	3.3 V	24.576	0.4 W

PS/2 Interface

Two PS/2 interfaces are provided with the development board for connecting a mouse and a keyboard. The transceiver provides the correct voltage level translation for the peripheral devices. Power and ground are also provided, because the mouse and keyboard are passive devices. Table 25 provides information on the devices used to implement the PS/2 interface.

Table 25. Keyboard & Mouse Interface Device Reference

Reference	Part Number	Manufacturer	Description
U36	DM7404M	Fairchild Semiconductor	Mouse interface buffer
U37	DM7404M	Fairchild Semiconductor	Keyboard interface buffer

Table 73 on page 64 provides detailed information on the PS/2 keyboard interface, and Table 74 on page 65 provides information on the PS/2 mouse interface. The APEX device may use a core, connected to a device to provide the PS/2 keyboard and mouse interfaces. Table 26 shows the keyboard and mouse interface characteristics.

Table 26. Keyboard & Mouse Interface Characteristics

Feature	I/O Pins	Voltage	Power Budget
Keyboard and mouse	8	5.0 V	0.25 W

10/100 Ethernet Interface

The ethernet interface consists of a transceiver, or PHY, and associated discrete components. This allows you to implement an ethernet media access controller (MAC) in the APEX device. As shown in Table 77 on page 67, the connections consist of the standard media independent interface (MII) and additional signals. Table 27 provides information on the devices used to implement the ethernet interface.

Table 27. Ethernet Interface Device Reference

Reference	Part Number	Manufacturer	Description
U29	78Q2120-64CG	TDK	Ethernet MII transceiver

Parallel I/O Interface

The parallel I/O interface consists of an IEEE-1284 compatible transceiver. Table 28 provides information on the device used to implement the parallel port interface.

Table 28. IEEE-1284 Interface Device Reference

Reference	Part Number	Manufacturer	Description
U25	74VHC161284MEA	National Semiconductor	IEEE-1284 (parallel port) transceiver
U24, U26	SN74LV245BDW	Texas Instruments	Bus transceiver

The parallel interface transceiver has eight bidirectional data buffers and can be used in extended capabilities port (ECP) mode. The interface provides enough buffers to connect all ECP control signals from the controller to the peripheral device. Internal pull-up resistors eliminate the need for external resistors for the high drive open drain buffers used to drive the data lines connected to the external device.

The parallel port interface uses a 5.0-V supply, with output signals set to 5.0 V. Two 3.3-V supply bus transceivers with 5.0-V tolerant inputs are used on APEX device input signals. The bidirectional data bus uses U24 and the transceiver direction is connected to the direction control for the IEEE-1284 transceiver. No additional control is required; however, the timing for the bus transceiver must be considered as part of the interface. The second transceiver is always enabled. If the signals are not used, the APEX device pins must always be left in the high-impedance (Input) state.

For further information on the parallel port control lines, see Table 78 on page 68 and Table 79 on page 70.

For the parallel port interface to operate normally, the APEX device contains the host controller and the external device serves as the peripheral. The parallel port interface can also be configured so that the APEX device can act as a peripheral device. Port direction is controlled by nine jumpers (JP19-34). Jumper positioning determines the direction of the parallel port. When all jumpers are placed in the 1-2 position, the parallel port will be in host mode, which is required for normal operation. By placing all jumpers in the 2-3 position, the directions for the control lines are reversed and the board interface operates as a peripheral. For proper operation, all jumpers must be in the same position. Table 78 on page 68 and Table 79 on page 70 provides information on the parallel port control lines. Table 29 shows the IEEE 1284 interface characteristics.

Table 29. IEEE 1284 Interface Characteristics

Feature	I/O	Voltage	Power Budget
1284 parallel port	19	5.0 V	0.4 W

Mezzanine Interfaces

A PCI Mezzanine Card (PMC) site is included on the board. The interface is 32 or 64-bit 33 or 66-MHz capable, operates at 3.3 V, and is ***PCI Local Bus Specification, Revision 2.2*** compliant.

See the following references for more detailed information on the PMC interface.

- ***PCI Local Bus Specification, Revision 2.2***.
- Standard for Physical and Environmental Layers for PCI Mezzanine Cards: PMC IEEE P1386.1.
- Standard for a Common Mezzanine Card Family: CMC IEEE P1386/Draft 2.0.

No user I/O pins are provided for the PMC interface. All user I/O pins from the PMC are provided through connectors mounted directly on the mezzanine card. Clearance is provided on the board to support a PMC with user I/O connectors as required by the CMC specification. For detailed information on the PCI interface and connector pinouts, refer to PMC and CMC specifications (IEEE-1386).

Table 81 on page 72, Table 82 on page 73, and Table 83 on page 73 list the PMC signal pin assignments.

APEX Device Signal Definition

Table 30 shows the definitions for the APEX device signals required to implement the PMC interface.

Table 30. APEX Device Signal Definitions

32-Bit PCI			
Function	**Signals**	**Number**	**I/O Format**
Address and data	AD[31:0] C/BE[3:0]# PAR	37	3.3-V PCI
Interface control	FRAME# TRDY# IRDY# STOP# DEVSEL# LOCK#	6	3.3-V PCI
Error reporting	PERR# SERR#	2	3.3-V PCI
Arbitration	REQ# GNT#	2	3.3-V PCI
Interrupts	INTA# INTB# INTC# INTD#	4	3.3-V PCI
Cache support	SBO# SDONE	2	3.3-V PCI
System	CLK RST#	2	3.3-V PCI
64-Bit PCI			
Address and data	AD[63:32] C/BE[7:4]# PAR64	37	3.3-V PCI
Arbitration	REQ64# GNT64#	2	3.3-V PCI

Some signals are not included in the above table. IDSEL is a PCI signal used as a device select for configuration cycles and is generally connected to one of the address lines. The PMC JTAG port signal can be daisy-chained with the APEX device JTAG port without using any APEX device I/Os. BUSMODE signals are defined to allow different specifications in the same mezzanine form factor.

Board-Level Issues

The PMC interface requires no devices on the board level, assuming that the PCI interface is implemented in the APEX device.

As the APEX device only supports 3.3-V PCI I/O, 5.0-V PMCs are not supported. PMCs can use up to 7.5 W and are supported by the development board.

The PCI clock signal should be driven to both the PMC CLK pin and to one of the APEX device dedicated clock inputs. This signal must comply with the PCI electrical and timing requirements.

The PCI mezzanine card standard only defines operation at 33 MHz. However, the development board is designed to support 66 MHz signaling. Table 31 lists the PMC-PCI interface characteristics.

Table 31. PMC-PCI Interface Characteristics

Interface Features	I/O Pins	Voltages	Clocks	Power Budget
PMC-PCI Interface	94	+/– 12 V	33 MHz	7.5 W
	94	3.3 V	66 MHz	7.5 W

General-Purpose Mezzanine Interface

The general-purpose mezzanine interface provides an additional custom interface prototyping area. The interface includes 38 general-purpose user I/O lines, power (3.3 V, 5 V, 12 V, and –12 V), and clock pins. The clock interface is synchronous with the main processor and memory clock to ease the effort required to interface with the rest of the board.

The general purpose mezzanine interface also includes a JTAG chain so that devices can be programmed using the same interface as devices on the development board.

External feedback pins for the PLL circuitry are also connected to the general-purpose mezzanine interface. This allows an optional method for externally connecting these signals. They may also be internally connected to the APEX device.

Table 84 on page 75 and Table 85 on page 76 provide a list of the general-purpose mezzanine signal pin assignments.

A socket is available for a user defined clock, which is distributed to both the APEX device and the general-purpose mezzanine connector. In addition, a BNC connector for an external clock signal can be selected. Table 32 shows the PMC-GP interface characteristics.

Table 32. PMC-GP Interface Characteristics

Feature	I/O Pins	Voltages	Clocks	Power Budget
PMC-GP interface	38	12, –12 V	Socket	7.5 W
	38	3.3 V	Socket	7.5 W

Display & Switch Interfaces

A two-row, 16-character liquid crystal display (LCD) is provided on the board. The LCD has an integrated controller and operates from a single 5.0-V supply. The LCD display is an Emerging Technologies ED162A0RU display that uses a Hitachi HD44780U controller. See Table 33.

Table 33. IEEE-1284 Interface Device Reference

Reference Designator	Part Number	Manufacturer	Description
J5	ED162A0RU	Emerging Display Technologies	2 × 16 Character display (connected through a 1 × 16 header)
N/A	HD44780U	Hitachi	LCD controller (installed on the display)
U7	SN74LV245BDW	Texas Instruments	Bus transceiver

The LCD is powered from a 5.0-V supply, where the output signal levels are 5.0-V TTL. A 3.3-V bus transceiver translates signal levels to match with the APEX device inputs. The direction of the bus transceiver is controlled by the read/write line of the display, so no additional control logic is required. The LCD interface requires a nominal 270 kHz clock, which is generated from a general-purpose APEX device output. Table 34 shows the LCD interface characteristics.

Table 34. LCD Interface Characteristics

Feature	I/O Pins	Voltages	Power Budget
LCD controller	11	5.0, –5.0 V	0.1 W

Table 87 on page 77 lists the LCD signal pin assignments.

LED Interface

The development board has several LEDs that tie user-defined functions and application-specific functions directly to the APEX device. Table 88 on page 77 provides more information on APEX device pins connected to LEDS.

Six LEDs are connected directly to the APEX device I/O pins. The LEDs illuminate when an I/O pin is driven low. These LEDs consist of:

- Four green LEDs (LED1, LED2, LED3, LED4)
- Two red LEDs (LED5, LED6)

LEDs are also used for specific application functions on the board, such as the configuration and ethernet interfaces. The green LEDs are also used as phase-locked loop (PLL) lock indicators. Table 35 lists the LEDs and their functions.

Table 35. Application LED Usage

LED Reference	Application	Use
D2	Conf_Done	Indicates that the APEX configuration is complete
D1	NStatus	Indicates an error in the APEX configuration
D5	LEDL	Ethernet: Link Up (normally on)
D6	LEDTX	Ethernet: TX (on during TX)
D7	LEDRX	Ethernet: RX (on During RX)
D4	LEDCOL	Ethernet: collision in half duplex mode (off in full duplex mode)
D8	LEDBTX	Ethernet: 100 BaseT connection (off for all other connection interfaces)
D9	LEDBT	Ethernet: 10 BaseT connection (off for all other connections)
D10	LEDFX	Ethernet: full duplex on (off in half duplex)

VGA Monitor Interface

The VGA monitor interface is a restricted version of VGA, and is compliant with the monitor interface used with the Altera University Program Design Laboratory Package.

The VGA monitor interface includes three-color outputs that can be turned on or off. High output on any of the R, G, or B outputs results in a 0.7-V nominal signal at the VGA connector pin. Low output results in 0-V output at the VGA connector. The output is achieved with a resistor/diode network between an APEX device I/O pin and the connector. The horizontal and vertical sync signals are connected directly from the APEX device. Table 86 on page 76 provides more information on the VGA interface. Table 36 shows the VGA monitor interface characteristics.

Table 36. VGA Monitor Interface Characteristics

Feature	I/O Pins	Clocks (MHz)	Power Budget
VGA interface	5	25.175	0

User-Defined Switches

Four momentary switches with integrated LEDs are connected to the APEX device. Pressing the switch inputs a low signal to the APEX device pin until the switch is released.

The (S1) switch is the device-wide clear input pin and is connected to DEV_CLRn on the APEX device. Another switch (S2) is connected to a low-skew dedicated input and functions as a reset input for applications where DEV_CLRn is not applicable. The remaining switches are connected to I/O pins and can be configured internally. Debouncing is provided for these signals and must be performed internally. Table 87 on page 77 provides more information on the switch interface.

User-Defined LEDs

The development board provides six user-definable LEDs driven from the APEX device that consist of two red LEDs, two yellow LEDs and two green LEDs. Table 37 lists the interface characteristics for the LED interfaces.

Table 37. LED Interface Characteristics

Feature	I/O Pins	Voltage (V)	Power Budget (W)
Two red LEDs	2	5.0	0.05
Two yellow LEDs	2	5.0	0.05
Two green LEDs	2	5.0	0.05

Test & Debugging Features

The development board includes three test features:

- The SignalTap embedded logic analyzer, which uses a JTAG interface to allow access to activity on internal nodes
- An EJTAG connector, which can be used for debugging processor cores
- Test connectors provided for debugging with a logic analyzer

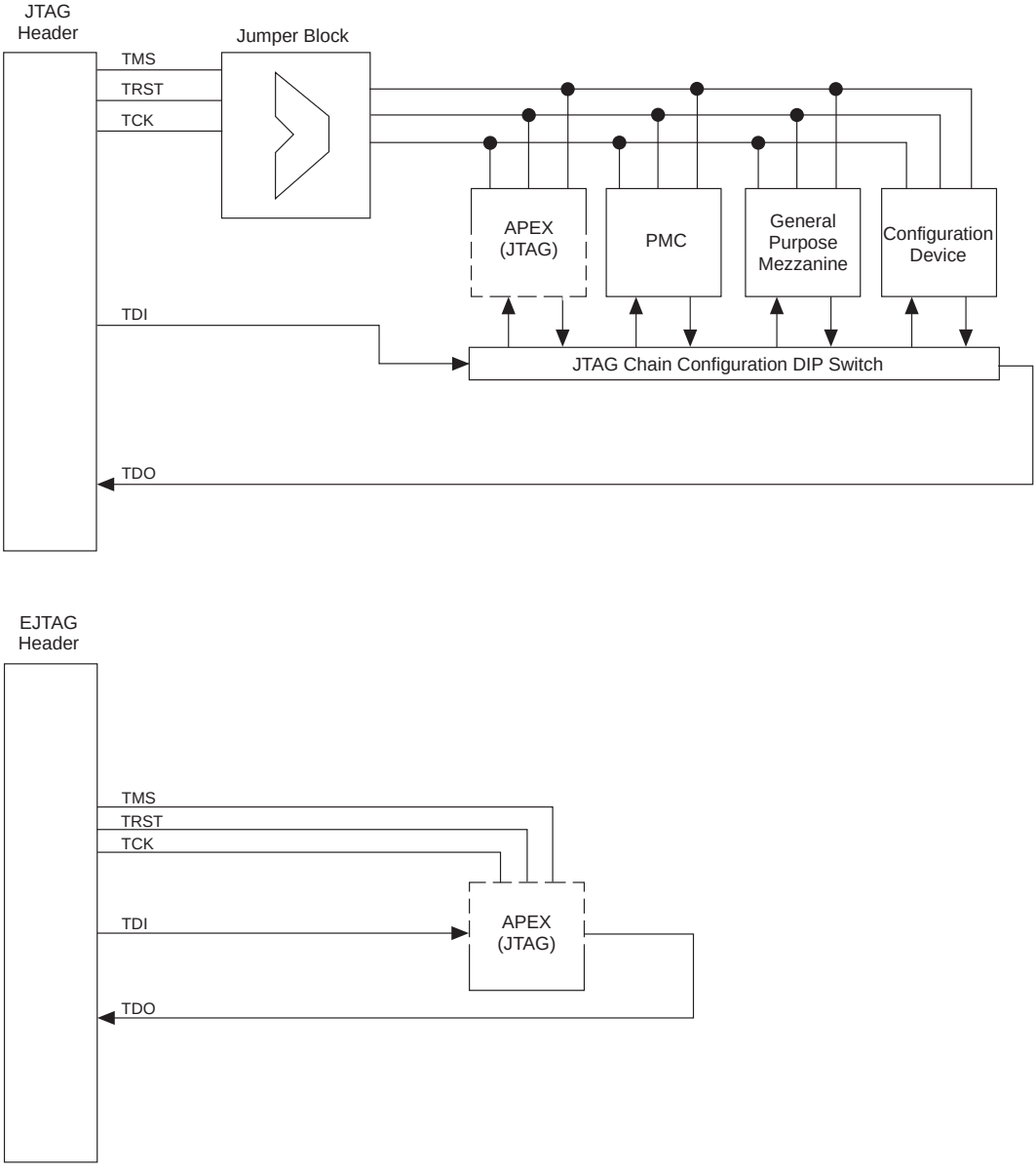
SignalTap Embedded Logic Analyzer

The development board supports in-circuit debugging with the SignalTap logic analyzer using the Quartus software and MasterBlaster communication cable.

EJTAG Interface

A 52-pin header is provided for use with an EJTAG interface for debugging a MIPS processor core in the APEX device. Although the EJTAG interface supports normal JTAG signals, it is not included as part of the programming chain. The EJTAG interface uses normal I/O pins. Before the APEX device is completely configured, these I/O pins are not available for general use because the external JTAG chain could be broken. Figure 6 shows the organization of the JTAG and EJTAG interfaces. The two interfaces are separate. The JTAG chain configuration jumpers are used to access all of the JTAG devices separately or as part of a long chain.

Figure 6. JTAG/EJTAG Configuration



Key external signals may be attached to connectors to support direct connection to external logic analyzers. External connectors are used during validation of the development board and can be removed from the final product. However, the SignalTap logic analyzer is designed to work effectively in conjunction with external logic analyzers, such as the SignalTap Plus system analyzer, supporting cross-triggering and other features. Table 80 on page 70 lists the APEX device pins used for the EJTAG interface.

Refer to the *MIPS EJTAG Debug Solution Rev 2.0* for a detailed reference on using the EJTAG interface.

Test Connectors

Six test connectors are provided on the development board. These test connectors allow for external monitoring of the high-speed memory interfaces. Refer to Table 99 on page 84 through Table 104 on page 87 for pin definitions of all of the test connectors.

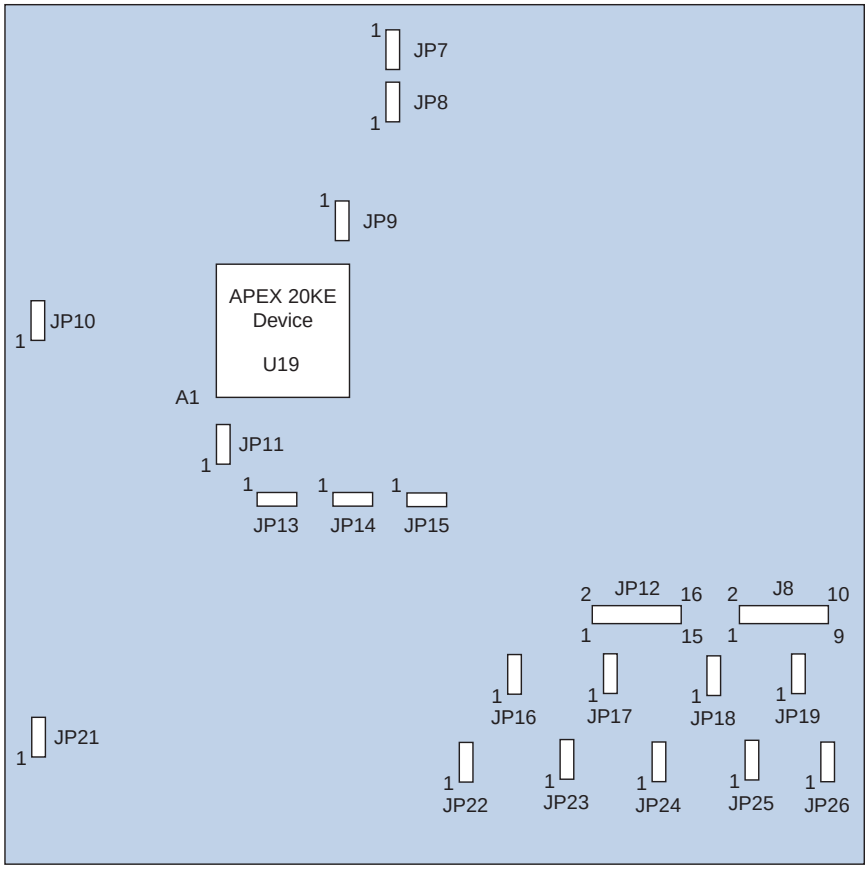
Jumper Configuration

The jumpers on the development board serve several functions:

- Clock distribution
- Enabling the PLL interface
- JTAG configuration
- Optional USB power setting
- IEEE 1284 parallel interface configuration

Figure 7 illustrates the development board jumper configuration.

Figure 7. Development Board Jumper Locations



Clock Distribution

Five inputs on the APEX device are used for clocks. Four are global clock inputs, and one is a low-skew dedicated input. Jumpers JP9 to JP14 are used to select different clock inputs. Table 38 lists all clock sources on the development board. Table 39 lists the APEX device pins used as clock inputs and the possible sources of the clock inputs for each pin. Table 40 and Figure 8 illustrate how to configure the clock selection jumpers.

Table 38. SOPC Clock Sources

Source Number	Name	Source Pin	Description
1	Memory/processor clock	U28	The 66 MHz main clock provided to all the synchronous memory and a processor core.
2	PMC clock (33MHz)	U27	33 MHz oscillator for a 33-MHz PCI core and PMC card.
3	PMC clock (66 MHz)	U6	66 MHz oscillator for a 66 MHz-PCI core and PMC card.
4	Ethernet TX clock	U29 pin 27	TX clock output from Phy.
5	Ethernet RX clock	U29 pin 24	RX clock output from Phy.
6	External source	J6	External source for the memory/processor clock.
7	VGA clock	U2	25.175 oscillator for VGA interface.
8	USB clock	U8	48 MHz oscillator for USB interface.
9	FireWire clock	U31 pin 2	FireWire SYSCLCK output from transceiver.
10	EJTAG TCK	J10 Pin 9	TCK input from EJTAG header.
11	Variable oscillator	U30	Socket provided for populating various clock frequencies.

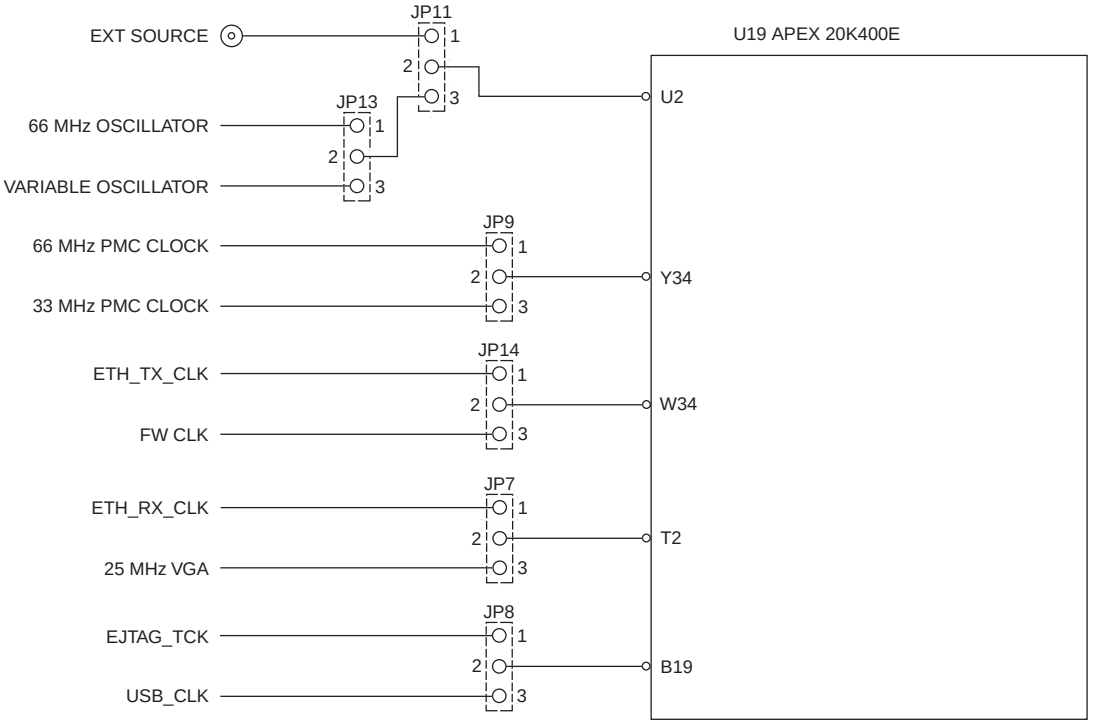
Table 39. EP20K400E Clock Input Pins and Sources

Pin	Description	Clock Inputs to Pin
U2	Global clock input	Clock source 1, 6, and 11
Y34	Global clock input	Clock source 2, and 3
W34	Global clock input	Clock source 4, and 9
T2	Global clock input	Clock source 5, and 7
B19	Low skew input	Clock source 8, and 10

Table 40. Clock Jumper Configuration

Clock Description	Header Designation	Jumper Position and Input Selected	
		1-2	2-3
PMC clock	JP9	66 MHz	33 MHz
Memory clock	JP11	External source J6	Output of JP13
VGA/ethernet RX clock	JP7	VGA 25.175 MHz	Ethernet RX
EJTAG/USB clock	JP8	EJTAG	USB 48 MHz
Mezzanine clock	JP13	66 MHz	Variable oscillator
FireWire/ethernet TX clock	JP14	Ethernet TX	FireWire clock

Figure 8. Clock Source Jumper Configuration



Jumpers JP11 and JP13 are used to select one clock input. JP11 chooses between the 66 MHz or the socketed variable oscillator. JP13 chooses between the output from JP11 and the external clock input.

The master clock input is the 66-MHz oscillator. This clock is used for all synchronous memory interfaces as well as the general-purpose mezzanine interface and the APEX device.

During development, you may need to run the interface at a slower clock rate, using either the external clock input or the variable oscillator.

The external oscillator is a BNC cable input (J6) that can be used to input a signal from a laboratory signal generator. The variable oscillator is a four-pin socket that supports a variety of 5.0-V oscillators.

The development board operates best for synchronous memory interface frequencies up to 66 MHz. You may attempt higher frequencies without risk of damaging the board; however, results may be unpredictable.

JTAG Configuration

All devices that can be programmed through the JTAG interface are connected to a 2 × 8 0.1-inch configuration header, JP12. The devices connected to the chain are programmed in the following order:

- EP20K400E device
- EPC2 configuration devices
- PMC interface
- General-purpose mezzanine interface

Table 41. JTAG Chain Configuration

Device	Bypass Jumper Setting (Pins for JP12)	Chained Jumper Settings (Pins for JP12)
APEX 20KE device	1-3	1-2 3-4
EPC2 configuration device	5-7	5-6 7-8
PMC interface	9-11	9-10 11-12
General-purpose mezzanine interface	13-15	13-14 15-16

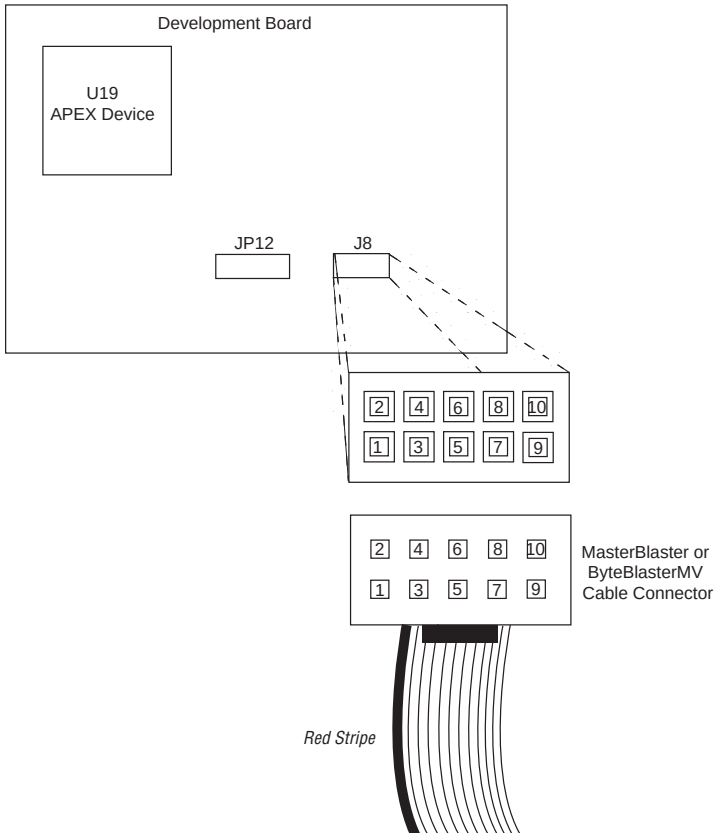
If a device is not included in the programming chain, the device must be bypassed at JP12 to prevent the the JTAG chain from being broken. For example, if the APEX device is programmed alone, shunts would be installed. Table 42 shows the JP12 configuration for APEX and EPC2 devices.

Table 42. JP12 Configuration for APEX & EPC2 Devices

APEX Device	EPC2 Device
Pins 1-2	Pins 1-3
Pins 3-4	Pins 5-6
Pins 5-7	Pins 7-8
Pins 9-11	Pins 9-11
Pins 13-15	Pins 13-15

The EPC2 device can be programmed with the MAX+PLUS II software version 9.5 or higher or the Quartus software version 2000.02 or higher using either the MasterBlaster or ByteBlasterMV communications cable. Figure 9 shows how to connect the MasterBlaster or ByteBlasterMV communication cable.

Figure 9. Connecting the MasterBlaster & ByteBlasterMV Cables



IEEE 1284 Parallel Interface

The IEEE 1284 parallel interface can be configured so that the development board can operate as a host or as a peripheral. To configure the interface to use the board as a host, jumpers JP19 to JP34 must be set to the 1-2 position. To configure the interface to use the development board as a peripheral, jumpers JP19 to JP34 must be set to the 2-3 position.

The same female connector is used when configuring the interface for host and peripheral mode. The interface does not meet the standard mechanical requirements when in peripheral mode; however, the interface meets the standard electrical requirements. A 25-pin gender adapter is required to allow a normal peripheral cable to be used with the development board.

Interface Specifications

Tables 43 through 53 list the interface specifications for the development board.

Table 43. APEX Device I/O Requirements

Interface	I/O Pins
Global reset input	1
VCCINT	40
VCCIO	24
VCCPLL	5
VCCCLK	1
GNDINT	68
GNDPLL	6
GNDCLK	1
Memory - SRAM #1	64
Memory - SRAM #1	64
Memory - EPROM, Flash & SDRAM	79
Clocks	5
Configuration	19
RS232C - DTE	7
RS232C - DCE	7
P/S2 - Keyboard	4
P/S2 - Mouse	4
USB	10
1394	14
Ethernet	18
1284	19
PMC - PCI	94
General purpose mezzanine	43
VGA	5
LCD	11
Switches - reset	1
Switches - user defined	3
LEDs - user defined	6
EJTAG	26
Unused / Test	3

Table 44. DTE UART DB9 Male Connector

Pin	Signal	Description
1	CD	Data carrier detect
2	RD	Receive data
3	TD	Transmit data
4	DTR	Data terminal ready
5	GND	Signal ground
6	DSR	Data set ready
7	RTS	Request to send
8	CTS	Clear to send
9	RI	Ring indicator

Figure 10. DTE UART DB9 Male Connector

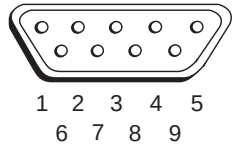


Table 45. DCE UART DB9 Female Connector

Pin	Signal	Description
1	CD	Data carrier detect
2	RD	Receive data
3	TD	Transmit data
4	DTR	Data terminal ready
5	GND	Signal ground
6	DSR	Data set ready
7	RTS	Request to send
8	CTS	Clear to send
9	VCC	Power supply (5.0 V)

Figure 11. DCE UART DB9 Female Connector

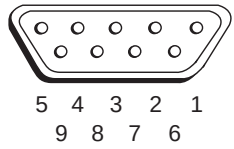


Table 46. Universal Serial Bus Male Connector

Pin	Signal	Connector Color	Description
1	VCC	Red	Cable power
2	–DATA	White	N/A
3	+DATA	Green	N/A
4	GND	Black	Cable ground

Figure 12. USB Male Connector

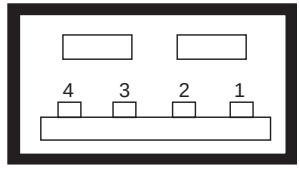


Table 47. IEEE 1394 (FireWire) Male Connector

Pin	Signal	Description
1	DATA0	Pair one data
2	DATA1	Pair one data
3	DATA2	Pair two data
4	DATA3	Pair two data
5	VCC	Power (N/C)
6	VCC	Power (N/C)

Table 48. Ethernet RJ45 Male Connector

Pin	Signal	Description
1	TX+	Transmit data +
2	TX–	Transmit data –
3	RX+	Receive data +
4	RX–	Receive data –
5	N/C	No connect
6	N/C	No connect
7	RX–	Receive data –
8	N/C	No connect

Figure 13. Ethernet RJ45 Male Connector

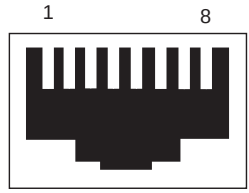


Table 49. PS/2 6-Pin Mini DIN Keyboard & Mouse Male Connector

Pin	Signal	Description
1	DATA	N/A
2	–	N/C
3	GND	Cable ground
4	VCC	Power supply (5.0 V)
5	CLOCK	Clock
6	–	N/C

Figure 14. PS/2 Keyboard & Mouse Male Connector

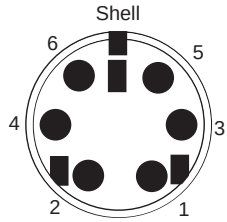


Table 50. IEEE 1284C Parallel Port DB25 Male Connector

Pin	Signal	Description	Direction
1	STB_N	Strobe	I/O
2	D0	Data bit 0	I/O
3	D1	Data bit 1	I/O
4	D2	Data bit 2	I/O
5	D3	Data bit 3	I/O
6	D4	Data bit 4	I/O
7	D5	Data bit 5	I/O
8	D6	Data bit 6	I/O
9	D7	Data bit 7	I/O
10	ACK_N	Acknowledge	I
11	BUSY	Busy	I
12	PE	Pend	I
13	SLCT	Select	I
14	AFD_N	Automatic feed	O
15	ERR_N	Error	I
16	INIT_N	Initialize	O
17	SLIN_N	Select in	O
18-25	N/A	Signal ground	N/A

Figure 15. IEEE 1284C Parallel Port DB25 Male Connector

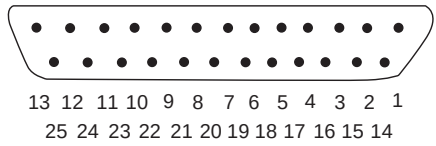


Table 51. PCI Mezzanine Card (PMC) Connector (Part 1 of 2)

Pn1/Jn1 32-Bit PCI				Pn2/Jn2 32-Bit PCI			
Pin	**Signal**	**Signal**	**Pin**	**Pin**	**Signal**	**Signal**	**Pin**
1	TCK	GND	2	1	+12 V	TRST#	2
3	GND	INTA#	4	3	TMS	TDO	4
5	INTB#	INTC#	6	5	TDI	GND	6
7	BUSMODE1#	+5 V	8	7	GND	PCI-RSVD	8
9	INTD#	PCI-RSVD	10	9	PCI-RSVD	PCI-RSVD	10
11	GND	PCI-RSVD	12	11	BUSMODE2#	+3.3 V	12
13	CLK	GND	14	13	RST#	BUSMODE3#	14
15	GND	GNT#	16	15	+3.3 V	BUSMODE4#	16
17	REQ#	+5 V	18	17	PCI-RSVD	GND	18
19	V (I/O)	AD[31]	20	19	AD[30]	AD[29]	20
21	AD[28]	AD[27]	22	21	GND	AD[26]	22
23	AD[25]	GND	24	23	AD[24]	+3.3 V	24
25	GND	C/BE[3]#	26	25	IDSEL	AD[23]	26
27	AD[22]	AD[21]	28	27	+3.3 V	AD[20]	28
29	AD[19]	+5 V	30	29	AD[18]	GND	30
31	V (I/O)	AD[17]	32	31	AD[16]	C/BE[2]#	32
33	FRAME#	GND	34	33	GND	PMC-RSVD	34
35	GND	IRDY#	36	35	TRDY#	+3.3 V	36
37	DEVSEL#	+5 V	38	37	GND	STOP#	38
39	GND	LOCK#	40	39	PERR#	GND	40
41	SDONE#	SBO#	42	41	+3.3 V	SERR#	42
43	PAR	GND	44	43	C/BE[1]#	GND	44
45	V (I/O)	AD[15]	46	45	AD[14]	AD[13]	46
47	AD[12]	AD[11]	48	47	GND	AD[10]	48
49	AD[09]	+5 V	50	49	AD[08]	+3.3 V	50
51	GND	C/BE[0]#	52	51	AD[07]	PMC-RSVD	52
53	AD[06]	AD[05]	54	53	+3.3 V	PMC-RSVD	54
55	AD[04]	GND	56	55	PMC-RSVD	GND	56

Table 51. PCI Mezzanine Card (PMC) Connector (Part 2 of 2)

Pn1/Jn1 32-Bit PCI				Pn2/Jn2 32-Bit PCI			
Pin	Signal	Signal	Pin	Pin	Signal	Signal	Pin
57	V (I/O)	AD[03]	58	57	PMC-RSVD	PMC-RSVD	58
59	AD[02]	AD[01]	60	59	GND	PMC-RSVD	60
61	AD[00]	+5 V	62	61	ACK64#	+3.3 V	62
63	GND	REQ64#	64	63	GND	PMC-RSVD	64

Table 52. PCI Mezzanine Card (PMC) Connector (Part 1 of 2)

Pn1/Jn1 32-Bit PCI				Pn2/Jn2 32-Bit PCI			
Pin	Signal	Signal	Pin	Pin	Signal	Signal	Pin
1	PCI-RSVD	GND	2	1	I/O	I/O	2
3	GND	C/BE[7]#	4	3	I/O	I/O	4
5	C/BE[6]#	C/BE[5]#	6	5	I/O	I/O	6
7	C/BE[4]#	GND	8	7	I/O	I/O	8
9	V (I/O)	PAR64	10	9	I/O	I/O	10
11	AD[63]	AD[62]	12	11	I/O	I/O	12
13	AD[61]	GND	14	13	I/O	I/O	14
15	GND	AD[60]	16	15	I/O	I/O	16
17	AD[59]	AD[58]	18	17	I/O	I/O	18
19	AD[57]	GND	20	19	I/O	I/O	20
21	V (I/O)	AD[56]	22	21	I/O	I/O	22
23	AD[55]	AD[54]	24	23	I/O	I/O	24
25	AD[3]	GND	26	25	I/O	I/O	26
27	GND	AD[52]	28	27	I/O	I/O	28
29	AD[51]	AD[50]	30	29	I/O	I/O	30
31	AD[49]	GND	32	31	I/O	I/O	32
33	GND	AD[48]	34	33	I/O	I/O	34
35	AD[47]	AD[46]	36	35	I/O	I/O	36
37	AD[45]	GND	38	37	I/O	I/O	38
39	V (I/O)	AD[44]	40	39	I/O	I/O	40
41	AD[43]	AD[42]	42	41	I/O	I/O	42
43	AD[41]	GND	44	43	I/O	I/O	44
45	GND	AD[40]	46	45	I/O	I/O	46
47	AD[39]	AD[38]	48	47	I/O	I/O	48
49	AD[37]	GND	50	49	I/O	I/O	50
51	GND	AD[36]	52	51	I/O	I/O	52

Table 52. PCI Mezzanine Card (PMC) Connector (Part 2 of 2)

Pn1/Jn1 32-Bit PCI				Pn2/Jn2 32-Bit PCI			
Pin	Signal	Signal	Pin	Pin	Signal	Signal	Pin
53	AD[35]	AD[34]	54	53	I/O	I/O	54
55	AD[33]	GND	56	55	I/O	I/O	56
57	V (I/O)	AD[32]	58	57	I/O	I/O	58
59	PCI-RSVD	PCI-RSVD	60	59	I/O	I/O	60
61	PCI-RSVD	GND	62	61	I/O	I/O	62
63	GND	PCI-RSVD	64	63	I/O	I/O	64

General Purpose Mezzanine Connectors

The general-purpose mezzanine interface uses two 64-pin connectors, which are the same connectors used for the PCI mezzanine connectors. The specific pinout is currently undefined. Table 53 lists proposed allocations.

Table 53. General-Purpose Mezzanine Connectors

Signal Type	Number of Pins
APEX device I/O	50
Clock	1
Reset (Connected to the development board RESET switch)	1
JTAG	5
+5.0 V	20
+3.3 V	20
+/– 12 V	2
GND	29

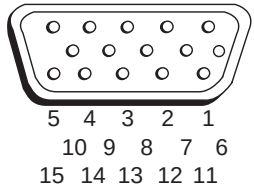
Analog I/O Interface

Table 54 shows the DB15 Mini-DIN Monitor (VGA) male connector.

Table 54. DB15 Mini-DIN Monitor (VGA) Male Connector

Pin	Signal	Description	Direction
1	RED	Red video	O
2	GREEN	Green video	O
3	BLUE	Blue video	O
4	N/C	N/A	N/A
5	GND	N/A	N/A
6	GND	N/A	N/A
7	GND	Signal ground	N/A
8	GND	Signal ground	N/A
9	N/C	No connection	N/A
10	GND	Signal ground	N/A
11	N/C	No connection	N/A
12	N/C	Reserved	N/A
13	HSYNC	Horizontal synchronization	O
14	VSYNC	Vertical synchronization	O
15	N/C	No connection	N/A

Figure 16. DB15 Mini-DIN Monitor Connector



Power Conditioning Interface

You can connect power can be connected to the development board using either an 8-pin DIN connector from International Power Supply Inc. (HES100-30) or a 4-pin terminal block supporting a laboratory bench supply. The signals connected are +5.0 V, ground, +12.0 V and –12.0 V.

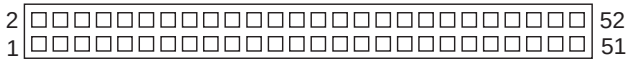
EJTAG Interface

Table 55 lists the EJTAG interface connections.

Table 55. EJTAG Interface

Pin	Signal	Description	Direction
1	TRST (optional)	Test reset input	I
3	TDI/DINT	Test data input/debug interrupt	I
5	TDO/TPC	Test data output/target PC output	O
7	TMS	Test mode select input	I
9	TCK	Test clock input	I
11	RST	Reset input	I
13	PCST[0]	PC trace status information bit 0	O
15	PCST[1]	PC trace status information bit 1	O
17	PCST[2]	PC trace status information bit 2	O
19	DCLK	Processor clock/N (N = 1, 2, 3, or 4)	O
21	TPC[2]	Target PC output bit 2	O
23	PCST2[0]	PC trace status information bit 0 (N = 2)	O
25	PCST2[1]	PC trace status information bit 1 (N = 2)	O
27	PCST2[2]	PC trace status information bit 2 (N = 2)	O
29	TPC[3]	Target PC output bit 3	O
31	PCST3[0]	PC trace status information bit 0 (N = 3)	O
33	PCST3[1]	PC trace status information bit 1 (N = 3)	O
35	PCST3[2]	PC trace status information bit 2 (N = 3)	O
37	TPC[4]	Target PC output bit 4	O
39	PCST4[0]	PC trace status information bit 0 (N = 4)	O
41	PCST4[1]	PC trace status information bit 1 (N = 4)	O
43	PCST4[2]	PC trace status information bit 2 (N = 4)	O
45	TPC[5]	Target PC output bit 5	O
47	TPC[6]	Target PC output bit 6	O
49	TPC[7]	Target PC output bit 7	O
51	TPC[8]	Target PC output bit 8	O
even	GND	Ground	N/A

Figure 17. EJTAG Interface



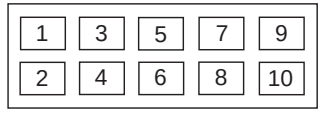
Configuration Interface

Table 56 shows the MasterBlaster female connector pin assignments.

Table 56. MasterBlaster Female Connector

Pin	JTAG Mode	
	Signal	Description
1	TCK	Clock signal
2	GND	Signal ground
3	TDO	Data from device
4	VCC	Power supply
5	TMS	JTAG state machine control
6	VIO	Reference voltage for MasterBlaster output driver
7	–	No connection
8	–	No connection
9	TDI	Data to device
10	GND	Signal ground

Figure 18. MasterBlaster Female Connector



Memory Interface

Table 57 lists the pin assignments for the SDRAM socket.

Table 57. SDRAM Socket Pin Assignments (Part 1 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	/S2	87	DQ33	129	/S3
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	Vdd	48	NC	90	Vdd	132	A13
7	DQ4	49	Vdd	91	DQ36	133	Vdd
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vdd	101	DQ45	143	Vdd
18	Vdd	60	DQ20	102	Vdd	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	CKE1	105	CB4	147	NC
22	CB1	64	Vss	106	CB5	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vdd	68	Vss	110	Vdd	152	Vss
27	/WE0	69	DQ24	111	/CAS	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	/S0	72	DQ27	114	/S1	156	DQ59
31	NC	73	Vdd	115	/RAS	157	Vdd
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61

Table 57. SDRAM Socket Pin Assignments (Part 2 of 2)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	CK2	121	A9	163	CK3
38	A10 (AP)	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	Vdd	82	SDA	124	Vdd	166	SA1
41	Vdd	83	SCL	125	CK1	167	SA2
42	CK0	84	Vdd	126	A12	168	Vdd

Table 58. SDRAM Sockets

Signal	Description	Signal	Description
A0 - A12	Multiplexed address input	/WE	Write enable
BA0 - BA1	Select bank	DQM0 - DQM7	DQM
DQ0 - DQ64	Data input/output	VCC	Power supply = 3.3 V
CLK0	Clock input	SDA	Serial data I/O
CKE0	Clock enable input	SCL	Serial clock
/SO	Chip select input	N/C	No connection
/RAS	Row address strobe	GND	Ground
/CAS	Column address strobe	–	–

APEX Pin Assignments

The main component of the development board is the EP20K400E device. The pins on the APEX device are assigned to functions on the board. When generating IP cores for the APEX device, the pins must be used as defined to avoid damaging the device. The following sections list the interfaces and dedicated pins on the board. Any pins not used for a design should be left in the high-impedance (input) state to avoid contention.

Configuration

The APEX device pins listed in Table 59 are used exclusively for configuring the device. Refer to the *Getting Started* section for more information about configuring the APEX device.

Table 59. EP20K400E Configuration Pins

Signal Name	APEX Pin	Description
MSEL0	U35	Configuration mode select (tied to GND)
MSEL1	W35	Configuration mode select (tied to GND)
NSTATUS	AN17	OE for EPC2s
NCONFIG	W32	INIT for EPC2s
DCLK	U3	Data clock for EPC2s
CONF_DONE	AM17	CS for EPC2s
nCE	U1	Not connected
DATA0	U4	Serial input for EPC2 configuration data
TDI	W1	JTAG data in
TDO	C17	JTAG data out (to next device in the chain)
TCK	AN19	JTAG clock
TMS	AM19	JTAG mode select
TRST	D19	JTAG reset (pulled high)
DEV_CLRn	T6	Global reset for the device

General-Purpose Memory Interface

The general-purpose memory bus has shared addresses and data with the SDRAM, Flash, and configuration devices. Each type of memory has separate control lines.

General-Purpose Memory Data Bus

The SDRAM module is 64-bits wide, and the general-purpose memory data bus is 32-bits wide. To allow access to the entire SDRAM memory array, data bus pins are doubled. This means that the upper half of the data bus is connected to the lower half. For example, GPM_D(0) is connected to data pin 0 and data pin 32 on the SDRAM DIMM. Ensure that only 32 bits of the SDRAM data bus are enabled at a time (D[31..0] or D[63..32]) to avoid contention. Table 60 lists the general-purpose memory data pus pin assignments.

Table 60. General-Purpose Memory Data Bus Pin Assignments

Signal Name	APEX Pin	Signal Name	APEX Pin
GPM_D(0)	AP16	GPM_D(16)	AR10
GPM_D(1)	AP20	GPM_D(17)	AR11
GPM_D(2)	AP21	GPM_D(18)	AR12
GPM_D(3)	AP22	GPM_D(19)	AR13
GPM_D(4)	AP23	GPM_D(20)	AR14
GPM_D(5)	AP24	GPM_D(21)	AR15
GPM_D(6)	AP25	GPM_D(22)	AR16
GPM_D(7)	AP26	GPM_D(23)	AR20
GPM_D(8)	AR2	GPM_D(24)	AR21
GPM_D(9)	AR3	GPM_D(25)	AR22
GPM_D(10)	AR4	GPM_D(26)	AR23
GPM_D(11)	AR5	GPM_D(27)	AR24
GPM_D(12)	AR6	GPM_D(28)	AR25
GPM_D(13)	AR7	GPM_D(29)	AR26
GPM_D(14)	AR8	GPM_D(30)	AR27
GPM_D(15)	AR9	GPM_D(31)	AR28

General-Purpose Memory Address Bus

The general-purpose memory address bus is also shared; however, all 20 pins are not required for each memory device. The address lines on the Flash and configuration device are isolated from the SDRAM by bus transceivers. These devices are always enabled, so additional control is not required. The delay on the address lines needs to be included for timing analysis. The SA[2..0] lines on the SDRAM module are used as the serial configuration address lines, so the exact module configuration may be read by the memory controller. Table 61 lists the general-purpose memory address bus pin assignments.

Table 61. General-Purpose Memory Address Bus Pin Assignments

Signal Name	APEX Pin	Connected to		
		DRAM / Name	Flash	EPROM
GPM_A(0)	AN16	A0	DQ15/A-1	A0
GPM_A(1)	AN20	A1	A0	A1
GPM_A(2)	AN21	A2	A1	A2
GPM_A(3)	AN22	A3	A2	A3
GPM_A(4)	AN23	A4	A3	A4
GPM_A(5)	AN24	A5	A4	A5
GPM_A(6)	AN25	A6	A5	A6
GPM_A(7)	AP3	A7	A6	A7
GPM_A(8)	AP4	A8	A7	A8
GPM_A(9)	AP5	A9	A8	A9
GPM_A(10)	AP6	A10	A9	A10
GPM_A(11)	AP7	A11	A10	A11
GPM_A(12)	AP8	BA1	A11	A12
GPM_A(13)	AP9	BA0	A12	A14
GPM_A(14)	AP10	NC	A13	A14
GPM_A(15)	AP11	NC	A14	A15
GPM_A(16)	AP12	NC	A15	NC
GPM_A(17)	AP13	SA0	A16	NC
GPM_A(18)	AP14	SA1	A17	NC
GPM_A(19)	AP15	SA2	A18	NC

SDRAM Control Lines

The SDRAM_DQM[7:0] lines are used to enable the SDRAM outputs. Because the data bus pins are doubled-up on the SDRAM DIMM, both halves of the data bus may not be enabled at the same time. For example, if SDRAM_DQM[0] is enabled, SDRAM_DQM(4) cannot be enabled or contention will occur. Tables 62 through 71 show the pin-outs.

Table 62. SDRAM Control Signal Pin Assignments

Signal Name	APEX Pin	Description
SDRAM_RAS	AD1	Row address strobe
SDRAM_CAS	AD2	Column address strobe
SDRAM_WE#	AC1	Write enable
SDRAM_CS1	AC2	Chip select
SDRAM_CS2	AF5	Chip select
SDRAM_CKE	AC4	Clock enable
SDRAM_SDA	AC5	Serial EPROM data output
SDRAM_SCL	N31	Serial EPROM clock input
SDRAM_DQM(0)	AA1	Data bus enable (D0-7)
SDRAM_DQM(1)	AA2	Data bus enable (D8-15)
SDRAM_DQM(2)	AA3	Data bus enable (D16-23)
SDRAM_DQM(3)	AA5	Data bus enable (D24-31)
SDRAM_DQM(4)	AA6	Data bus enable (D32-39)
SDRAM_DQM(5)	AA32	Data bus enable (D40-47)
SDRAM_DQM(6)	AB1	Data bus enable (D48-55)
SDRAM_DQM(7)	AB2	Data bus enable (D56-63)
SDRAM_RAS	AD1	Row address strobe
SDRAM_CAS	AD2	Column address strobe
SDRAM_WE#	AC1	Write enable
SDRAM_CS1	AC2	Chip select

Table 63. EPROM Memory Control Signal Pin Assignments

Signal	APEX Pin	Description
EPROM_CE(0)	AN8	Chip enable
EPROM_CE(1)	AN9	Chip enable
EPROM_OE	AD3	Output enable

Table 64. Flash Memory Control Signal Pin Assignments

Signal Name	APEX Pin	Description
FLASH_WE(0)	AN12	Write enable (D0-7)
FLASH_WE(1)	AN13	Write enable (D8-15)
FLASH_WE(2)	AN14	Write enable (D16-23)
FLASH_WE(3)	AN15	Write enable (D24-31)
FLASH_CS	AJ1	Chip select
FLASH_OE	AJ2	Output enable
FLASH_RP	AJ3	Reset/power down
FLASH_WP	AJ4	Write protect

Table 65. SSRAM Bank 1 Data Bus Pin Assignments

Signal Name	APEX Pin	Signal Name	APEX Pin
SSRAM1_Data(0)	B13	SSRAM1_Data(16)	B32
SSRAM1_Data(1)	B14	SSRAM1_Data(17)	B33
SSRAM1_Data(2)	B15	SSRAM1_Data(18)	C1
SSRAM1_Data(3)	B16	SSRAM1_Data(19)	C5
SSRAM1_Data(4)	B20	SSRAM1_Data(20)	C6
SSRAM1_Data(5)	B21	SSRAM1_Data(21)	C7
SSRAM1_Data(6)	B22	SSRAM1_Data(22)	C8
SSRAM1_Data(7)	B23	SSRAM1_Data(23)	C9
SSRAM1_Data(8)	B24	SSRAM1_Data(24)	C10
SSRAM1_Data(9)	B25	SSRAM1_Data(25)	C11
SSRAM1_Data(10)	B26	SSRAM1_Data(26)	C12
SSRAM1_Data(11)	B27	SSRAM1_Data(27)	C14
SSRAM1_Data(12)	B28	SSRAM1_Data(28)	C20
SSRAM1_Data(13)	B29	SSRAM1_Data(29)	C21
SSRAM1_Data(14)	B30	SSRAM1_Data(30)	C22
SSRAM1_Data(15)	B31	SSRAM1_Data(31)	C23

Table 66. SSRAM Bank 1 Address Bus Pin Assignments

Signal Name	APEX Pin	Signal Name	Apex Pin
SSRAM1_A(0)	A2	SSRAM1_A(9)	A12
SSRAM1_A(1)	A3	SSRAM1_A(10)	A13
SSRAM1_A(2)	A4	SSRAM1_A(11)	A15
SSRAM1_A(3)	A5	SSRAM1_A(12)	A16
SSRAM1_A(4)	A6	SSRAM1_A(13)	A20
SSRAM1_A(5)	A7	SSRAM1_A(14)	A21
SSRAM1_A(6)	A9	SSRAM1_A(15)	A22
SSRAM1_A(7)	A10	SSRAM1_A(16)	A23
SSRAM1_A(8)	A11	SSRAM1_A(17)	A24

Table 67. SSRAM Bank 1 Control Signal Pin Assignments

Signal Name	APEX Pin	Direction	Description
SSRAM1_BW(0)	C24	Output	Byte enable (D0-7)
SSRAM1_BW(1)	C25	Output	Byte enable (D8-15)
SSRAM1_BW(2)	C26	Output	Byte enable (B16-23)
SSRAM1_BW(3)	C27	Output	Byte enable (D24-31)
SSRAM1_ADV	D1	Output	Address advance
SSRAM1_ADSP	D6	Output	Address status processor
SSRAM1_ADSC	D7	Output	Address status controller
SSRAM1_OE	D8	Output	Output enable
SSRAM1_BWE	E35	Output	Byte write enable
SSRAM1_GW	E34	Output	Global write
SSRAM1_CE2	E28	Output	Chip select
SSRAM1_CE	E27	Output	Chip select
SSRAM1_MODE	E26	Output	Mode (select burst seq.)
SSRAM1_ZZ	E25	Output	Power down

Table 68. SSRAM Bank 2 Data Bus Pin Assignments

Signal Name	APEX Pin	Signal Name	Apex Pin
SSRAM2_Data(0)	D9	SSRAM2_Data(16)	D30
SSRAM2_Data(1)	D10	SSRAM1_Data(17)	D35
SSRAM2_Data(2)	D11	SSRAM2_Data(18)	E1
SSRAM2_Data(3)	D13	SSRAM2_Data(19)	E2
SSRAM2_Data(4)	D14	SSRAM2_Data(20)	E8
SSRAM2_Data(5)	D15	SSRAM2_Data(21)	E9
SSRAM2_Data(6)	D16	SSRAM2_Data(22)	E10
SSRAM2_Data(7)	D20	SSRAM2_Data(23)	E11
SSRAM2_Data(8)	D21	SSRAM2_Data(24)	E13
SSRAM2_Data(9)	D22	SSRAM2_Data(25)	E14
SSRAM2_Data(10)	D23	SSRAM2_Data(26)	E15
SSRAM2_Data(11)	D25	SSRAM2_Data(27)	E16
SSRAM2_Data(12)	D26	SSRAM2_Data(28)	E20
SSRAM2_Data(13)	D27	SSRAM2_Data(29)	E21
SSRAM2_Data(14)	D28	SSRAM2_Data(30)	E22
SSRAM2_Data(15)	D29	SSRAM1_Data(31)	E23

Table 69. SSRAM Bank 2 Address Bus Pin Assignments

Signal Name	APEX Pin	Signal Name	APEX Pin
SSRAM2_A(0)	A25	SSRAM2_A(9)	A34
SSRAM2_A(1)	A26	SSRAM2_A(10)	B3
SSRAM2_A(2)	A27	SSRAM2_A(11)	B4
SSRAM2_A(3)	A28	SSRAM2_A(12)	B6
SSRAM2_A(4)	A29	SSRAM2_A(13)	B8
SSRAM2_A(5)	A30	SSRAM2_A(14)	B9
SSRAM2_A(6)	A31	SSRAM2_A(15)	B10
SSRAM2_A(7)	A32	SSRAM2_A(16)	B11
SSRAM2_A(8)	A33	SSRAM2_A(17)	B12

Table 70. SSRAM Bank 2 Control Signal Pin Assignments

Signal Name	APEX Pin	Direction	Description
SSRAM2_BW(0)	C28	Output	Byte enable (D0-7)
SSRAM2_BW(1)	C29	Output	Byte enable (D8-15)
SSRAM2_BW(2)	C30	Output	Byte enable (B16-23)
SSRAM2_BW(3)	C31	Output	Byte enable (D24-31)
SSRAM2_ADV	G3	Output	Address advance
SSRAM2_ADSP	G2	Output	Address status processor
SSRAM2_ADSC	G1	Output	Address status controller
SSRAM2_OE	F34	Output	Output enable
SSRAM2_BWE	F1	Output	Byte write enable
SSRAM2_GW	F2	Output	Global write
SSRAM2_CE2	F5	Output	Chip enable
SSRAM2_CE	F6	Output	Chip select
SSRAM2_MODE	F32	Output	Mode (select burst seq.)
SSRAM2_ZZ	F33	Output	Power down

Table 71. RS-232 DTE Pin Assignments

Signal Name	APEX Pin	Direction	Description
DT_DTR	AG3	Output	Data terminal ready
DT_TD	AF34	Output	Transmit data
DT_RTS	AG2	Output	Request to send
DT_DCD	AE5	Input	Carrier detect
DT_DSR	AE6	Input	Data set ready
DT_RD	AE34	Input	Receive data
DT_CTS	AF1	Input	Clear to send

Figure 19 illustrates the DTE UART interface configuration.

Figure 19. DTE UART Interface

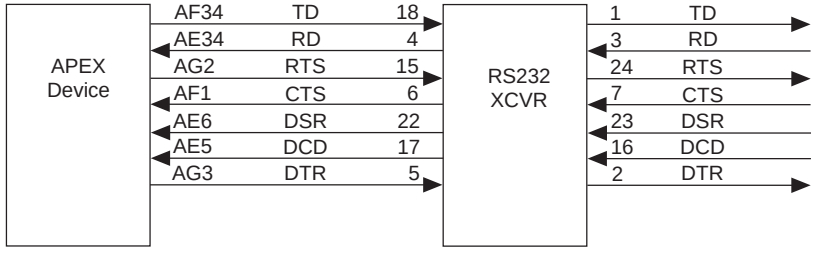


Table 72 and Figure 20 show the pin assignments and inteface diagram for the DCE UART interface.

Table 72. RS-232 DCE Pin Assignments

Signal Name	APEX Pin	Direction	Description
DC_DTR	AF4	Input	Data terminal ready
DC_TD	AF2	Input	Transmit data
DC_RTS	AF3	Input	Request to send
DC_DCD	AG6	Output	Carrier detect
DC_DSR	AG30	Output	Data set ready
DC_RD	AG35	Output	Receive data
DC_CTS	AC33	Output	Clear to send
DC_DTR	AF4	Input	Data terminal ready

Figure 20. DCE UART Interface

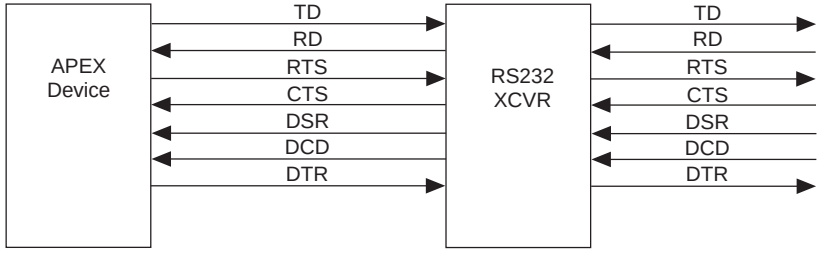


Table 73 and Figure 21 show the pin assignments and interface diagram for the keyboard and mouse interface.

Table 73. PS/2 Keyboard Pin Assignments

Signal Name	APEX Pin	Direction	Description
K_DATA_OUT	B5	Output	Output data
K_DATA_IN	G31	Input	Input data
K_CLK_OUT	B7	Output	Output data clock
K_CLK_IN	G6	Input	Input data clock

Figure 21. Keyboard & Mouse Interface

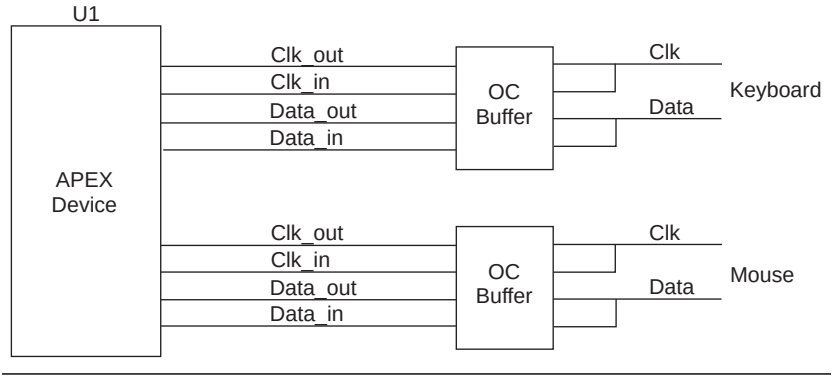


Table 74. PS/2 Mouse Pin Assignments

Signal Name	APEX Pin	Direction	Description
M_DATA_OUT	E7	Output	Output data
M_DATA_IN	G5	Input	Input data
M_CLK_OUT	G32	Output	Output data clock
M_CLK_IN	G4	Input	Input data clock

Table 75. USB Pin Assignments

Signal Name	APEX Pin	Direction	Description
USB_OE	J4	Output	USB transceiver enable
USB_SUSPND	J5	Output	Suspend (low power mode)
USB_SPEED	J6	Output	Edge Rate Speed Control
USB_VPO	P5	Output	Output Data from SIE
USB_VMO	P6	Output	Output Data from SIE
USB_RCV	G33	Input	Receive Data input to SIE
USB_VP	H6	Input	Gated Version of D+
USB_VM	J1	Input	Gated Version of D-
USB_RERR	J2	Input	Receive Error
USB_RSEO	J3	Input	Receive Single Ended Zero

Figure 22 illustrates the USB interface.

Figure 22. USB Interface

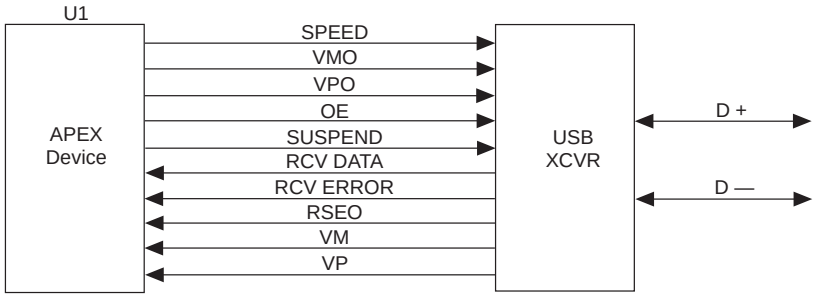


Table 76. IEEE-1394 FireWire Interface Pin Assignments

Signal Name	APEX Pin	Direction	Description
FW_DATA(0)	AJ6	Input/Output	Fire Wire Data (0)
FW_DATA(1)	AK1	Input/Output	Fire Wire Data (1)
FW_DATA(2)	AK3	Input/Output	Fire Wire Data (2)
FW_DATA(3)	AK4	Input/Output	Fire Wire Data (3)
FW_DATA(4)	AK5	Input/Output	Fire Wire Data (4)
FW_DATA(5)	AL1	Input/Output	Fire Wire Data (5)
FW_DATA(6)	AL9	Input/Output	Fire Wire Data (6)
FW_DATA(7)	AL10	Input/Output	Fire Wire Data (7)
FW_RESET	AF6	Output	Reset
FW_LREQ	AK2	Input	Link Request (to LLC)
FW_PD	AL11	Output	Power Down
FW_CTL0	AL13	Output	Control 0
FW_CTL1	AL14	Output	Control 1
FW_CNA	AL15	Output	Cable Not Active output
FW_LKON	AL7	Input	Link On (Connected)

Figure 23 illustrates the IEEE 1394 FireWire interface.

Figure 23. IEEE 1394 FireWire Interface

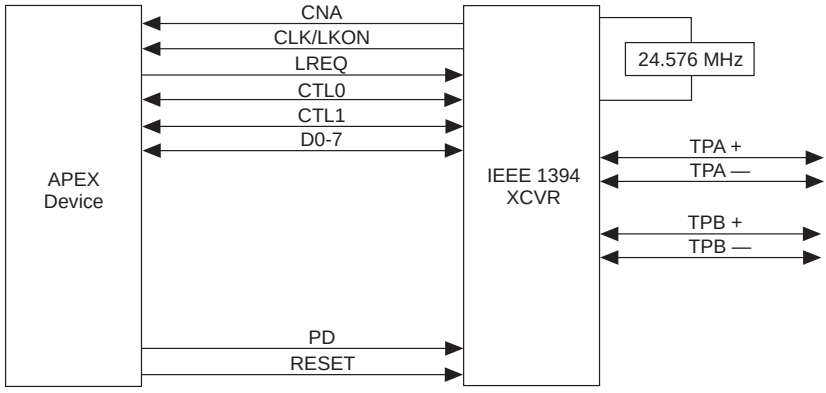


Table 77. Ethernet Interface Pin Assignments

Signal Name	APEX Pin	Direction	Description
ETH_TXD(0)	J30	Output	Transmit Data (0)
ETH_TXD(1)	J31	Output	Transmit Data (1)
ETH_TXD(2)	J32	Output	Transmit Data (2)
ETH_TXD(3)	J33	Output	Transmit Data (3)
ETH_TX_EN	J35	Output	Transmit Enable
ETH_TX_ER	J34	Output	Transmit Error
ETH_MDC	M6	Output	Management Data Clock
ETH_GLOB_RES	A8	Output	Reset
ETH_RX_DV	AH6	Input	Receive Data Valid
ETH_RX_ER	AJ5	Input	Receive Error
ETH_RXD(0)	AH1	Input	Receive Data
ETH_RXD(1)	AH2	Input	Receive Data
ETH_RXD(2)	AH3	Input	Receive Data
ETH_RXD(3)	AH5	Input	Receive Data
ETH_MDIO	AK6	Input/Output	Management Data I/O
ETH_COL	Y31	Input	Collision
ETH_INTR	AK35	Input	Interrupt
ETH_CRS	R1	Input	Carrier Sense

Figure 24 illustrates the ethernet interface.

Figure 24. Ethernet Interface

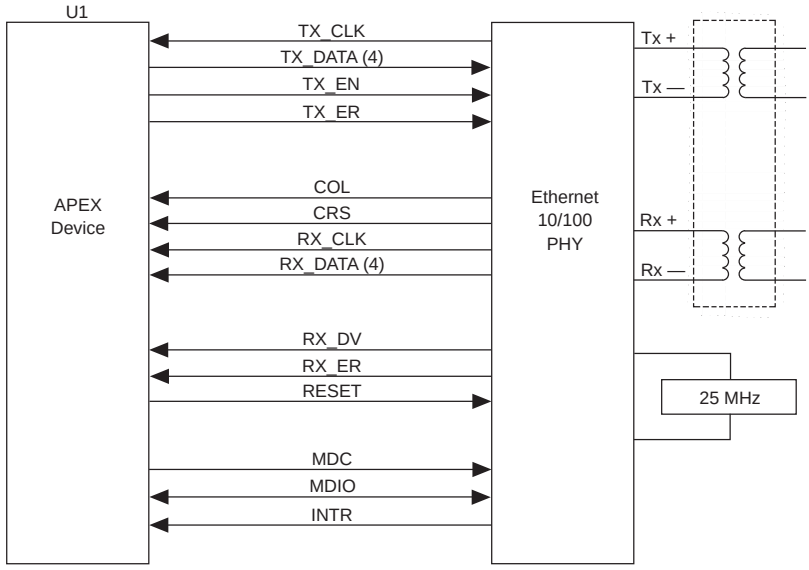


Table 78. Parallel Port Interface in Host Mode (Part 1 of 2)

Signal Name	APEX Pin	Direction	Description
PP_D(0)	AM1	Input/Output	Bi-directional Data line
PP_D(1)	AM6	Input/Output	Bi-directional Data line
PP_D(2)	AM7	Input/Output	Bi-directional Data line
PP_D(3)	AM8	Input/Output	Bi-directional Data line
PP_D(4)	AM9	Input/Output	Bi-directional Data line
PP_D(5)	AM10	Input/Output	Bi-directional Data line
PP_D(6)	AM11	Input/Output	Bi-directional Data line
PP_D(7)	AM13	Input/Output	Bi-directional Data line
PP_SLCTIN_N	AL16	Output	Deselect Protocol
PP_INT_N	AL20	Output	Initialize Printer
PP_AFEED_N	AL21	Output	Auto Feed
PP_STROBE_N	AL22	Output	Data Strobe
PP_HD	AL23	Output	HD Enable
PP_DIR	AL27	Output	Control Direction of Data
PP_ACK_N	AM14	Input	Finished with last char
PP_BUSY	AM15	Input	Not Ready

Table 78. Parallel Port Interface in Host Mode (Part 2 of 2)			
Signal Name	**APEX Pin**	**Direction**	**Description**
PP_PEND	AM16	Input	Paper end
PP_SLCT	AM20	Input	Select
PP_ERR_N	AM21	Input	Error (cannot print)

Figure 25 illustrates the parallel port interface in host mode.

Figure 25. Parallel Port Interface in Host Mode

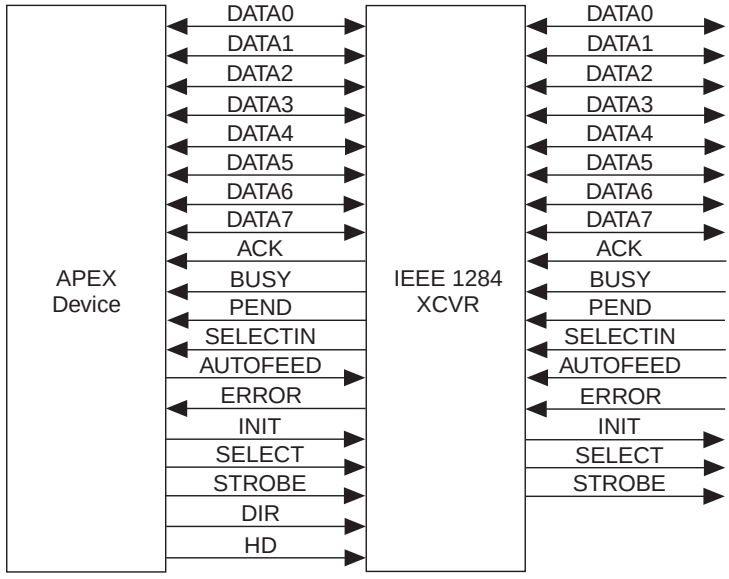


Table 79. Parallel Port Interface in Peripheral Mode

Signal Name	APEX Pin	Direction	Description
PP_D(0)	AM1	Input/Output	Bidirectional data line
PP_D(1)	AM6	Input/Output	Bidirectional data line
PP_D(2)	AM7	Input/Output	Bidirectional data line
PP_D(3)	AM8	Input/Output	Bidirectional data line
PP_D(4)	AM9	Input/Output	Bidirectional data line
PP_D(5)	AM10	Input/Output	Bidirectional data line
PP_D(6)	AM11	Input/Output	Bidirectional data line
PP_D(7)	AM13	Input/Output	Bidirectional data line
PP_BUSY	AL16	Output	Not ready
PP_ACK_N	AL20	Output	Ready for next character
PP_ERR_N	AL21	Output	Error (cannot print)
PP_PEND	AL22	Output	Paper end
PP_HD	AL23	Output	HD enable
PP_DIR	AL27	Output	Control direction of data
PP_INIT_N	AM14	Input	Initialize printer
PP_SLCTIN_N	AM15	Input	Deselect protocol
PP_STROB	AM16	Input	Data strobe
PP_SLCT	AM20	Input	Select
PP_AFEED	AM21	Input	Auto feed

Table 80. EJTAG Interface Pin Assignments (Part 1 of 2)

Signal Name	APEX Pin	Direction
EJTAG_TRST	AB3	Input/Output
EJTAG_TDI	AB4	Input/Output
EJTAG_TDO	C13	Input/Output
EJTAG_TMS	AB5	Input/Output
EJTAG_TCK	AB32	Input/Output
EJTAG_RST	AD4	Input/Output
EJTAG_PCST[0]	AD5	Input/Output
EJTAG_PCST[1]	AD6	Input/Output
EJTAG_PCST[2]	AD33	Input/Output
EJTAG_DCLK	AE1	Input/Output
EJTAG_PCST2[0]	AE4	Input/Output
EJTAG_TPC2	AE3	Input/Output
EJTAG_PCST2[1]	N32	Input/Output

Table 80. EJTAG Interface Pin Assignments (Part 2 of 2)

Signal Name	APEX Pin	Direction
EJTAG_PCST2[2]	N33	Input/Output
EJTAG_TPC3	R6	Input/Output
EJTAG_PCST3[0]	T1	Input/Output
EJTAG_PCST3[1]	N34	Input/Output
EJTAG_PCST3[2]	T3	Input/Output
EJTAG_TPC4	P31	Input/Output
EJTAG_PCST4[0]	T5	Input/Output
EJTAG_PCST4[1]	W5	Input/Output
EJTAG_PCST4[2]	P30	Input/Output
EJTAG_TPC5	P33	Input/Output
EJTAG_TPC6	P34	Input/Output
EJTAG_TPC7	Y4	Input/Output
EJTAG_TPC8	Y6	Input/Output

PMC Interface

Tables 81 through 83 provide pin definitions for the three PMC interface connectors. The PMC connector pins are allocated as specified in the PMC specification and the PMC mezzanine sections on page 29.

Table 81. PMC Interface JN1 Pin Assignments

Signal Name	APEX Pin	PMC Pin
PMC_INTA#	T35	JN1-4
PMC_INTB#	H2	JN1-5
PMC_INTC#	H3	JN1-6
PMC_INTD#	H4	JN1-9
PMC_GNT#	AM29	JN1-16
PMC_REQ#	AL29	JN1-17
AD(31)	AR31	JN1-20
AD(28)	AR32	JN1-21
AD(27)	AP32	JN1-22
AD(25)	AP33	JN1-23
PMC_C_BE(3)	AM25	JN1-26
AD(22)	AL33	JN1-27
AD(21)	AL35	JN1-28
AD(19)	AK31	JN1-29
AD(17)	AK34	JN1-32
PMC_FRAME#	AM27	JN1-33
PMC_IRDY#	AP17	JN1-36
PMC_DEVSEL#	AN29	JN1-37
PMC_LOCK#	L1	JN1-40
PMC_SDONE	AJ33	JN1-41
PMC_SBO	AL8	JN1-42
PMC_PAR	AR30	JN1-43
AD(15)	AJ31	JN1-46
AD(12)	AJ35	JN1-47
AD(11)	AH30	JN1-48
AD(9)	AH33	JN1-49
PMC_C_BE(0)	AM26	JN1-52
AD(6)	AG32	JN1-53
AD(5)	AG33	JN1-54
AD(4)	AG34	JN1-55
AD(3)	AF30	JN1-58
AD(2)	AF31	JN1-59
AD(1)	AF32	JN1-60
AD(0)	AF33	JN1-61
PMC_REQ64#	AN30	JN1-64

Table 82. PMC Interface JN2 Pin Assignments

Signal Name	APEX Pin	PMC Pin
PMC_GLOB_RES	L6	JN2-13
AD(30)	AP31	JN2-19
AD(29)	AN31	JN2-20
AD(26)	AR33	JN2-22
AD(24)	AR34	JN2-23
PMC_IDSEL	AL34	JN2-25
AD(23)	AM35	JN2-26
AD(20)	AK30	JN2-28
AD(18)	AK32	JN2-29
AD(16)	AJ30	JN2-31
PMC_C_BE(2)	AL25	JN2-32
PMC_TRDY#	AP19	JN2-35
PMC_STOP#	AP30	JN2-38
PMC_PERR#	AR29	JN2-39
PMC_SERR#	AP29	JN2-42
PMC_C_BE(1)	AN26	JN2-43
AD(14)	AJ32	JN2-45
AD(13)	AJ34	JN2-46
AD(10)	AH32	JN2-48
AD(8)	AH34	JN2-49
AD(7)	AG31	JN2-51

Table 83. PMC Interface JN3 Pin Assignments (Part 1 of 2)

Signal Name	APEX Pin	PMC Pin
PMC_C_BE(7)	AL26	JN3-4
PMC_C_BE(6)	AP27	JN3-5
PMC_C_BE(5)	AN27	JN3-6
PMC_C_BE(4)	AP28	JN3-7
PMC_PAR64	AN28	JN3-10
AD(63)	AF35	JN3-11
AD(62)	AE30	JN3-12
AD(61)	AE31	JN3-13
AD(60)	AE32	JN3-16
AD(59)	AE35	JN3-17
AD(58)	AD30	JN3-18

Table 83. PMC Interface JN3 Pin Assignments (Part 2 of 2)

Signal Name	APEX Pin	PMC Pin
AD(57)	AD31	JN3-19
AD(56)	AD32	JN3-22
AD(55)	AD34	JN3-23
AD(54)	AD35	JN3-24
AD(53)	AC30	JN3-25
AD(52)	AC31	JN3-28
AD(51)	AC34	JN3-29
AD(50)	AC35	JN3-30
AD(49)	AB30	JN3-31
AD(48)	AB31	JN3-34
AD(47)	AB33	JN3-35
AD(46)	AB34	JN3-36
AD(45)	AB35	JN3-37
AD(44)	R30	JN3-40
AD(43)	AA33	JN3-41
AD(42)	AA34	JN3-42
AD(41)	T32	JN3-43
AD(40)	T30	JN3-46
AD(39)	P32	JN3-47
AD(38)	Y33	JN3-48
AD(37)	P35	JN3-49
AD(36)	Y35	JN3-52
AD(35)	R32	JN3-53
AD(34)	R33	JN3-54
AD(33)	T31	JN3-55
AD(32)	R35	JN3-58

Table 84. General-Purpose Mezzanine Interface J3 Pin Assignments

Signal Name	APEX Pin	GP Mezzanine Connector Pin
GP_IO(0)	K30	J3-1
GP_IO(1)	K32	J3-5
GP_IO(2)	K33	J3-7
GP_IO(3)	K34	J3-9
GP_IO(4)	K35	J3-13
GP_IO(5)	L30	J3-17
GP_IO(6)	L31	J3-19
GP_IO(7)	L32	J3-21
GP_IO(8)	L33	J3-23
GP_IO(9)	L34	J3-27
GP_IO(10)	L35	J3-29
GP_IO(11)	M31	J3-31
GP_IO(12)	M32	J3-33
GP_IO(13)	M33	J3-37
GP_IO(14)	M34	J3-41
GP_IO(15)	M35	J3-43
GP_IO(16)	N30	J3-45
GP_IO(17)	H34	J3-47
GP_IO(18)	H35	J3-49
GP_IO(19)	M1	J3-53
GP_IO(20)	N1	J3-55
GP_IO(21)	P2	J3-57
GP_IO(22)	R2	J3-59
GP_IO(23)	A14	J3-61
GP_IO(24)	C15	J3-4
GP_IO(29)	L2	J3-10

Table 85. General-Purpose Mezzanine J2 Pin Assignments

Signal Name	APEX Pin	GP Mezzanine Connector Pin
GP_IO(25)	H30	J2-3
GP_IO(26)	H31	J2-5
GP_IO(27)	H32	J2-9
GP_IO(28)	H33	J2-11
GP_MEZZ_RST	AG4	J2-13
GP_IO(30)	K3	J2-17
GP_IO(31)	K4	J2-19
GP_IO(32)	K5	J2-23
GP_IO(33)	K6	J2-25
GP_IO(34)	AL28	J2-29
GP_IO(35)	AM28	J2-31
GP_IO(36)	G34	J2-35
GP_IO(37)	G35	J2-39
CLKOUT0	U31	J2-43
CLKOUT1	Y3	J2-49
CLKFBIN0	Y32	J2-45
CLKFBIN1	T4	J2-51

Table 86. VGA Interface Pin Assignments

Signal Name	APEX Pin	Description
VSYNC	AM22	Vertical Synchronization
HSYNC	AM23	Horizontal Synchronization
BLUE	AN5	Blue Signal Output
GREEN	AN6	Green Signal Output
RED	AN7	Red Signal Output

Table 87. LCD Interface Pin Assignments

Signal Name	APEX Pin	Description
LCD_DB(0)	M2	Data signal (LSB)
LCD_DB(1)	M3	Data signal
LCD_DB(2)	M4	Data signal
LCD_DB(3)	M5	Data signal
LCD_DB(4)	N2	Data signal
LCD_DB(5)	N3	Data signal
LCD_DB(6)	N5	Data signal
LCD_DB(7)	N6	Data signal (MSB)
LCD_RS	P1	Register Select
LCD_RW	P3	Read / not Write signal
LCD_ENABLE	P4	Enable signal

Table 88. LED & Switch Pin Assignments

Signal Name	APEX Pin	Description
LOCK1/LED 4	AA30	Active high lock 1 / user LED
LOCK2/LED 3	AB6	Active high lock 2 / user LED
LOCK3 / LED 2	R31	Active high lock 3 / user LED
LOCK4 / LED 1	AC6	Active high lock 4 / user LED
APEX_LED5	K2	User LED 5 (active low)
APEX_LED6	K1	User LED 6 (active low)
GLOB_RES	T6	Global device clear input
APEX_SW2	B17	Low skew reset
APEX_SW3	L4	User switch
APEX_SW4	L5	User switch

Connector Pin Assignments

For the connectors on the board, the pin numbering is indicated on the board.

JTAG / MasterBlaster Configuration Header

The MasterBlaster cable header is a 2 × 5-pin 0.1-inch header used to connect the MasterBlaster cable to the development board. The reference designator for the header is JP12. Table 89 lists the pin definitions for the JTAG/MasterBlaster header.

Table 89. JTAG/MasterBlaster Header Pin Definition

Pin	Signal Name
1	MASTER_TCK
2	GND
3	MASTER_TDO
4	VCC (3.3 V)
5	MASTER_TMS
6	VIO (3.3 V)
7	N/C
8	N/C
9	MASTER_TDI
10	GND

EJTAG Connector

The EJTAG connector is a 2 × 26-pin 0.050-inch header. The reference designator for the header is J10. Table 90 only lists the odd pins because the even-numbered pins are connected to ground.

Table 90. EJTAG Connector Pin Definitions (Part 1 of 2)

Pin	Signal Name
1	EJTAG_TRST
3	EJTAG_TDI
5	EJTAG_TDO
7	EJTAG_TMS
9	EJTAG_TCK
11	EJTAG_RST
13	EJTAG_PCST[0]
15	EJTAG_PCST[1]

Table 90. EJTAG Connector Pin Definitions (Part 2 of 2)

Pin	Signal Name
17	EJTAG_PCST[2]
19	EJTAG_DCLK
21	EJTAG_TRC2
23	EJTAG_PCST2[0]
25	EJTAG_PCST2[1]
27	EJTAG_PCST2[2]
29	EJTAG_TPC3
31	EJTAG_PCST3[0]
33	EJTAG_PCST3[1]
35	EJTAG_PCST3[2]
37	EJTAG_TPC4
39	EJTAG_PCST4[0]
41	EJTAG_PCST4[1]
43	EJTAG_PCST4[2]
45	EJTAG_TPC5
47	EJTAG_TPC6
49	EJTAG_TPC7
51	EJTAG_TPC8

RS-232 DTE Connector

Table 91 lists the RS-232C DTE interface connector pin-out. The RS-232C DTE is a DB9 female connector. The reference designator for this connector is J12.

Table 91. RS-232C DTE Connector Definitions

Pin	Signal Name	Input/Output
1	DCD	Input
2	RD	Input
3	TD	Output
4	DTR	Output
5	GND	–
6	DSR	Input
7	RTS	Output
8	CTS	Input
9	N/C	–

RS-232 DCE Connector

Table 92 lists the pin out for the RS-232C DCE interface connector. The RS-232C DCE connector is a DB9 male receptacle. The reference designator for this connector is J13.

Table 92. RS-232C DCE Connector Definitions

Pin	Signal Name	Input/Output
1	DCD	Output
2	RD	Output
3	TD	Input
4	DTR	Input
5	GND	–
6	DSR	Output
7	RTS	Input
8	CTS	Output
9	N/C	–

PS/2 Connectors

Table 93 lists the PS/2 pin outs. These pin outs are the same for both the J17 and J18 connectors. Table 93 lists the connector pin definitions for both PS/2 connectors.

Table 93. PS/2 Connector Definitions

Pin	Signal Name	Input/Output
1	DATA	Input/Output
2	N/C	–
3	GND	–
4	5 V	–
5	CLOCK	Input/Output
6	N/C	–

USB Connector

The USB connector is J16. Table 94 lists the connector pin definitions.

Table 94. USB Connector Definitions

Pin	Signal Name	Input/Output
1	Optional Power	Output
2	D-	Input/Output
3	D+	Input/Output
4	GND	Output

If the downstream device requires power, it may be provided by installing JP20. Be sure to remove this jumper if power is not required.

IEEE-1394a FireWire Connector

The FireWire connector is J15, and the connector pin definition is listed in Table 95.

Table 95. IEEE-1394a FireWire Connector Definitions

Pin	Signal Name	Input/Output
1	CPS	Input
2	GND	–
3	TPB0-	Input/Output
4	TPB0+	Input/Output
5	TPA0-	Input/Output
6	TPA0+	Input/Output

Ethernet Connector

The ethernet connector is J11. Table 96 lists the connector pin definitions.

Table 96. Ethernet Connector Definitions

Pin	Signal Name	Input / Output
1	TX+	Output
2	TX-	Output
3	RX+	Input
4	N/C	Input
5	N/C	–
6	RX-	Output
7	N/C	Input
8	N/C	Output

Parallel Port Connector

The IEEE-1284 (parallel port) interface connector is J14 and is a DB25 female connector. The connector pin definitions are listed in Table 97.

Table 97. Parallel Port Connector Definitions (Part 1 of 2)

Pin	Signal Name	Input / Output
1	STROBE	Output
2	D(0)	Input/Output
3	D(1)	Input/Output
4	D(2)	Input/Output
5	D(3)	Input/Output
6	D(4)	Input/Output
7	D(5)	Input/Output
8	D(6)	Input/Output
9	D(7)	Input/Output
10	ACKNLG	Input
11	BUSY	Input
12	PEND	Input
13	SLCT	Input
14	AFEED	Output
15	ERROR	Input
16	INIT	Output
17	SLCT	Output

Table 97. Parallel Port Connector Definitions (Part 2 of 2)

Pin	Signal Name	Input / Output
18	GND	–
19	GND	–
20	GND	–
21	GND	–
22	GND	–
23	GND	–
24	GND	–
25	GND	–

VGA Connector

The VGA Connector is J9, and is a DB15 male connector. Table 98 lists the connector pin definitions.

Table 98. VGA Connector Definitions

Pin	Signal Name	Input / Output
1	RED	Output
2	GREEN	Output
3	BLUE	Output
4	N/C	–
5	GND	–
6	GND	–
7	GND	–
8	GND	–
9	N/C	–
10	GND	–
11	N/C	–
12	N/C	–
13	HSYNC	Output
14	VSYNC	Output
15	N/C	–

Test Connectors

This section lists the pins connected to each of the six logic analyzer test connectors on the board. These connectors are not in use, but the signals are connected as listed in Tables 99 through 104. These signals may be used by populating the required connector or probing directly on the connector pads.

Table 99. JP5 Pin Definitions

Pin	Signal Name
1	N/C
2	N/C
3	N/C
4	GPM_DATA[7]
5	GPM_DATA[6]
6	GPM_DATA[5]
7	GPM_DATA[4]
8	GPM_DATA[3]
9	GPM_DATA[2]
10	GPM_DATA[1]
11	GPM_DATA[0]
12	GPM_ADDRESS[7]
13	GPM_ADDRESS[6]
14	GPM_ADDRESS[5]
15	GPM_ADDRESS[4]
16	GPM_ADDRESS[3]
17	GPM_ADDRESS[2]
18	GPM_ADDRESS[1]
19	GPM_ADDRESS[0]
20	GND

Table 100. JP3 Pin Definitions

Pin	Signal Name
1	N/C
2	N/C
3	N/C
4	SSRAM2_D[7]
5	SSRAM2_D[6]
6	SSRAM2_D[5]
7	SSRAM2_D[4]
8	SSRAM2_D[3]
9	SSRAM2_D[2]
10	SSRAM2_D[1]
11	SSRAM2_D[0]
12	SSRAM2_A[7]
13	SSRAM2_A[6]
14	SSRAM2_A[5]
15	SSRAM2_A[4]
16	SSRAM2_A[3]
17	SSRAM2_A[2]
18	SSRAM2_A[1]
19	SSRAM2_A[0]
20	GND

Table 101. JP2 Pin Definitions (Part 1 of 2)

Pin	Signal Name
1	N/C
2	N/C
3	N/C
4	SSRAM1_D[7]
5	SSRAM1_D[6]
6	SSRAM1_D[5]
7	SSRAM1_D[4]
8	SSRAM1_D[3]
9	SSRAM1_D[2]
10	SSRAM1_D[1]
11	SSRAM1_D[0]
12	SSRAM1_A[7]

Table 101. JP2 Pin Definitions (Part 2 of 2)

Pin	Signal Name
13	SSRAM1_A[6]
14	SSRAM1_A[5]
15	SSRAM1_A[4]
16	SSRAM1_A[3]
17	SSRAM1_A[2]
18	SSRAM1_A[1]
19	SSRAM1_A[0]
20	GND

Table 102. JP1 Pin Definitions

Pin	Signal Name
1	N/C
2	N/C
3	N/C
4	SSRAM1_BWE[3]
5	SSRAM1_BWE[2]
6	SSRAM1_BWE[1]
7	SSRAM1_BWE[0]
8	SSRAM1_ADV#
9	SSRAM1_ADSP#
10	SSRAM1_ADSC#
11	SSRAM1_OE#
12	SSRAM1_BWE#
13	SSRAM1_GW#
14	SSRAM1_CE2
15	SSRAM1_CE#
16	FLASH_WE[3]
17	FLASH_WE[2]
18	FLASH_WE[1]
19	FLASH_WE[0]
20	GND

Table 103. JP4 Pin Definitions

Pin	Signal Name
1	N/C
2	N/C
3	TEST_CLK
4	FLASH_RP#
5	FLASH_OE#
6	SSRAM2_BWE[3]
7	SSRAM2_BWE[2]
8	SSRAM2_BWE[1]
9	SSRAM2_BWE[0]
10	SSRAM2_ADV#
11	SSRAM2_ADSP#
12	SSRAM2_ADSC#
13	SSRAM2_OE#
14	SSRAM2_BWE#
15	SSRAM2_GW#
16	SSRAM2_CE2
17	SSRAM2_CE#
18	FLASH_CS#
19	TEST_CLK
20	GND

Table 104. JP6 Pin Definitions (Part 1 of 2)

Pin	Signal Name
1	N/C
2	N/C
3	N/C
4	SDRAM_CS2#
5	SDRAM_RAS#
6	EPROM_CE2#
7	SDRAM_CS1#
8	EPROM_CE1#
9	SDRAM_CAS#
10	EPROM_OE
11	SDRAM_WE#
12	SDRAM_DQM[7]

Table 104. JP6 Pin Definitions (Part 2 of 2)

Pin	Signal Name
13	SDRAM_DQM[6]
14	SDRAM_DQM[5]
15	SDRAM_DQM[4]
16	SDRAM_DQM[3]
17	SDRAM_DQM[2]
18	SDRAM_DQM[1]
19	SDRAM_DQM[0]
20	GND

General Usage Guidelines

To ensure proper use of the development board and to avoid damage to the board, follow the guidelines in this section.

SDRAM Data Bus

The SDRAM data bus is 64-bits wide and the general-purpose memory data bus is only 32-bits wide. To allow all of the SDRAM memory array to be accessed, the data bus is doubled. The lower half of the SDRAM data pins on the DIMM are directly connected to the upper half. For example, data pins 0 and 32 on the DIMM are connected to general-purpose memory data bus pin 0. Only one of these pins can be active at one time. The output from the SDRAM is controlled by the DQM[7:0] lines; ensure that only the desired portion of the bus is enabled at any one time.

Parallel Port Jumpers

Nine additional jumpers on the development board allow the parallel port to operate in both host and peripheral mode. The jumpers change the direction of the control lines depending on which mode is desired. Ensure that all of the jumpers are in the same position. All jumpers must short pins 1 and 2 for the port to be in host mode. All jumpers must short pins 2 and 3 for the port to be in peripheral mode. Any other configuration will cause contention and the parallel port will not function properly.

Unused APEX Device Pins

All general-purpose I/O APEX device pins have been allocated for on-board functions. In most circumstances, not all of the pins will be required to be active. To avoid unnecessary power consumption and possible contention, it is very important that unused pins are left in the high impedance (input) state. This will avoid unnecessary power consumption and possible contention. All the critical control lines for the interfaces on the board are pulled to the inactive state. If a device is not used, it can be ignored and the APEX device interface pins left as inputs.

Power Consumption

Power consumption issues need to be addressed only if the board is powered from a terminal strip and not the supply. Altera recommends that you monitor the input current to be sure that sufficient power is supplied. The power required by the board is directly related to the following:

- Number of interfaces used
- Density and speed of the APEX device
- Population of either mezzanine interface

The typical maximum current is 5.0 A. This can be exceeded if the board is heavily loaded with many interfaces running at high-clock speeds.

Testing Software

The development board includes test cores to help developers perform functional tests on cores.

Test Core Functionality

For implementing a test plan, multiple test cores are included with the development board and can be programmed onto the APEX device using the JTAG chain. Each test core tests one or more interfaces and uses LEDs to indicate a pass or a fail in a design.

Table 105 lists test cores available to test the development board.

Table 105. Test Cores Available for the Development Board

Test Core Name	Test Interface
Mix_Test_1.sof	-Configuration of the APEX device -Switches and LED interface -VGA interface
Mix_Test_2.sof	-SRAM1 interface -SRAM2 interface
Mix_Test_3.sof	-RS232 interface -PS2 interface -USB interface -Parallel interface -PMC interface -GPM interface -EJTAG interface -JTAG chain
Mix_Test_4.sof	-FireWire interface -Ethernet interface
Mix_Test_5.sof	-Flash interface -Eprom interface
Sdram_top.sof	-SDRAM interface
Lcd_top.pof **Lcd_top1.pof** **Lcd_top2.pof**	-LCD interface -EPC2s

Mix_Test_1 Core

The Mix_Test_1 Core performs a test on the configuration interface, the switches and LED interface, and the VGA interface.

Switch & LED Test

The configuration interface test confirms the proper operation of the configuration circuitry of the APEX device. The APEX device is first configured directly using the MasterBlaster cable with the Mix_Test_1 test core, **Mix_Test_1.sof**. Proper configuration of the APEX device indicates proper functioning of the configuration interface.

The switches and LED interface test confirms the proper operation of the user switches and LEDs. The test core allows the LEDs to be turned on and off using the user-defined switches, confirming the proper operation of both the switches and the LEDs. During reset, all the LEDs will illuminate. Pressing another switch causes two of the LEDs to illuminate. Table 106 lists user switch and LED tests.

Table 106. User Switch & LED Test

User Switch	User LEDs
S2	LED11, LED12
S3	LED13, LED14
S4	LED15, LED16

VGA Interface Test

The VGA interface test confirms the proper operation of the VGA interface. The core provides a "walking ones" pattern output waveform to the five outputs and to the VGA connector that is measured using an oscilloscope to confirm proper operation. The proper LVTTL logic levels are confirmed for the sync signals while the color signals are verified for an acceptable analog level: 0.5 to 0.7 V. The presence and timing of the pulse waveform verifies the proper connection of the VGA signals. A pulse width greater than a clock period of 40 ns, or multiple pulses occurring within a five clock period time frame, signifies a failed test result.

Mix_Test_2 Core

The Mix_Test_2 Core confirms the proper operation of both SSRAM memories operating at 66 MHz. Both reads and writes are performed to each device, including 32-bit accesses and 8-bit cycles to test the byte lane control signals and burst accesses. In addition, the address and data convergence test of the SSRAM is also performed. The address convergence test is performed first, using 32-bit accesses. The test writes a unique value to all addresses and reads each memory location to ensure the presence of the correct data. The core then checks the integrity of the data bus by writing a "walking ones and zeros" pattern to the SSRAM. All values are read back and checked. The core performs a 32-bit burst write length of four followed by four, 32-bit reads to verify the data. Two 16-bit writes are followed by a single 32-bit read for verification of the data. Finally, a single 32-bit write is confirmed by four 8-bit reads.

Table 107 lists the error detection codes used to identify an interface that failed a test. LEDs D[14..11] are used to display this error detection code.

Table 107. Error Detection Codes

SRAM Core	Error LED	Done LED
SRAM1 core	D11	D13
SRAM2 core	D12	D14

Mix_Test_3 Core

The Mix_Test_3 performs a variety of tests, including:

- RS-232 Interface
- PS/2 Interface
- USB Interface
- IEEE 1284 Interface
- PMC-PCI Interface
- General-Purpose Mezzanine Interface
- EJTAG Interface
- JTAG Interface

RS-232 Interface

This test confirms the proper operation of the RS-232 interface. The core provides a "walking ones and zeros" pattern to the RS-232 outputs. The outputs of each connector are wired to the inputs of the other connector. The inputs are read to check for the proper pattern on the outputs of each interface.

PS/2 Interface

This test confirms the proper operation of the PS/2 interface. The core provides a "walking ones and zeros" pattern to the PS/2 connectors that are wired from one connector to the other. The inputs are read to check for the proper pattern on the outputs of each interface.

Universal Serial Bus (USB) Interface

This test confirms the proper operation of the USB interface. The core provides an output waveform to the USB connector that is measured using an oscilloscope to confirm proper operation. A data pattern of `10101100` is transmitted at 12 MHz. The input signals from the USB transceiver are also checked to confirm they remain at a low LVTTL logic level.

IEEE 1284 Parallel Interface

This test confirms the proper operation of the parallel interface. The four sub-cores provide a "walking ones and zeros" pattern to the parallel connector that has the various outputs wired to the available inputs. The inputs are read to check for the proper pattern on the outputs of each interface. Multiple cores and connectors are required to cover all the available outputs with the limited number of inputs.

PMC - PCI Interface

This test confirms the proper operation of the PMC interface. The core provides a "walking ones and zeros" pattern to the PMC connectors that are wired from the designated outputs to the inputs. The inputs are read to check for the proper pattern on the outputs of each interface. This core is run at 66 Mhz to ensure that the PCI interface can support operation at this frequency.

General-Purpose Mezzanine Interface

This test confirms the proper operation of the General-Purpose Mezzanine interface. The core provides a "walking ones and zeros" pattern to the GPM connectors that are wired from one connector to the other. The inputs are read to check for the proper pattern on the outputs of each interface.

EJTAG Interface

This test confirms the proper operation of the EJTAG interface. The core provides a "walking ones and zeros" pattern to the EJTAG connector that is wired from outputs to inputs. The inputs are read to check for the proper pattern on the outputs of each interface.

JTAG Interface

This test confirms the proper operation of the JTAG interface. The JTAG chain is configured to include the APEX device, PMC, and general-purpose mezzanine. The cables on the PMC and general-purpose mezzanine connectors connect the `TDI` signal to `TDO` allowing the APEX device to be programmed if the chain is functional. The Mix_Test_3 core, **Mix_Test_3.sof** is programmed onto the APEX device.

Table 108 lists the error detection codes that are used to identify an interface that failed the test. LEDs `D[16..14]` are used to display this error detection code.

Table 108. Mix_Test_3 Error Detection Codes *Note (1)*

Interface	D14	D15	D16
No failure	0	0	0
RS232	0	0	1
EJTAG	0	1	0
General-purpose mezzanine	0	1	1
Parallel	1	0	0
PMC	1	0	1
PS2	1	1	0
USB	1	1	1

Note:
(1) A one (1) indicates illuminated, and a zero (0) indicates not illuminated.

Mix_Test_4 Core

The Mix_Test_4 performs tests on the IEEE 1394 and 10/100BASE-TX ethernet interfaces.

IEEE 1394a FireWire Interface

This test confirms the proper operation of the FireWire interface. The core performs read and write cycles to registers on the FireWire physical device to confirm the proper operation of the interface.

10/100BASE-TX Ethernet Interface

This test confirms the proper operation of the ethernet interface. The core performs read and write cycles to registers on the ethernet physical device to confirm the proper operation of the interface. In addition, a collision test, as specified in the device data sheet, is completed. The operation of the status LEDs for the ethernet interface are manually verified through the selection of the technology input switch positions.

Table 109 lists error detection code used to identify an interface that failed the test. LEDs `D[13..12]` are used to display this error detection code.

Table 109. FireWire Test Error Detection Codes

Interface	Error LED	Done LED
FireWire core	D12	D13
Ethernet core	N/A	N/A

Mix_Text_5 Core

The Mix_Test_5 performs tests on the EPROM configuration device and Flash interfaces.

EPROM Configuration Device Interface

This test confirms the proper operation of the EPROM configuration device memory. Several reads are performed that include not only 32-bit wide accesses, but also 16-bit read cycles to test the word lane control signals. The core first reads eight 32-bit values followed by eight 16-bit accesses to one word lane. Eight more 16-bit reads are performed to the other portion of the bus. In each case, the received data is compared to the expected value corresponding to the pre-programmed test pattern present in the EPROM device, signaling an error if they do not agree.

Flash Interface

This test confirms the proper operation of the Flash memory. Both reads and writes perform 32-bit accesses and 8-bit cycles to test the byte lane control signals. In addition, the address convergence testing of the general purpose memory bus is performed using the Flash memory. The core erases the entire Flash memory. The address convergence test is then performed, using 32-bit accesses, that writes a unique value to all addresses and reads each memory location to ensure the presence of the correct data. A portion of the memory is erased to allow four 8-bit write cycles to be completed, testing the byte lanes control signals. A single 32-bit read is performed to verify these byte-sized writes.

Table 110 lists the error detection codes used to identify an interface that failed the test. LEDs `D[14..11]` are used to display this error detection code.

Table 110. Flash & EPROM Test Error Detection Codes

Interface Core	Error LED	Done LED
Flash core	LED11	LED13
EPROM core	LED12	LED14

SDRAM_top

This test confirms the proper operation of the SDRAM memory operating at 66 MHz. Both reads and writes perform 32-bit accesses and 8-bit cycles to test the byte lane control signals and both burst read and write accesses. In addition, the data convergence testing of the general-purpose memory bus is performed using the SDRAM memory. The core first initializes the SDRAM, then performs the "walking ones and zeros" data convergence test on the data bus. Eight individual 8-bit writes are performed followed by two 32-bit reads to verify the data to confirm the byte lane control signals. Finally, the core performs a burst write of length four followed by a burst read of length four. A pass is communicated by the illumination of LED D13. A failure is indicated by the illumination of LED D11.

LCD_top

The LCD_top core is downloaded onto the EPC2 devices. When the board is powered up, and the LCD_top core is programmed in the EPC2 configuration devices, the LCD interface displays the phrase "SOPC Development Board" indicating that the LCD interface is functioning correctly.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com
Applications Hotline:
(800) 800-EPLD
Literature Services:
(888) 3-ALTERA
lit_req@altera.com