White Paper

Using I/O Standards in the Quartus Software

This document shows how to implement and view the selectable I/O standards for APEX™ 20KE devices in the Quartus™ software and give placement and assignment guidelines. The following topics will be discussed in detail.

- APEX 20KE I/O Standard Support
- Device & Pin Options Dialog Box (Compiler Settings Dialog Box)
- Pin Assignments Dialog Box
- Representation of I/O Banks and I/O Standards in the Floorplan Editor
- Guidelines for Selectable I/O Standards
- I/O & V_{REF} Pin Placement Guidelines

APEX 20KE I/O Standard Support

The I/O banks in APEX 20KE devices support 13 I/O standards and are the first programmable logic devices (PLDs) in the industry with dedicated circuitry supporting low-voltage differential signaling (LVDS). Altera's revolutionary APEX 20KE devices offer the highest density, highest performance programmable logic solution with the necessary I/O standards for the communication and computer industries.

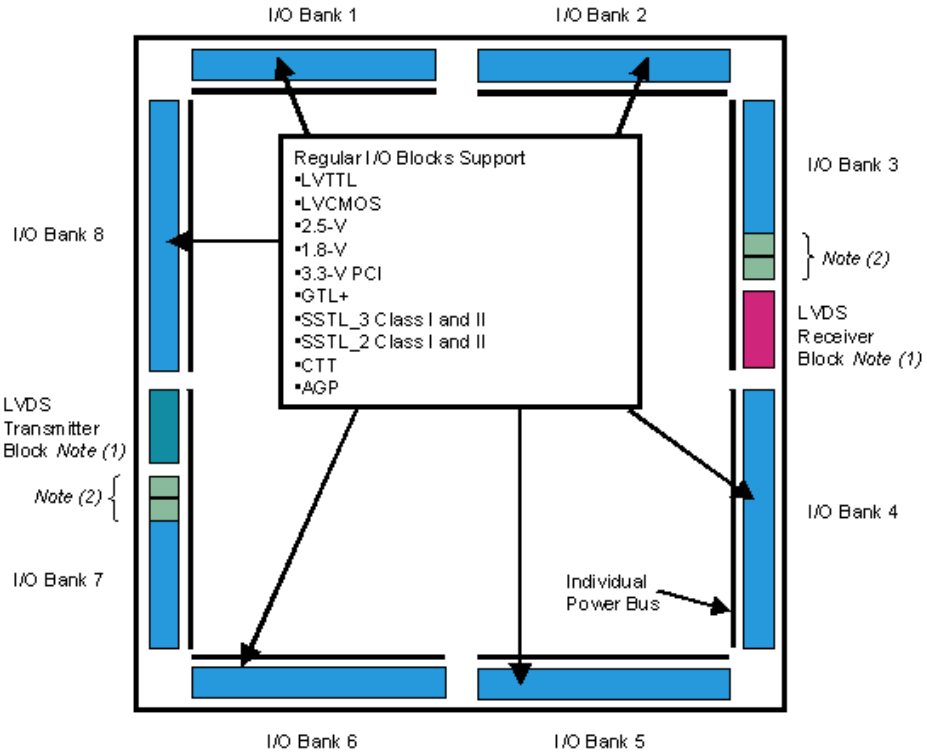
The I/O buffers in APEX 20KE devices are designed to meet the voltage, drive strength, and AC characteristics necessary to be compliant with the I/O standards listed in Table 1.

Table 1. APEX 20KE Supported I/O Standards

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTL	Single-ended	N/A	3.3	N/A
LVCMOS	Single-ended	N/A	3.3	N/A
2.5V	Single-ended	N/A	2.5	N/A
1.8V	Single-ended	N/A	1.8	N/A
3.3-V PCI	Single-ended	N/A	3.3	N/A
LVDS	Differential	N/A	3.3	N/A
GTL+	Voltage referenced	1.0	N/A	1.5
SSTL-2 Class I and II	Voltage referenced	1.125	2.5	1.125
SSTL-3 Class I and II	Voltage referenced	1.5	3.3	1.5
AGP	Voltage referenced	1.32	3.3	N/A
CTT	Voltage referenced	1.5	3.3	1.5

APEX 20KE devices in FineLine BGA™ and BGA packages have eight programmable I/O banks and two LVDS I/O blocks (one transmitter block and one receiver block). The programmable input/output element (IOE) banks in APEX 20KE devices have individual power planes with separate I/O supply voltage (VCCIO) pins for each I/O bank. The V_{CCIO} supply supports 3.3-V, 2.5-V, and 1.8-V levels. Figure 1 shows the representation of the I/O banks.

Figure 1. APEX 20KE I/O Banks



Notes:

(1) If the LVDS transmitter and receiver blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with V_{CCIO} set to 3.3 V, 2.5 V, or 1.8 V.

(2) The first two I/O pins that border the LVDS blocks can only be used for input to maintain voltage stability on the V_{CCIO} plane.

Device & Pin Options Dialog Box (Compiler Settings Dialog Box)

The **Voltage** tab in the **Device & Pin Options** dialog box contains a **Default I/O Standard** drop-down menu, which is used to set the default I/O standard for a device. All I/O pins without a specific I/O standard assignment will default to the I/O standard specified in this drop-down menu. The drop-down menu is populated with the following items for APEX 20KE devices:

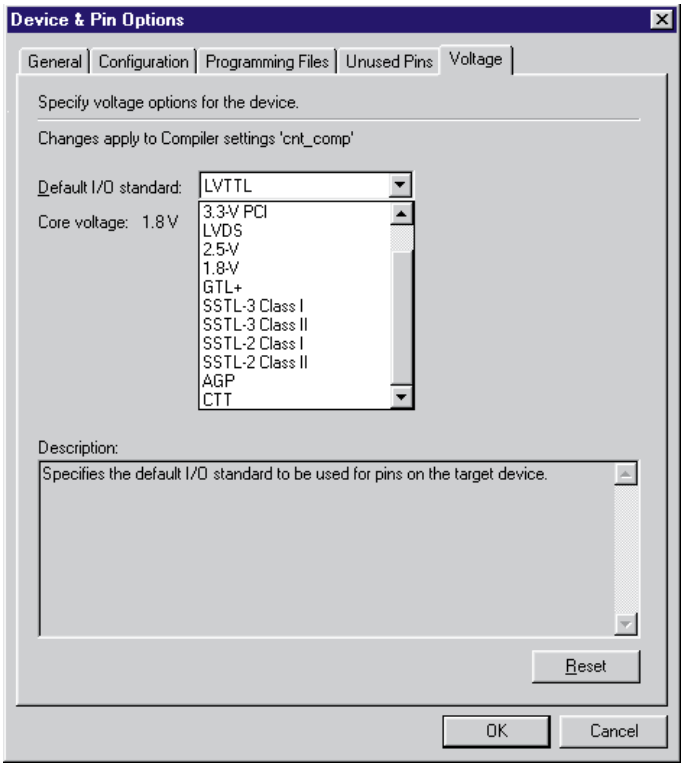
- LVTTL(default setting)
- LVCMOS
- 3.3-V PCI
- LVDS
- 2.5-V
- 1.8-V
- GTL+
- SSTL-2 Class I
- SSTL-2 Class II
- SSTL-3 Class I
- SSTL-3 Class II
- AGP
- CTT

For APEX 20K devices, three possible entries exist in the drop-down menu:

- LVTTL/LVCMOS(default setting)
- 2.5-V
- 3.3-V PCI

Figure 2 shows the **Device & Pin Options** dialog box when targeting an APEX 20KE device.

Figure 2. Device & Pin Options Dialog Box (APEX 20KE Devices)



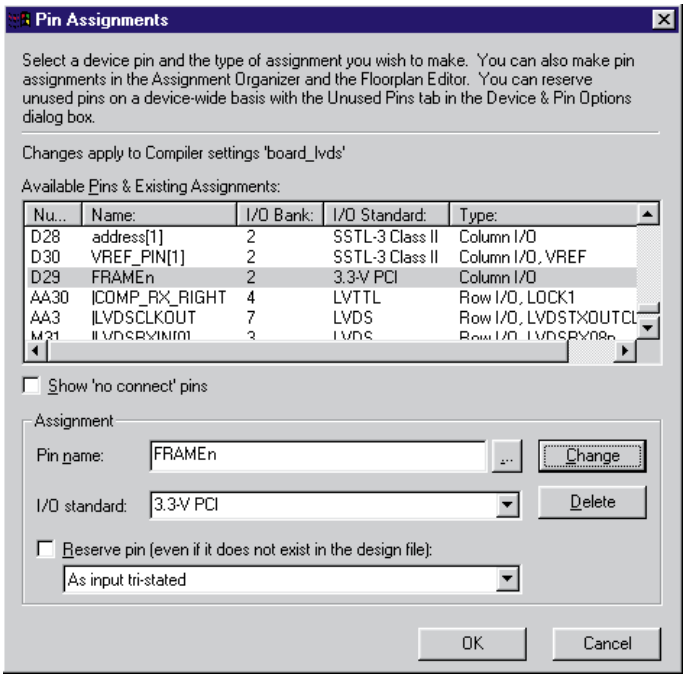
Pin Assignments Dialog Box

In the **Pin Assignments** dialog box, designers make pin assignments, specify I/O standards, make V_{REF} assignments, and view the settings made to each pin.

Figure 3 shows the **Pin Assignments** dialog box. The Number column corresponds with the pin number on the specified package. The Name column contains the user-specified pin name in the design. There are two new columns to note: I/O Bank and I/O Standard. The Type column in the **Available Pins & Existing Assignments** list box displays the following pin types: Row I/O, Column I/O, V_{REF}, Reserved, and dual-purpose pin names. The list box is sortable on any column by clicking on the column heading.

There are drop-down menus for making I/O Standard and Reserved Pin assignments on a pin-by-pin basis. V_{REF} pins are assigned the same way as reserved pins. To select the I/O standard for I/O and V_{REF} pins, choose an I/O standard from the **I/O Standard** drop-down menu. To assign a pin to be a V_{REF}, enter a pin name (reserve pin names are not declared in the design file), check the **Reserve** pin box, and select reserve as V_{REF} from the drop-down menu.

Figure 3. Pin Assignments Dialog Box



Follow the steps below to make pin assignments, designate I/O standard types, and reserve pins. Designers should reserve I/O pins that may be needed in the future.

1. If you have not already done so, open or create the project that you want to modify.

2. Choose **Compiler Settings** (Processing menu).

3. Click the **Chips & Devices** tab.

4. Select the target device in the **Available devices** list.

5. Click **Assign Pins**.

6. In the **Pin Assignments** dialog box, to show the pins for which you cannot assign a node name in the **Available pins & existing assignments** list, turn on **Show 'no connect' pins.**

7. In the **Available pins & existing assignments** list, select the pin number for the pin to which you want to assign, change, or delete a node name assignment.

8. To delete the node name assignment from the pin, under **Assignment,** click **Delete**.

9. To assign a new node name to the pin, or change the existing node name assignment for the pin, under **Assignment**, type a node name in the **Pin name** box.

or

10. Copy the node name to the **Pin Assignments** dialog box with the Node Finder.

11. If you added or changed the node name assignment for the pin and you want to assign an **I/O Standard** to the pin, under **Assignment**, select a standard from the **I/O Standard** list.

12. If you added or changed the node name assignment or I/O standard and you want to reserve the pin for future use, under **Assignment**, turn on **Reserve pin (even if it does not exist in the design file),** and select **As input tri-stated**, **As output driving ground**, **As output driving an unspecified signal**, or **As VREF** from the list.

13. To save a new assignment and add the assignment to the **Available pins & existing assignments** list, under **Assignment**, click **Add**.

14. To save the changed assignment and add the assignment to the **Available pins & existing assignments** list, under **Assignment**, click **Change**.

15. Repeat steps 7 to 15 for each additional assignment you want to make, change, or delete.

16. Click **OK**.

Representation of I/O Banks and I/O Standards in the Floorplan Editor

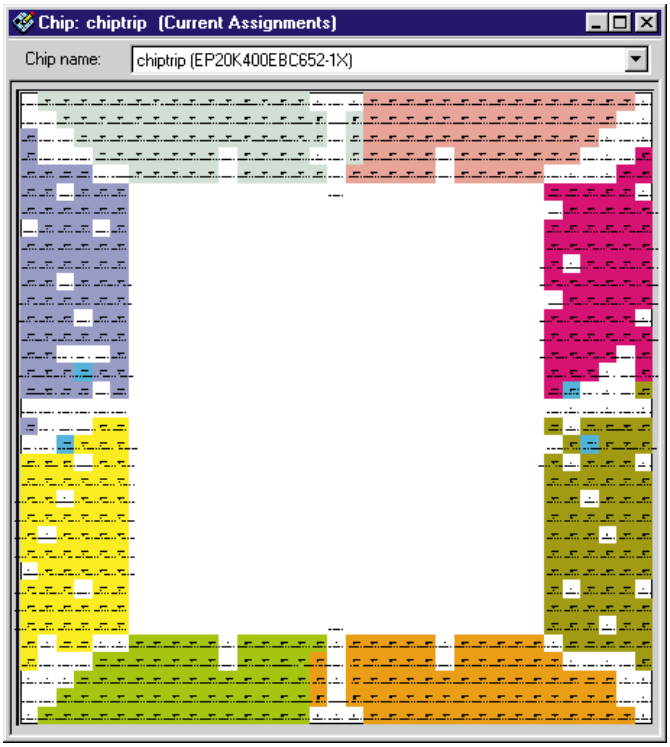
Several enhancements have been made to the Floorplan Editor to support new features in APEX 20KE devices: multiple I/O standards, the PLL, and the LVDS transmitter and receiver block.

I/O Bank Coloring & Numbering

The Floorplan Editor shows membership in I/O banks by using a unique background fill color around each pin for each I/O bank. In addition, the bank number is shown. The Floorplan editor has 2 package views (Package Top, Package Bottom) and three internal views (Interior MegaLABs™, Interior LABs, Interior Cells). In the package views the I/O bank number is labeled above the pin for pin-grid array (PGA) and BGA packages, or on the inside of the device for quad flat pack (QFP) packages. In the interior views, it will be outside the package as a background around the pin name.

Only I/O and `VCCIO` pins have the colored background; `GNDINT`, `GNDIO`, and `VCCINT` pins do not. Figure 4 shows the coloring in the Floorplan Editor for the EP20K400EBC652-1X device in package view.

Figure 4. Package View with Show I/O Banks On



The display of I/O bank colors is controlled by the **Show I/O Banks** command, which is under the View pull-down menu when the Floorplan Editor is open. This command also turns on the display of both the I/O bank colors and bank numbers in the three interior views.

The Floorplan Editor's Color Legend has an entry for each I/O bank color, as shown in Figure 5. The output clock and feedback pins for PLL1 and PLL2 reside in I/O Bank 9 and I/O Bank 10 and can support any of the I/O standards supported for APEX 20KE devices. The **Color Legend** window is located under the View pull-down menu when the Floorplan Editor is open.

Figure 5. Pin Color Legend Window for the Floorplan Editor

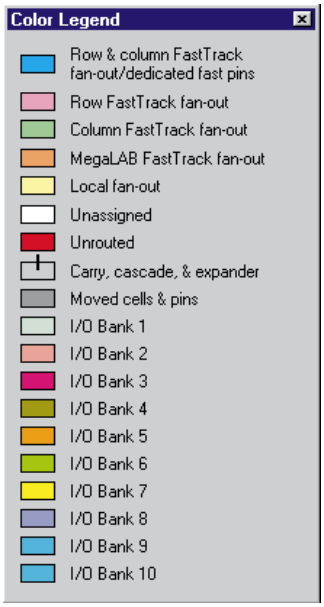


Figure 6 shows a portion of two I/O Banks of the EP20K100E device in package view of a QFP package in the Floorplan Editor.

In the QFP packages, the eight I/O Banks have been merged into 4 merged I/O Banks. The `VCCIO` planes on merged I/O banks are internally connected in the QFP packages. The naming convention for merged I/O banks lists the real I/O bank that the pin belongs to and then lists the I/O bank with which it shares `VCCIO`. The I/O Bank, Bank6 (and Bank7), shares its `VCCIO` with Bank7 (and Bank6) but has a different V_{REF} bus. This allows Bank6 (and Bank7) to be used for one voltage-referenced I/O standard and Bank7 (and Bank6) for another because they have separate VREF buses. For example, Bank6 (and Bank7) can implement GTL+ while Bank7 (and Bank6) implements SSTL-3 Class I.

Figure 6. Top View of the 240-Pin Plastic Quad Flat Pack (PQFP) Package

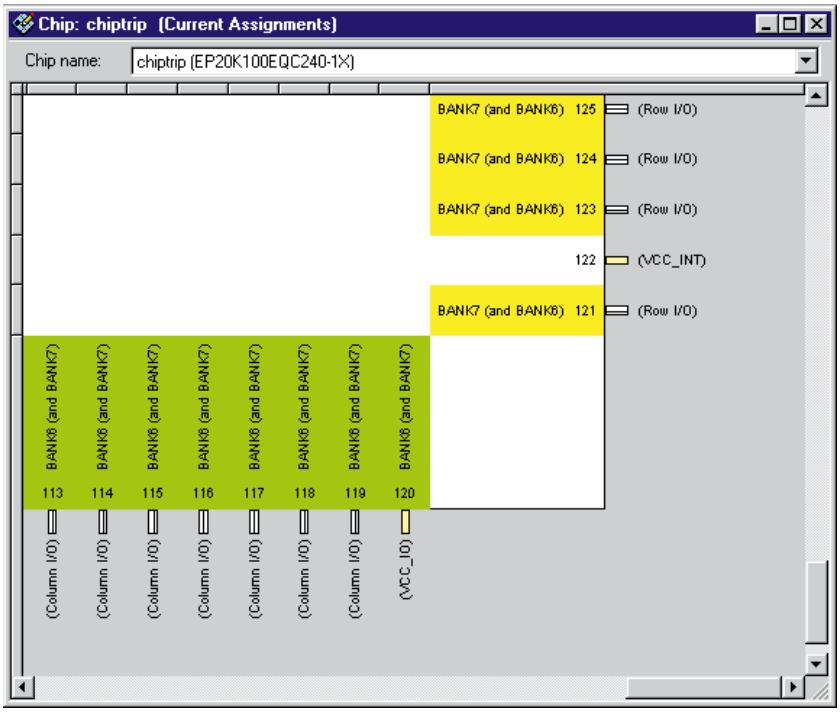


Figure 7 shows the same boundary between I/O Bank 6 and 7 in the BGA package view.

Figure 7. Top View of the 652-Pin BGA Package

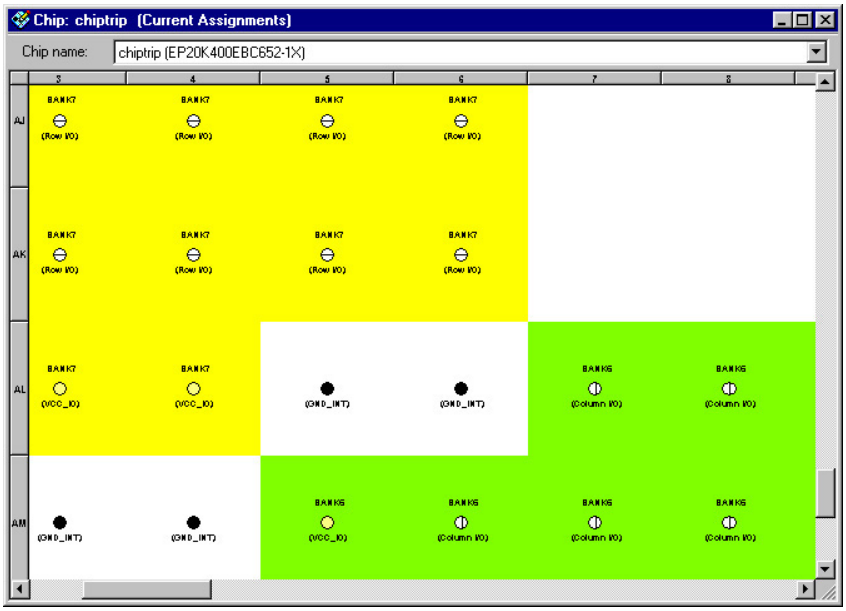
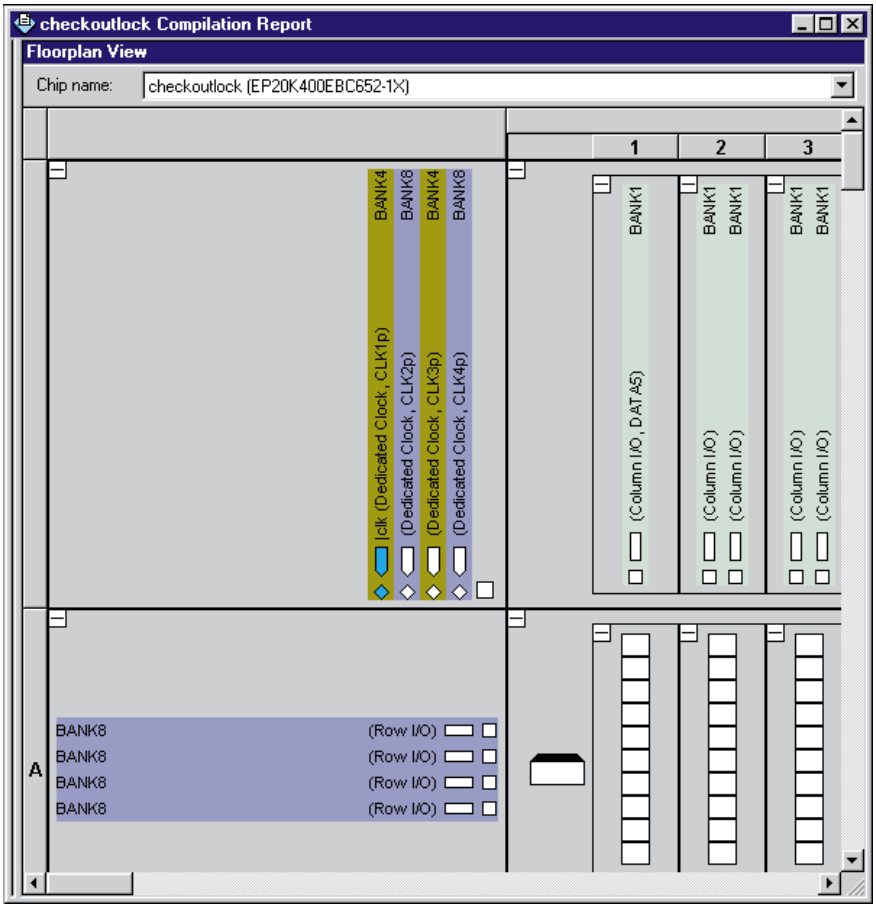


Figure 8 shows the Interior Cells view of the APEX 20KE devices with an “X” suffix in the part number indicating PLL support. The diamond next to the dedicated clocks indicates that the PLL is used.

Figure 8. View of Internal Cells in Floorplan Editor



LVDS Paired Pin Labeling

Information on the dual-purpose paired LVDS pins are displayed in the same text string as the other information on a pin, similar to other pins that have secondary functions such as `INIT_DONE`. For example, in Figure 9 on page 11, Row I/O is now shown as Row I/O, `LVDSRXINCLK1p`.

LVDS pins have a specific naming convention; all LVDS pin names begin with LVDS. The next two characters for data pins indicate whether they belong to the receiver (RX) or transmitter (TX), followed by the two-digit channel <*number*> which ranges from 01 to 16. The last character at the end of the pin name indicates polarity, p for positive polarity and n for negative polarity.

Table 2 summarizes names for all LVDS pins.

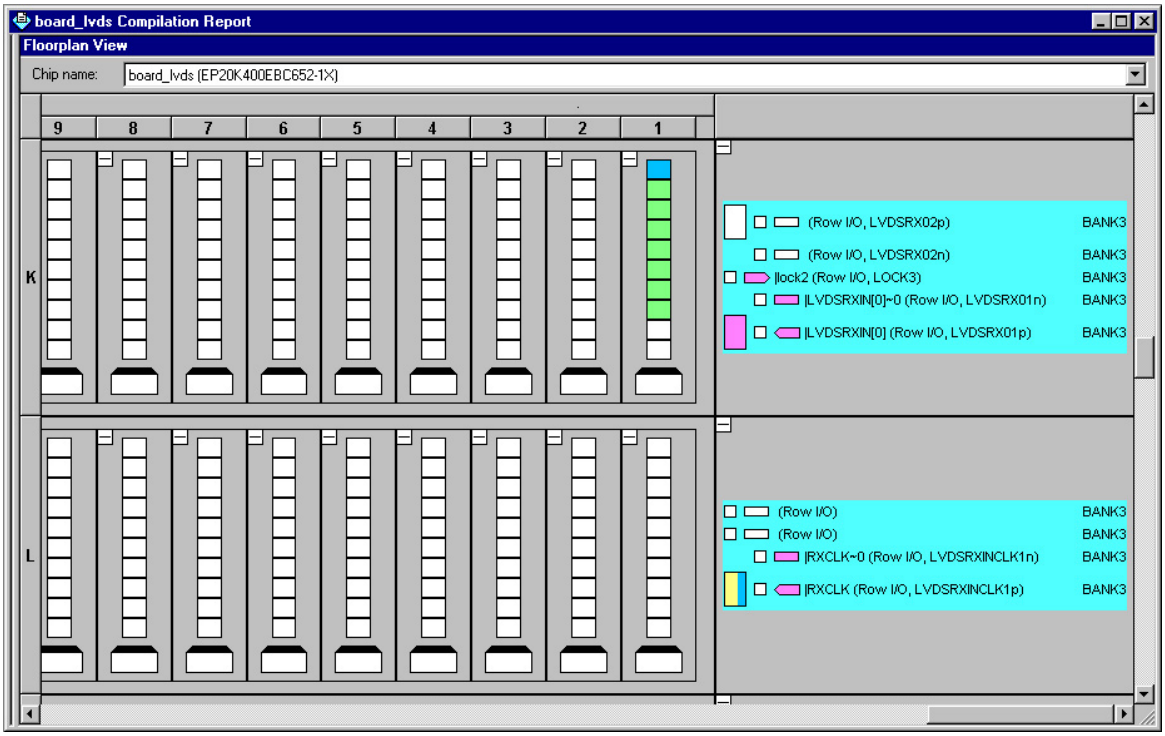
Table 2. LVDS Pin Naming Convention

Pin Names	Function
LVDSRX<*number*>p	Receiver positive data pin
LVDSRX<*number*>n	Receiver negative data pin
LVDSTX<*number*>p	Transmitter positive data pin
LVDSTX<*number*>n	Transmitter negative data pin
LVDSRXINCLK1p	Receiver input clock positive pin
LVDSRXINCLK1n	Receiver input clock negative pin
LVDSTXINCLK1p	Transmitter input clock positive pin
LVDSTXINCLK1n	Transmitter input clock negative pin
LVDSTXOUTCLK1p	Transmitter output clock positive pin
LVDSTXOUTCLK1n	Transmitter output clock negative pin
CLK1p	Dedicated clock 1 positive pin (PLL 1)
CLK1n	Dedicated clock 1 negative pin (PLL 1)
CLK2p	Dedicated clock 2 positive pin (PLL 2)
CLK2n	Dedicated clock 2 negative pin (PLL 2)
CLK3p	Dedicated clock 3 positive pin (PLL 3)
CLK3n	Dedicated clock 3 negative pin (PLL 3)
CLK4p	Dedicated clock 4 positive pin (PLL 4)
CLK4n	Dedicated clock 4 negative pin (PLL 4)
CLKLK_FB1p	Dual-purpose ClockLock feedback positive pin (PLL 1)
CLKLK_FB1n	Dual-purpose ClockLock feedback negative pin (PLL 1)
CLKLK_FB2p	Dual-purpose ClockLock feedback positive pin (PLL 2)
CLKLK_FB2n	Dual-purpose ClockLock feedback negative pin (PLL 2)
CLKLK_OUT1p	Dual-purpose ClockLock output positive pin (PLL 1)
CLKLK_OUT1n	Dual-purpose ClockLock output negative pin (PLL 1)
CLKLK_OUT2p	Dual-purpose ClockLock output positive pin (PLL 2)
CLKLK_OUT2n	Dual-purpose ClockLock output negative pin (PLL 2)

The dedicated clock pins (CLK1p, CLK2p, CLK3p, CLK4p) support LVDS and have optional dual-purpose negative polarity pins associated with them. The PLL feedback pins (CLKLK_FB1p, CLKLK_FB2p) and the PLL output pins (CLKLK_OUT1p, CLKLK_OUT2p) also support LVDS following the same convention as the dedicated clock pins.

Figure 9 shows the LVDS receiver in the Floorplan Editor. The receiver data channel, represented by LVDSRX01p and LVDSRX01n, feeds the dedicated serial-to-parallel converter. The LVDS clock (LVDSRXINCLK1p, LVDSINCLK1n) clocks the serial-to-parallel converter. The serial-to-parallel converter is shown by the filled rectangle adjacent to the IOE register associated with each positive polarity LVDS data and clock pin.

Figure 9. LVDS Receiver

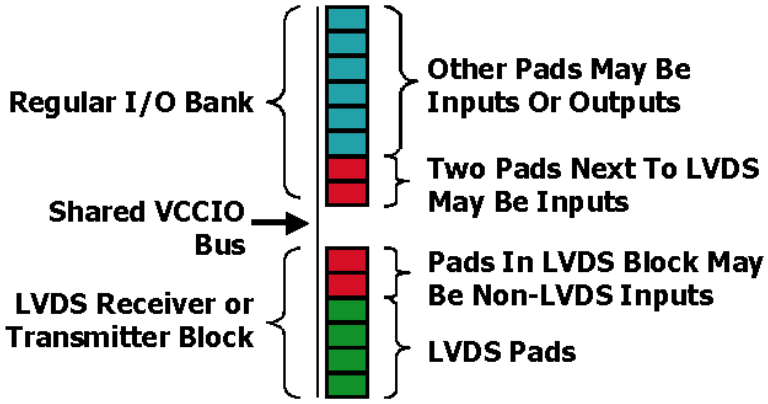


Guidelines for Selectable I/O Standards

The following guidelines should be used when designing for the selectable I/O standards in APEX 20KE devices. The guidelines define which standards are compatible based on input, output, and bidirectional types within an I/O bank.

- When an LVDS pin is used, non-LVDS output pins cannot be placed in or within two I/O pins of the LVDS receiver and transmitter blocks in the same I/O bank. This only applies for the neighboring I/O bank that shares the same VCCIO bus. Switching outputs on these pins could affect the LVDS pins and degrade performance. The only exception is the PLL LOCK pin, because it rarely changes. As shown in Figure 10, output pins must be at least 2 pads away from the LVDS receiver and transmitter blocks. The **Show Pads** view in the Floorplan Editor can be used to see the pad order.

Figure 10. I/O Pin Placement in the I/O Bank Adjacent to the LVDS Blocks



- No two input pins can be placed in the same I/O bank if their I/O standards require a different V_{REF} voltage. However, non-voltage-referenced standards can coexist with voltage-referenced standards; e.g. one bank can support GTL+ and LVTTL. For QFP packages, the two merged I/O banks still support separate V_{REF} inputs for each bank. For example, if bank 1 and bank 8 are merged together, bank 1 can support GTL+ while bank 8 can support SSTL-3.
- No two push-pull standard output pins can be placed in the same I/O bank if they require a different VCCIO voltage level. All output pins have the same VCCIO level for merged I/O banks in the QFP packages. GTL+ is an open-drain I/O standard and therefore can be assigned to I/O banks with a 2.5-V or 3.3-V VCCIO level.
- The clamp diode affects input tolerance. When the PCI clamp diode is turned on, an I/O pin is clamped to VCCIO. For example, a 2.5-V VCCIO bank without the clamp diode is tolerant to 3.3-V inputs. However, when the clamp is turned on, the 2.5-V VCCIO bank is not 3.3-V tolerant. An LVTTL input that does not have its clamp diode turned on can be placed in a bank that has a 2.5-V VCCIO level.
- Bidirectional pins have to satisfy both input and output guidelines.
- All output drivers between two GNDIO pins should not sink more current than 273 mA in total. Pins using the 1.8-V standard are not current limited. The current requirement for I/O standards with 3.3-V and 2.5-V VCCIO levels are defined as follows:

  For VCCIO = 3.3V,

  ((# of GTL+ * 36) + (# of LVTTL * I_{LVTTL}) + (# of PCI * 1.5) + (# of LVCMOS * I_{LVCMOS}) + (# of SSTL-3 class I * 8) + (SSTL-3 class II * 16) + (# of LVDS * 4.5) + (# of AGP * 1.5) + (# of CTT * 8)) mA <= 273 mA

  Where I_{LVTTL} (4 mA default value) and I_{LVCMOS} (0.1 mA default value) are the current sink on the LVTTL and LVCMOS pins, respectively. If your system requires higher I_{CC} for LVTTL or LVCMOS pins (for example, due to termination) then adjust the equation accordingly.

  For VCCIO = 2.5V,

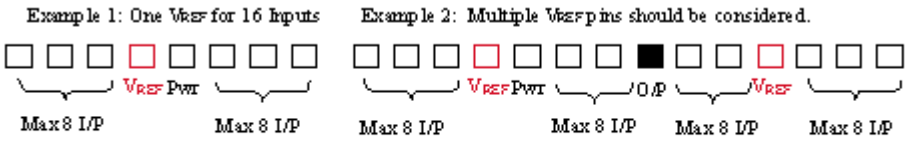
  ((# of 2.5V * 2) + (# of SSTL-2 class I * 7.6) + (# of SSTL-2 class II * 15.2) mA <= 273 mA

  In practice, this rule applies only to SSTL-2 Class II, SSTL-3 Class II, GTL+, and LVCMOS and LVTTL pins which can sink more than 14 mA per output pin. For other standards, every pin can be used without violating this requirement.

  The *APEX 20K Programmable Logic Device Family Data Sheet* shows the relationship of I/O pins to GNDIO pins to enable correct pin placement. This is also shown in the Quartus software's Floorplan Editor and in Quartus Help.

- When placing V_{REF} pins follow these guidelines. Output pins that can switch while an input is using a V_{REF} have to be placed a distance of 2 pads away from the V_{REF} pin, or a distance of 1 pad away from the V_{REF} pin if the pad between them is a power (VCC or GND) pad. Example 1 in Figure 11 shows both cases. Multiple V_{REF} pins may be used in an I/O bank that uses a voltage-referenced input standards, depending on the quantity and placement of the input pins as shown in Example 2 in Figure 11. Further V_{REF} guidelines are discussed in the "I/O & VREF Placement Guidelines" on page 13.

Figure 11. Examples of V_{REF} Placement



Automatic Placement & Verification of Selectable I/O Standards With Quartus

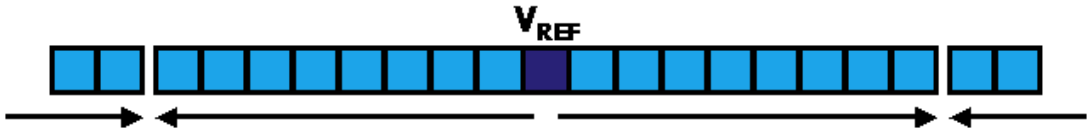
The Quartus software verifies correct placement of all I/O and VREF pins, following the same rules outlined in the Guidelines for Selectable I/O Standards section.

- Designers must assign VREF pins for all voltage-referenced I/O pins. Quartus automatically places I/O pins of different VREF standards without pin assignments in separate I/O banks.
- The Quartus software verifies that no two voltage-referenced I/O pins requiring different VREF levels are placed in one bank.
- The Quartus software ensures that an I/O pin requiring a VREF pin is no more than 16 pins from a VREF pin. All 16 voltage-referenced I/O pins may be placed on only one side of the VREF pin or staggered on both sides of the VREF pin.
- The Quartus software reports an error message if the current limitation is exceeded between `GNDIO` pins. It uses the equations documented in the "Guidelines for Selectable I/O Standards" on page 11.
- The Quartus software ensures that no more than 16 voltage referenced I/O standard pins are using a single VREF.
- The Quartus software does not allow you to place an output pin within two pins of a VREF if a power pin does not separate them. To view pad orientation, use the show pads view in the Floorplan Editor.
- The Quartus software will reserve the unused LVDS channels in the LVDS transmitter and receiver blocks when any of the LVDS channels are being used. It will also reserve the two I/O pins adjacent to the LVDS blocks that share a `VCCIO` pin with the LVDS blocks.
- The Quartus software will not allow placement of non-LVDS output pins in or within 2 I/O pins (with a common `VCCIO` pin) of the LVDS blocks.

I/O & V_{REF} Placement Guidelines

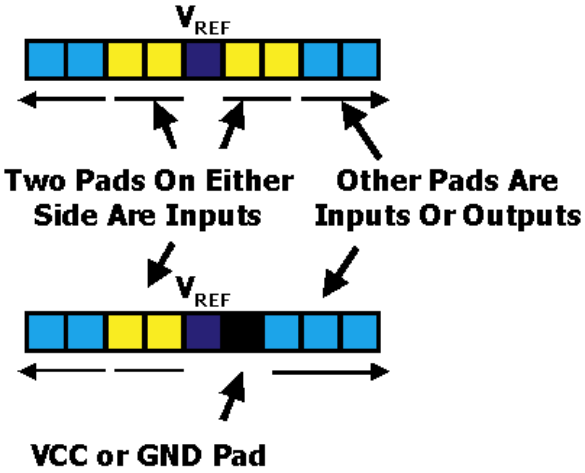
This section discusses V_{REF} and I/O pin placement guidelines when designing with I/O buses. Each V_{REF} pin can support up to 8 voltage-referenced input pins on each side, 16 input pins in total, as shown in Figure 12. The Quartus software will give an error message if a voltage-referenced input pin is placed more than 16 pads from a V_{REF} pin.

Figure 12. Each V_{REF} Can Support 16 Input Pins



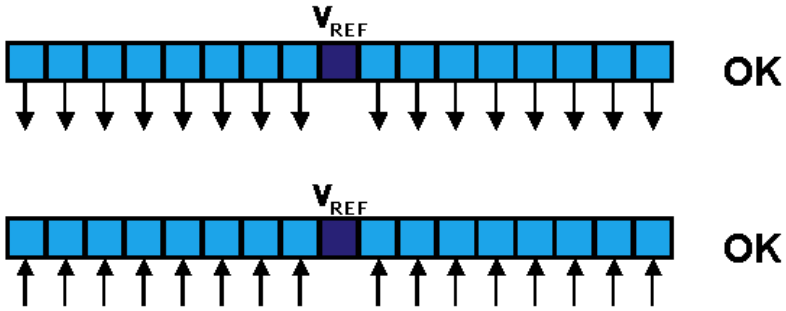
Output pins should be placed 2 or more pins away from V_{REF} pins, except when the V_{REF} is next to a power pin. In that case the power pin isolates the V_{REF} pin from the switching output. Output pins can be placed on the other side of the power pin, as shown in Figure 13.

Figure 13. V_{REF} Pin Placement Guidelines



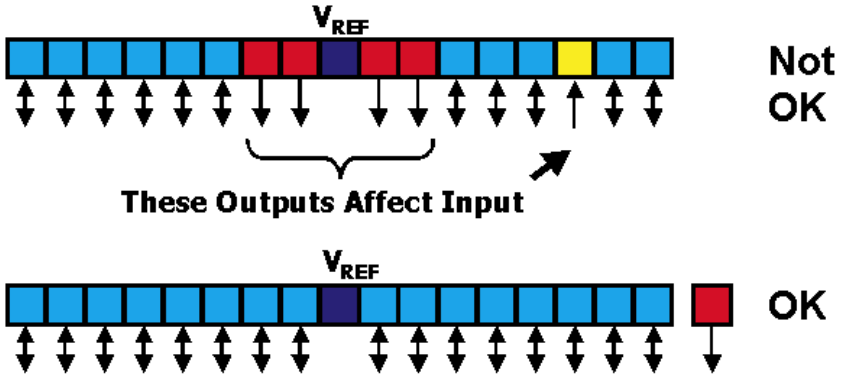
Voltage-referenced bidirectional buses that share a single tri-state control signal can be placed around the V_{REF} pin, as shown in Figure 14. This works because the bus is only operating in one direction at a time. When the bidirectional pins are driving out, no inputs are using the V_{REF} pin. When the bidirectional pins are accepting input signals, there are no output pins that would interfere with the input pins' ability to use the V_{REF} level.

Figure 14. Placement of Bidirectional Buses with Single OE Control



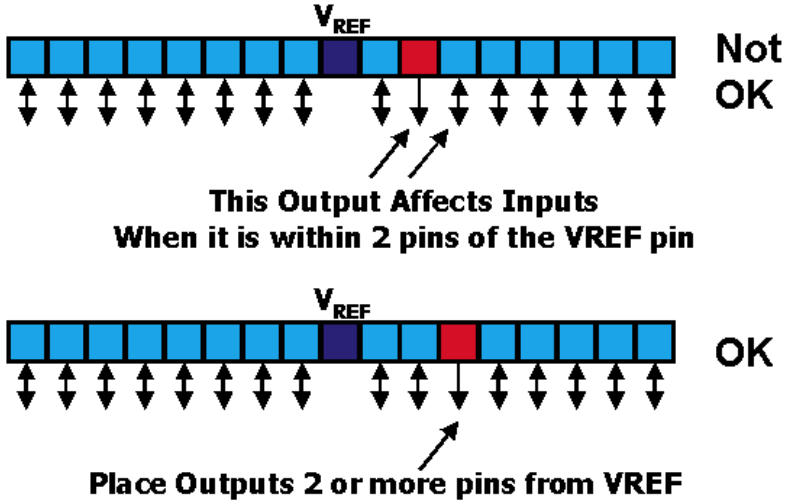
Output pins can be placed outside the bus without affecting the use of V_{REF} in the bidirectional bus, as shown in Figure 15. Furthermore, an unrelated output pin may be placed within a voltage-referenced bidirectional bus if the output pin is more than two pads from the V_{REF} pin or separated by a power pin.

Figure 15. Placement of Output Pins Outside the Bidirectional Buses



Output pins can also be placed inside the bus if they are more than two pins away from the V_{REF} pin, as shown in Figure 16.

Figure 16. Output Pin Placement in a Bidirectional Bus



Summary

The APEX 20KE devices support 13 programmable I/O standards, allowing customization for a wide variety of applications. Input, output, and bidirectional pins of different I/O standards can be intermixed with I/O banks by following the guidelines in this document.

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