White Paper

Using LVDS in APEX 20KE Devices

Introduction

New designs continually demand more bandwidth. To address this need, Altera has added low-voltage differential signaling (LVDS) technology to the APEX™ device family. LVDS meets new requirements for high data rates and low power consumption.

With LVDS, one chip can interface with high-speed, low-voltage backplanes or data channels. Board design can be simplified because dedicated circuitry like LVDS is now integrated into the PLD. LVDS integration saves board space, reduces pin usage, and improves performance.

This white paper explains the advantages and describes how to use LVDS technology on APEX 20KE devices.

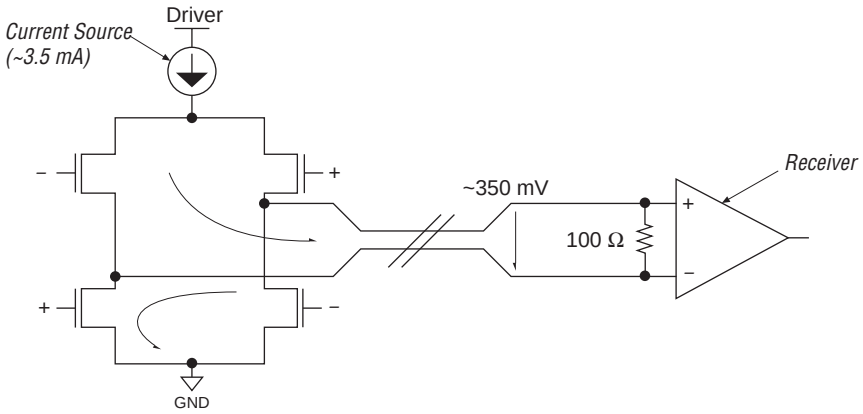
LVDS Standards

Two key industry standards define LVDS: IEEE Std. 1596.3 SCI-LVDS and ANSI/TIA/EIA-644. Both standards have similar features, but the IEEE Std. 1596.3 SCI-LVDS standard supports a maximum data transfer rate of 250 million bits per second (Mbps). APEX 20KE devices are designed to meet the ANSI/TIA/EIA-644 standard at up to 624 Mbps.

ANSI/TIA/EIA-644

The ANSI/TIA/EIA-644 standard defines driver output and receiver input characteristics. Additionally, this standard recommends a maximum data rate of 655 Mbps and a theoretical maximum of 1.923-gigabits per second (Gbps), based on a loss-less media. It also documents fail-safe operation of the receiver under fault conditions. Figure 1 shows how the current-mode LVDS driver works.

Figure 1. LVDS Current Mode Driver



Low-Voltage Differential Signaling

LVDS is a low voltage swing, general-purpose I/O standard that has high-speed, low-power, and low-noise advantages. LVDS is capable of extremely high data transfer across a variety of interconnect media: PCB traces, backplanes, and cables. LVDS utilizes a differential input without the need of an input reference voltage. Typical uses for LVDS are high-bandwidth data transfer, backplane driver, and clock distribution applications.

The faster the transition time (i.e., edge rate), the higher the potential data rate. To provide switching speeds in the hundreds-of-Mbps range, the LVDS standard typically has a low-voltage signal level of 350 mV. Since there is little margin for noise with a swing that small, a differential data transmission scheme is used.

Differential transmission means that every LVDS signal uses two lines. The voltage difference between the two lines defines the logic state of the LVDS signal. For each signal pair, there is the true signal denoted as LVDSRX<*number*>, and the complement signal denoted as LVDSRX<*number*>a where the channel number ranges from 1 to 16. The differential signal for channel 1 is LVDSRX01 minus LVDSRX01a.

For more information on the LVDS naming convention refer to the *Using I/O Standards in the Quartus Software White Paper.*

The differential scheme has two key advantages over single-ended schemes:

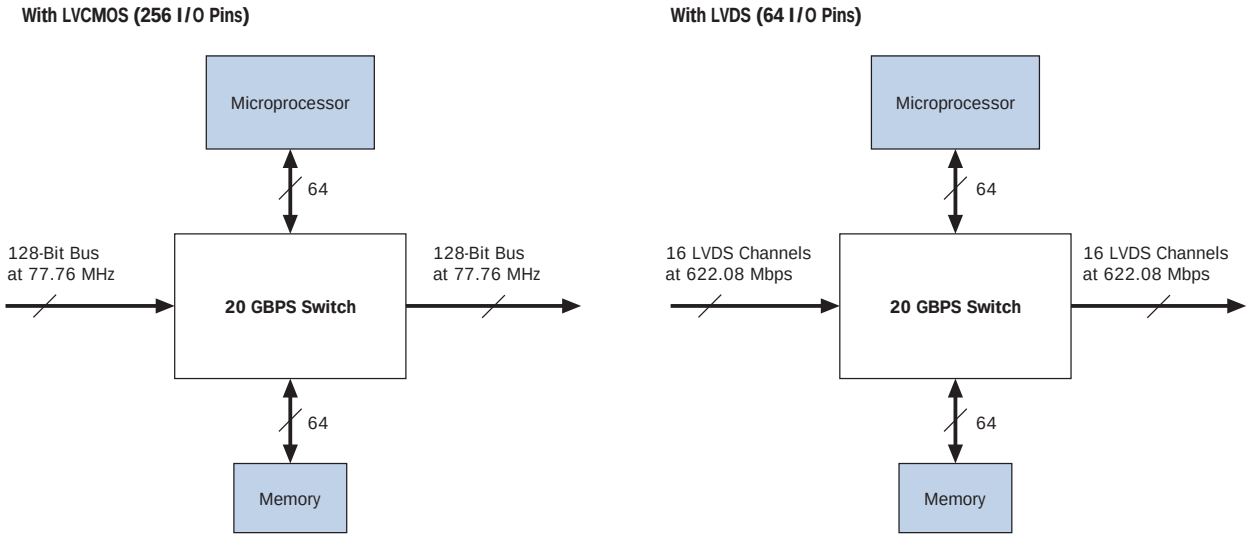
- The low-voltage swing reduces power consumption and increases performance
- Less susceptible to electromagnetic interference (EMI)

Increased Performance

Low voltage swing is important for high performance. To provide switching speeds in the hundreds of Mbps range, the LVDS standard defined a low-voltage signal level of 350 mV. The smaller the voltage swing, the faster a signal can change logic levels. The faster the transition time (i.e., edge rate), the higher the potential data rate. Since there is little margin for noise with a small voltage swing, a differential data transmission scheme is used. The two signals are referenced to each other, not to GND or another static signal level. Therefore, a differential standard can have a much smaller switching region.

The same bandwidth for a LVCMOS data bus can be achieved with LVDS using 4x fewer pins by operating the LVDS signals at 8x the frequency. Figure 2 shows a 128-bit LVCMOS data bus that can be implemented with 16 LVDS channels (32 pins).

Figure 2. LVDS uses 4x Fewer Pins than LVCMOS



Power-Efficiency

LVDS is a power-efficient standard. Because of the low-switching voltage (typically 350 mV) and a DC current of 3.5 mA per channel, the AC power dissipation per signal is small. Table 1 shows the equations that calculate the load power dissipation.

Table 1. Calculating the Load Power Dissipation

Calculation	Equation	Example
DC power per channel (P_{DC})	($P_{DC} = V \times I$)	350 mV × 3 mA = 1.225 mW
AC power per channel (P_{AC})	($P_{AC} = 2CV^2F$)	2 x 8pF x $(0.35V)^2$ x 311 MHz = 0.610 mW
Total Power	$P_{AC} + P_{DC}$	1.225 mW + 0.610 mW = 1.835 mW

To understand how LVDS power consumption compares to LVTTL, consider the following example in which both LVDS and LVCMOS are operating at a 622.08 Mbps bandwidth. The comparison is shown in Table 2.

Table 2. LVDS Consumes Less Power than CMOS

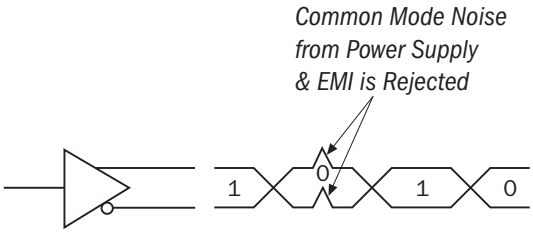
Parameter	LVDS	LVCMOS	Unit
Number of Pins/Channels	1 channel	8 pins	-
Frequency	622.08	77.76	MHz
Bandwidth	622.08	622.08	MBPS
Data Voltage Swing	0.35	3.3	V
Power Per Pin	-	3.387	mW
Total Power	1.835	27.09	mW

Reduced Electromagnetic Interference (EMI)

Electromagnetic interference (EMI) is radiated noise created from the acceleration of electric charge within a device and across the transmission medium between devices. Device-generated EMI is dependent on frequency, output voltage swing, and slew rate. Due to the low voltage swing of the LVDS standard, the EMI effects are much smaller than CMOS, TTL, or other I/O standards. Reduced EMI effects is a major advantage of using the LVDS standard.

Furthermore, LVDS is less susceptible to common-mode noise because it is a differential standard. Figure 3 shows that system and power supply noise is equally coupled to both LVDS signals, thus not affecting signal quality.

Figure 3. System Level Noise Rejection

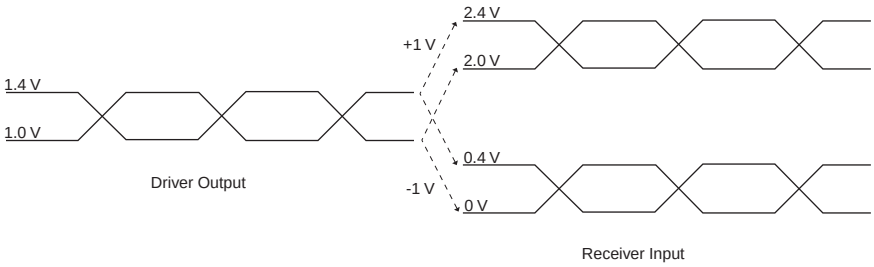


Common Mode Range

An LVDS receiver can tolerate a maximum of ±1 V ground shift between the driver and the receiver ground. The recommended input voltage ranges from 0.0 V to 2.4 V. Because the typical voltage offset is 1.2 V, the common mode range of the receiver is 0.2 V to 2.2 V. The LVDS driver will have an output voltage swing between 1.4 V and 1.0 V, with respect to ground. When there is a +1 V ground shift, the voltage swing ranges from 2.4 V to 2.0 V, which is

within the input voltage range. Similarly, if there is a –1.0 V shift, the output voltage swing ranges from 0.0 V to 0.4 V. Figure 4 shows the ground shift tolerance.

Figure 4. Common Mode Voltage Range



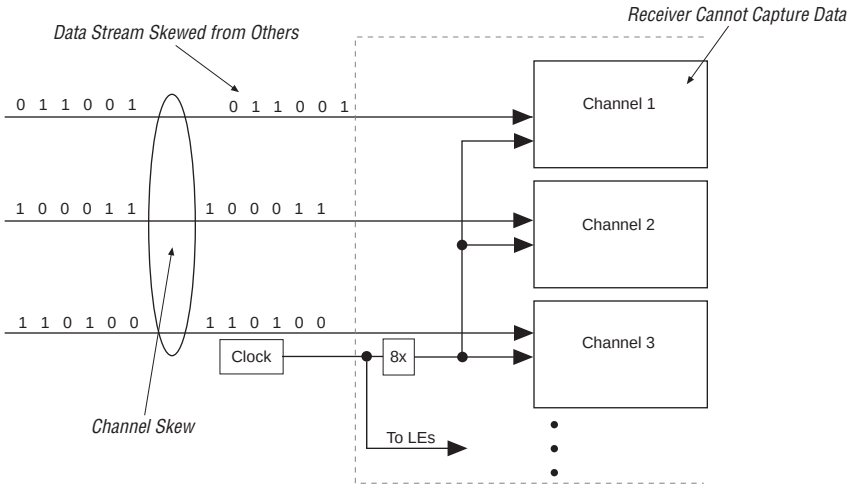
LVDS Timing

This section discusses the timing waveforms and parameters for LVDS in APEX 20KE devices. APEX 20KE devices incorporate deskew circuitry, which ensures successful data capture at high rates when the LVDS PLL is used in 7x or 8x modes. For designs using the LVDS PLL in 4x mode, the deskew circuitry is not required.

Deskew Circuitry

The deskew circuitry is implemented inside the APEX 20KE device to compensate for board skew and clock skew within the APEX 20KE devices, as shown in Figure 5.

Figure 5. Channel-to-Channel and Clock-to-Channel Skew



APEX 20KE devices use deskew circuitry to provide high-data transfer rates. Because LVDS inputs have a high bandwidth, an over-sampling circuit is used to accurately capture the data. The inputs are captured by four separate clocks, and the results are examined to determine which clock successfully captured the data.

The deskew circuitry can compensate up to ± 25% the bit time period.

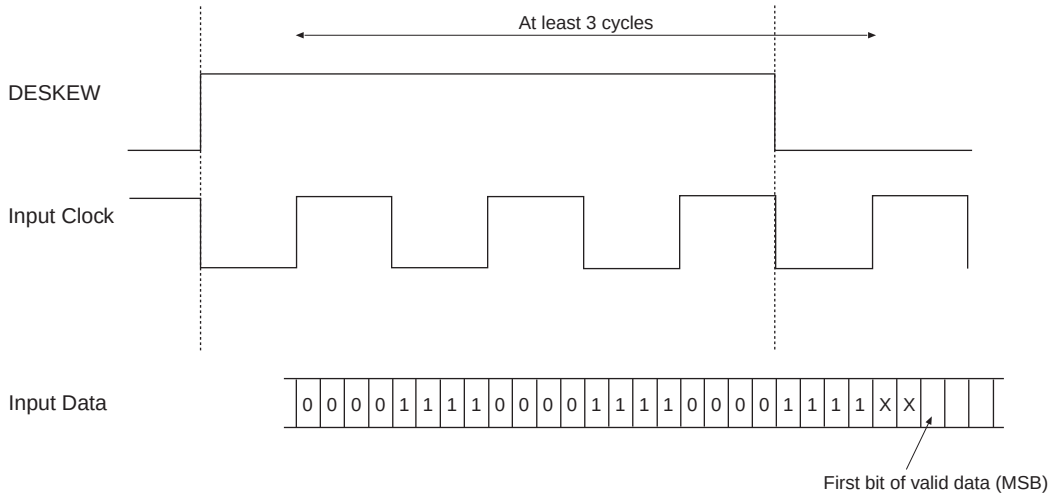
A calibration pattern is required to phase align the clock with the incoming LVDS data. The calibration data values depend on the operating mode of the LVDS phase-locked loop (PLL). Contrary to user mode data, the first bit of the calibration data is the first bit after the input clock. The calibration data is shown in Table 3.

Table 3. Calibration Data Pattern for Deskew Circuitry

LVDS ClockBoost™ Multiplication Rate	Calibration Pattern
4	0011
7	0000111
8	00001111

A dual-function DESKEW pin places the LVDS inputs in calibration mode. The calibration pattern must be applied for three input clock cycles (see Figure 6). The deskew pin should be controlled by the falling edge of the input clock. All channels are calibrated simultaneously. Each LVDS input channel can independently align the clock with the received data to account for differences in routing. After all channels have been successfully calibrated, the LVDS data pins are ready to transmit and receive data.

Figure 6. Deskew Circuitry Calibration Waveform for 8x Mode

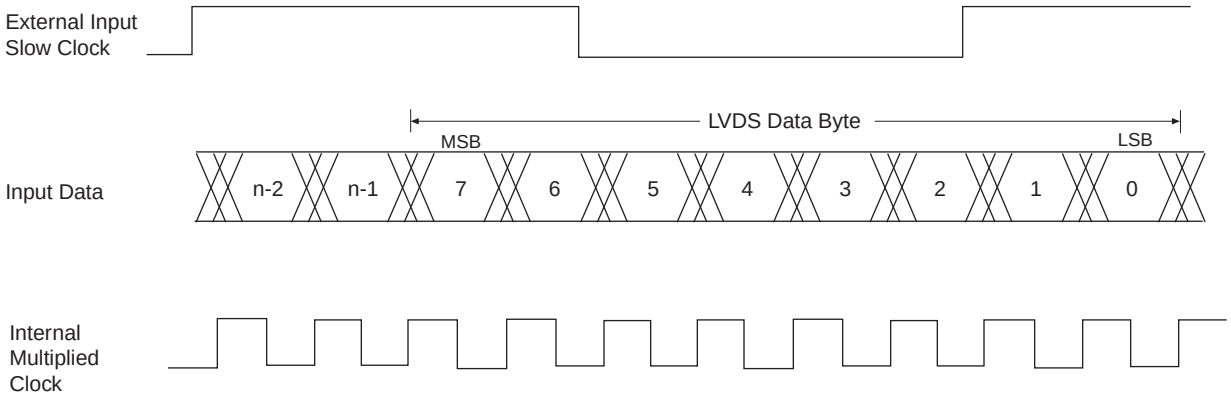


Changes in temperature and voltage can affect the receiver input skew margin (RSKM). RSKM is the tolerance of the difference between the input clock and the input data. For LVDS in x8 mode, deskew is only required if the worst case board skew between clock and data channels is more than 0.3 ns. The deskew circuitry needs to be recalibrated often enough to satisfy the RSKM specification of ± 0.7ns. An analysis of the circuit must be performed to determine if the RSKM specification is violated.

Timing Budget and Definitions

Data synchronization is necessary for successful data transmission with LVDS at high frequencies. For operation at 622.08 MBPS, the external clock is multiplied by 8 and phase aligned by the PLL to coincide with the sampling window of each data bit. Figure 7 shows the data bit orientation defined in the altlvds_rx megafunction in the Quartus software for the 8-to-1 data conversion mode.

Figure 7. Internal Data Synchronization



The internally-generated PLL clock is positioned to meet the requirements of the timing budget. Figure 8 shows the timing budget that is available for capturing serial data at 622.08 MHz.

Figure 8. LVDS Timing Budget

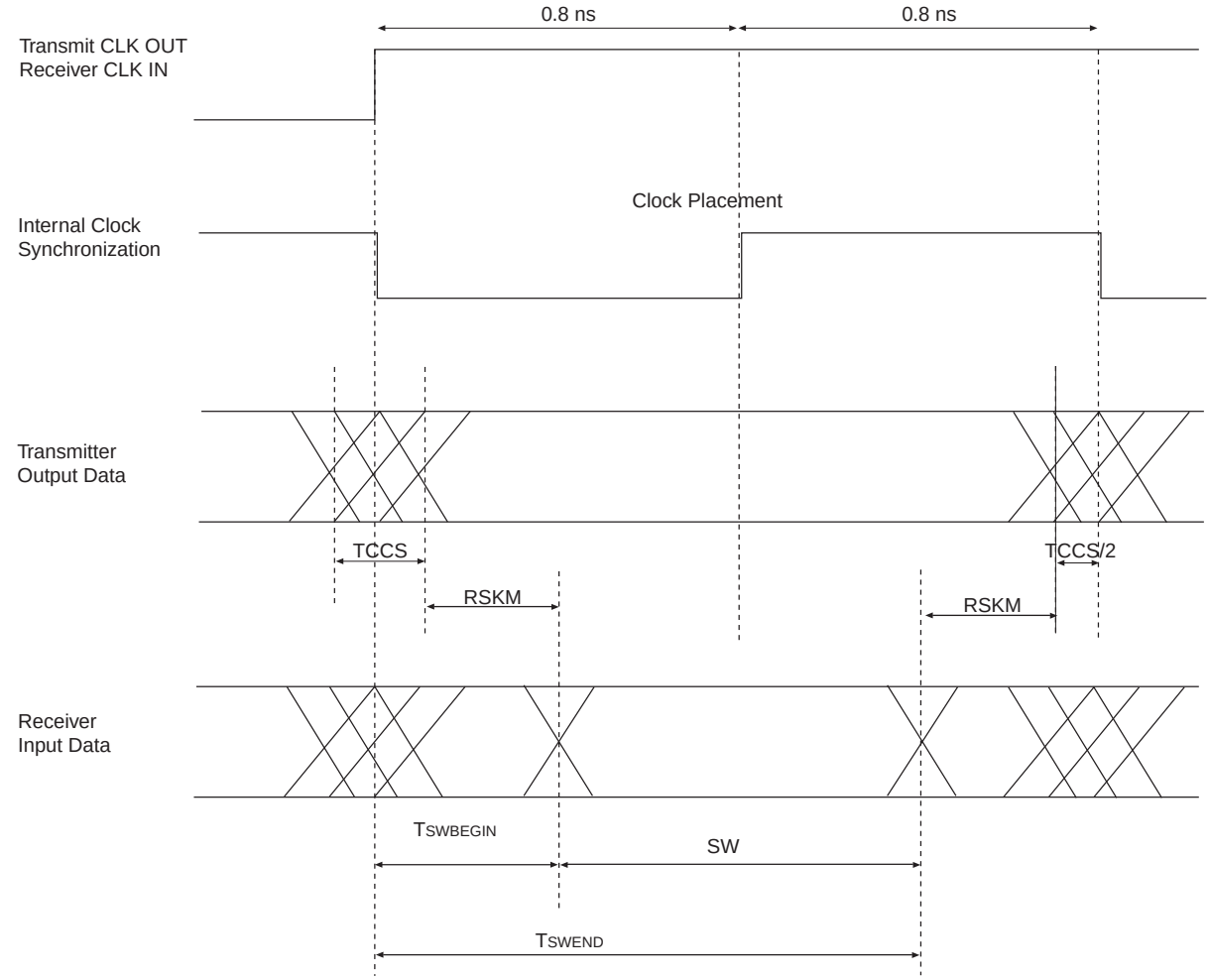


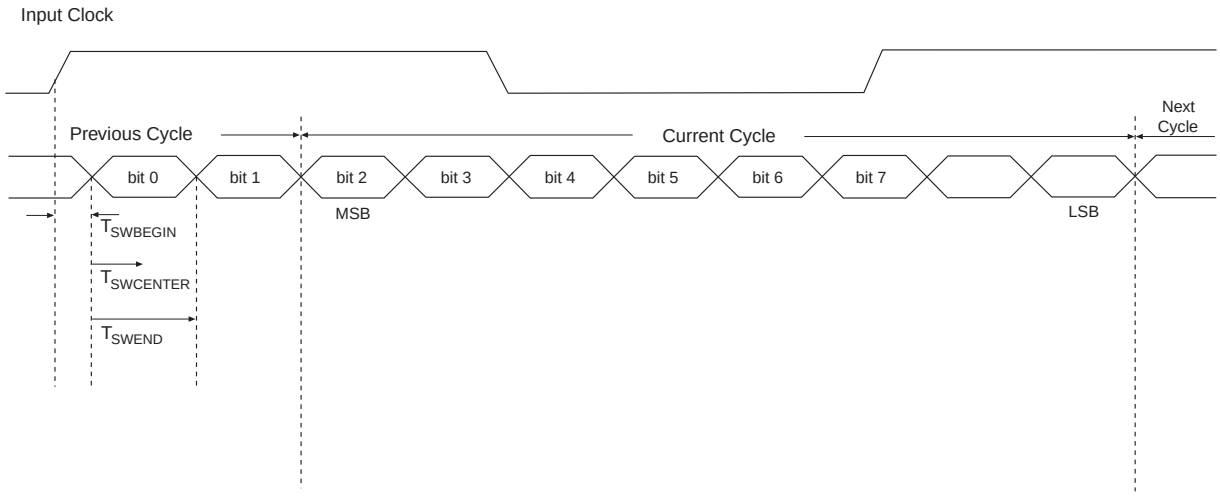
Table 4 shows the LVDS timing specifications and terminology.

Table 4. LVDS Timing Specifications and Terminology

LVDS Timing Specification	Terminology
Sampling Window (SW)	This parameter defines the window where the internal receiver PLL clock rising edge should be placed to capture data. The setup and hold times determine the ideal strobe position within the sampling window. The input data must be valid in the sampling window. ($T_{SW} = T_{SWEND} - T_{SWBEGIN}$)
Begin Sampling Window ($T_{SWBEGIN}$)	This parameter defines the beginning of the sampling window for each bit in a word of data. From the beginning to end of the sampling window the input data must be valid to meet setup and hold time requirements.
End Sampling Window (T_{SWEND})	This parameter defines the end of the sampling window for each bit in a word of data. From the beginning to end of the sampling window the input data must be valid to meet setup and hold time requirements.
Channel-to-Channel Skew (T_{CCS})	The channel-to-channel skew is defined as the timing difference between fastest and slowest output edges, including t_{CO} variation and clock skew. Skew is the variation in arrival time of two signals specified to arrive at the same time. The skew occurs on the registered output pins because of the differences in propagation delay of the clock signal through the clock network.
Receiver Input Skew Margin (RSKM)	Receiver input skew margin is the timing margin between clock input and data input for user board design, which allows LVDS cable skew, and jitter on the LVDS PLL. RSKM = (Bit Time Period – TCCS – SW)/2.
Bit Time Period	The bit time period is the period of the internal receiver LVDS PLL divided by its multiplication ratio. This is the timing budget allowed for skew, propagation delays, and data sampling window (Bit Time Period = 1/(Receiver Input Clock Frequency x Multiplication Factor)).

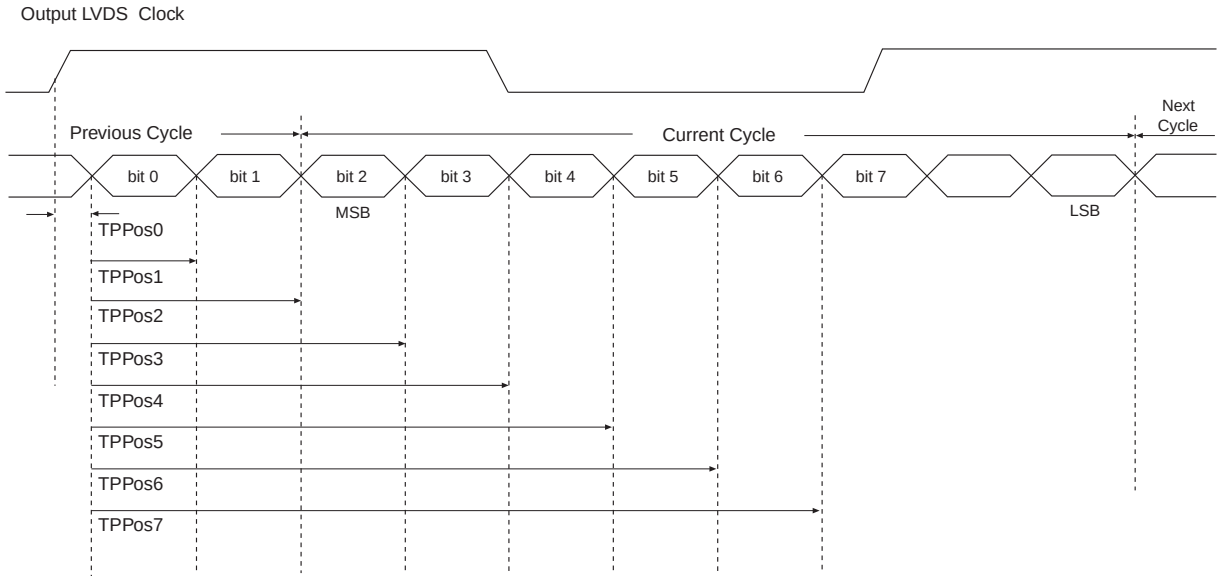
The input timing waveform is shown in Figure 9. The two bit cycle phase delay from the input clock to the input data is to account for clock insertion delay. The clock insertion delay is the delay from the clock input pin to the arrival of the rising edge at the LVDS conversion circuitry.

Figure 9. Input Timing Waveforms



The output timing waveform in Figure 10 shows the relationship between the output LVDS clock and the serial output data stream.

Figure 10. Output Timing Waveforms



The Sampling Window

For these internally-generated LVDS PLLs to be properly phase-aligned at the serial-to-parallel converter for data capture, the data sampling window must be properly positioned with respect to the clock.

Tables 5 through 10 show the sampling window positions for 8-to-1, 7-to-1, and 4-to-1 data conversion modes.

Table 5. 8-to-1 Mode Receive Window (622.08 Mbps transfer)

Symbol	$T_{SWBEGIN}$	$T_{SWCENTER}$	T_{SWEND}	Units
Bit 0	0.50	0.80	1.10	ns
Bit 1	2.11	2.41	2.71	ns
Bit 2	3.72	4.02	4.32	ns
Bit 3	5.33	5.63	5.93	ns
Bit 4	6.93	7.23	7.53	ns
Bit 5	8.54	8.84	9.14	ns
Bit 6	10.15	10.45	10.75	ns
Bit 7	11.76	12.06	12.36	ns

Table 6. 8-to-1 Mode Transmitter Pulse Positions (622.08 Mbps transfer)

Symbol	Min	Typ	Max	Units
TPPos0	-0.20	0.00	0.20	ns
TPPos1	1.41	1.61	1.81	ns
TPPos2	3.02	3.22	3.42	ns
TPPos3	4.62	4.82	5.02	ns
TPPos4	6.23	6.43	6.63	ns
TPPos5	7.84	8.04	8.24	ns
TPPos6	9.45	9.65	9.85	ns
TPPos7	11.05	11.25	11.45	ns

Table 7. 7-to-1 Mode Receive Window (462 Mbps transfer)

Symbol	$T_{SWBEGIN}$	$T_{SWCENTER}$	T_{SWEND}	Units
Bit 0	0.73	1.08	1.43	ns
Bit 1	2.90	3.25	3.60	ns
Bit 2	5.06	5.41	5.76	ns
Bit 3	7.23	7.58	7.93	ns
Bit 4	9.39	9.74	10.09	ns
Bit 5	11.55	11.90	12.25	ns
Bit 6	13.72	14.07	14.42	ns

Table 8. 7-to-1 Mode Transmitter Pulse Positions (462 Mbps transfer)

Symbol	Min	Typ	Max	Units
TPPos0	-0.35	0.00	0.35	ns
TPPos1	1.81	2.16	2.51	ns
TPPos2	3.98	4.33	4.68	ns
TPPos3	6.14	6.49	6.84	ns
TPPos4	8.31	8.66	9.01	ns
TPPos5	10.47	10.82	11.17	ns
TPPos6	12.64	12.99	13.34	ns

Table 9. 4-to-1 Mode Receive Window (320 Mbps transfer)

Symbol	$T_{SWBEGIN}$	$T_{SWCENTER}$	T_{SWEND}	Units
Bit 0	1.06	1.56	2.06	ns
Bit 1	4.19	4.69	5.19	ns
Bit 2	7.31	7.81	8.31	ns
Bit 3	10.44	10.94	11.44	ns

Table 10. 4-to-1 Mode Transmitter Pulse Positions (320 Mbps transfer)

Symbol	Min	Typ	Max	Units
TPPos0	-0.4	0.0	0.4	ns
TPPos1	2.73	3.13	3.53	ns
TPPos2	5.85	6.25	6.65	ns
TPPos3	8.98	9.38	9.78	ns

LVDS Specifications

Table 11 shows the recommended operating conditions for the LVDS I/O block.

Table 11. 3.3-V LVDS I/O Specifications

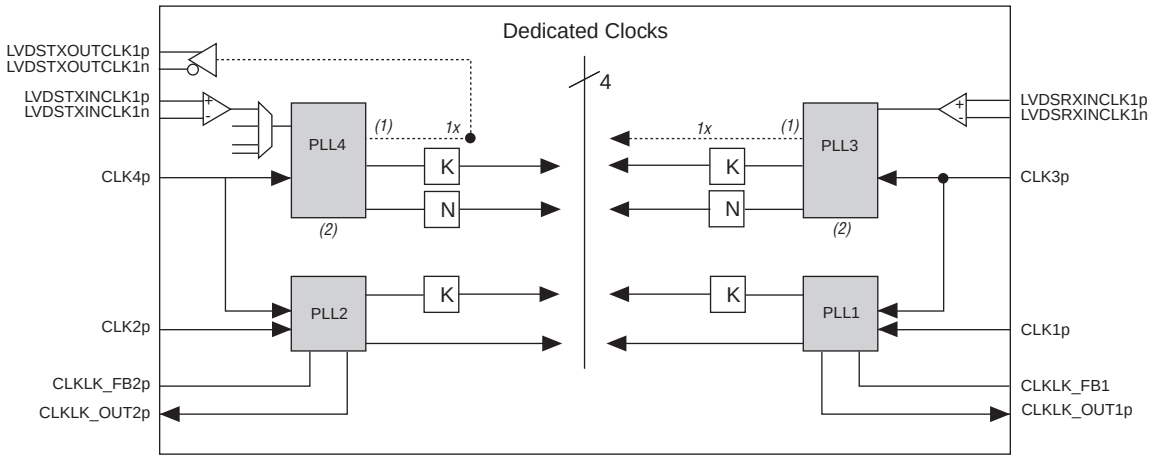
Symbol	Parameter	Conditions	Min	Typical	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffers		1.7	1.8	1.9	V
V_{CCIO}	Supply voltage		3.0	3.3	3.6	V
V_{OD}	Differential output voltage	RL = 100 Ω	250		450	mV
ΔV_{OD}	Change in VOD between H and L	RL = 100 Ω			50	mV
V_{OS}	Output offset voltage	RL = 100 Ω	1.125	1.25	1.375	V
ΔV_{OS}	Change in VOS between H and L	RL = 100 Ω			50	mV
V_{TH}	Differential Input threshold	VCM = 1.2 V	-100		100	mV
R_L	Receiver differential input resistor		90	100	110	W

Data Conversion Modes

The PLL is the key to successful transmission of the high data rates supported by LVDS. The PLL minimizes skew, and phase-aligns the clock at the parallel-to-serial and serial-to-parallel data converters.

In EP20K300E and larger devices, two of the ClockLock™ PLLs can be configured for use in the LVDS I/O interfaces. One LVDS PLL is used for the input block, and another is used for the output block. Figure 11 shows a block diagram of the APEX 20KE LVDS PLLs, including LVDS-specific pin names.

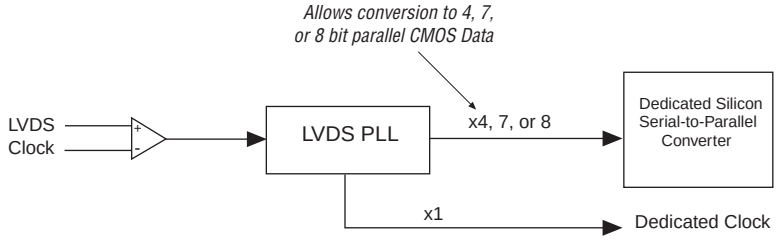
Figure 11. LVDS PLL Block Diagram



Notes:
(1) These PLL outputs are only used in LVDS mode.
(2) PLL3 and PLL4 can only be used for LVDS or as a general-purpose PLL.

When using LVDS, these clocks can be multiplied to support high-speed data transfer rates and convert between LVDS and CMOS data. You can multiply the input clock by 4, 7, or 8 for use in the dedicated data conversion circuitry. A general-purpose PLL should be used for LVDS in bypass mode. Figure 12 shows the connections to the LVDS PLL on the receiver side.

Figure 12. LVDS PLL Block Diagram



An LVDS PLL is used to boost the LVDS input clock from 77.76 MHz to 622.08 MHz for internally clocking the LVDS data. The PLL also phase-aligns the clock with the incoming data.

The incoming serial LVDS channels can either use or bypass the serial-to-parallel converter. The parallel converter can operate in different data-conversion modes (e.g., 8-to-1, 7-to-1, 4-to-1). When operating in 1-to-1 mode, the dedicated LVDS circuitry is bypassed, and the data directly feeds the LEs. The 1x generated clock from the LVDS

PLL can also be used to clock internal logic within the device. Figure 13 shows the block diagram of the LVDS input circuitry.

Figure 13. Dedicated LVDS Receiver Circuitry Block Diagram

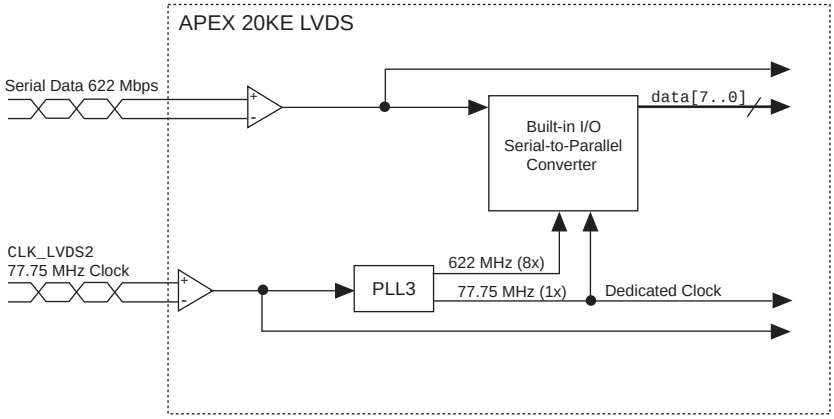
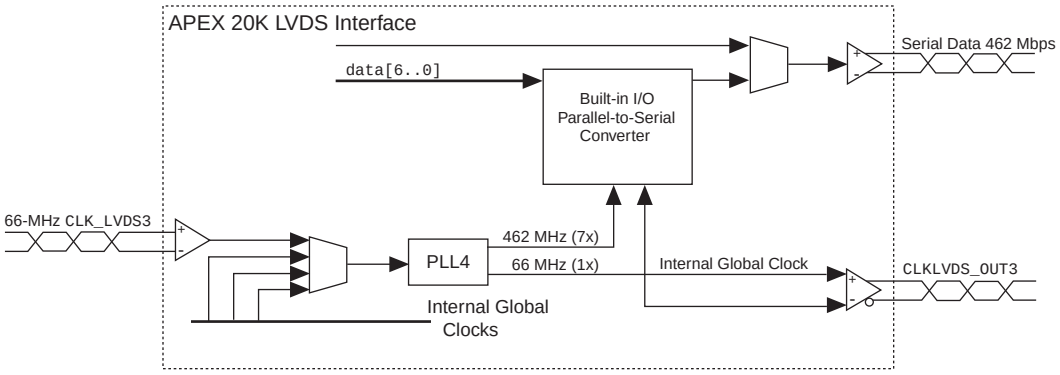


Figure 14 shows a block diagram of the LVDS output circuitry. The transmitter PLL can be driven externally or by the output of the receiver PLL via an internal global. The output of the transmitter PLL can be driven off-chip to clock other LVDS devices in the system.

Figure 14. Dedicated LVDS Transmitter Circuitry Block Diagram

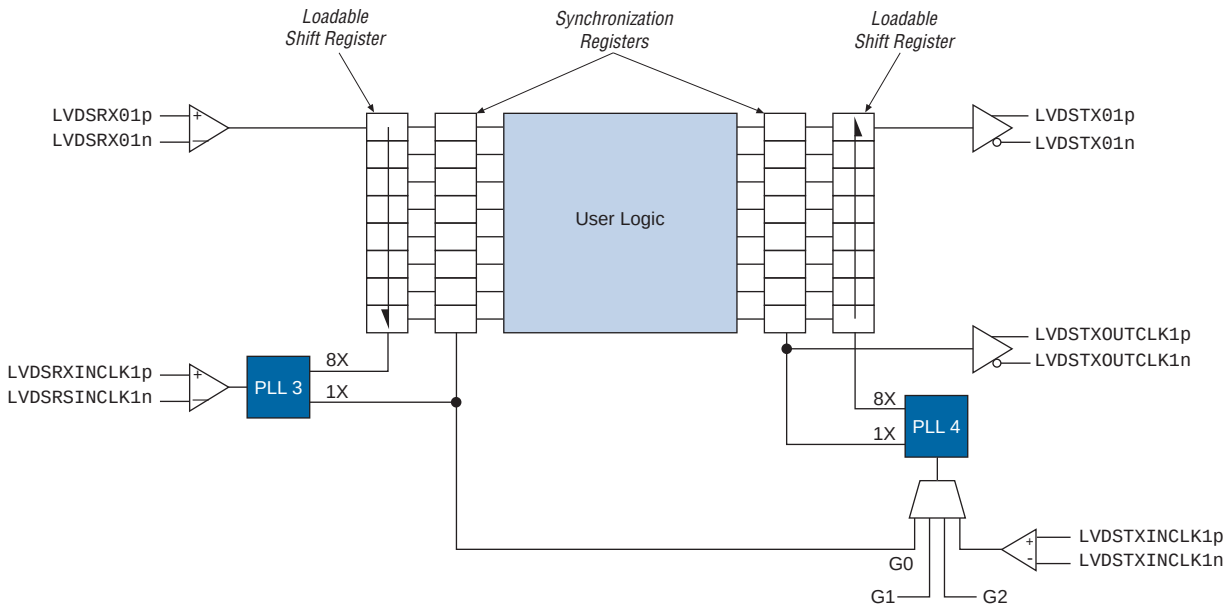


For more information on ClockLock and ClockBoost, refer to *Application Note 115 (Using the ClockLock & ClockBoost Features in APEX Devices)*.

LVDS Interface

Figure 15 shows how the LVDS receiver and transmitter internally interface with the logic and other devices in the system. There are 16 input LVDS channels in the input block, with an LVDS PLL used to clock the serial-to-parallel converter in the receiver. Two PLLs (PLL 3 for the receiver and PLL 4 for the transmitter) generate phase-locked clock signals for the serial-to-parallel and parallel-to-serial data converters. The receiver has 16 input channels, and the transmitter has 16 output LVDS channels. The LVDS receiver converts a maximum of 16 LVDS signals into 128 CMOS data bits, which feeds internal LEs within the device. Similarly, the LVDS transmitter converts a maximum of 128 CMOS on-chip data bits into 16 LVDS data streams, using an 8-to-1 parallel-to-serial converter.

Figure 15. LVDS Receiver and Transmitter Interface



The internal LVDS PLL clocks have an 8× maximum multiplication rate. The LVDS transmitter has the ability to drive the 1× locked PLL clock off-chip. The external transmitter clock output and output data signals are in-phase. Every cycle of transmit and receive clock data—up to 128 bits of input and output data—are sampled via the 16 LVDS I/O channels.

The LVDS input pins are row pins located on the right side of the device. Each LVDS input channel interfaces with dedicated shift registers and drive row lines. Similarly, the LVDS output pins are also row pins located on the left side of the device. Each LVDS output channel interfaces with dedicated shift registers, driven by peripheral logic elements (LEs).

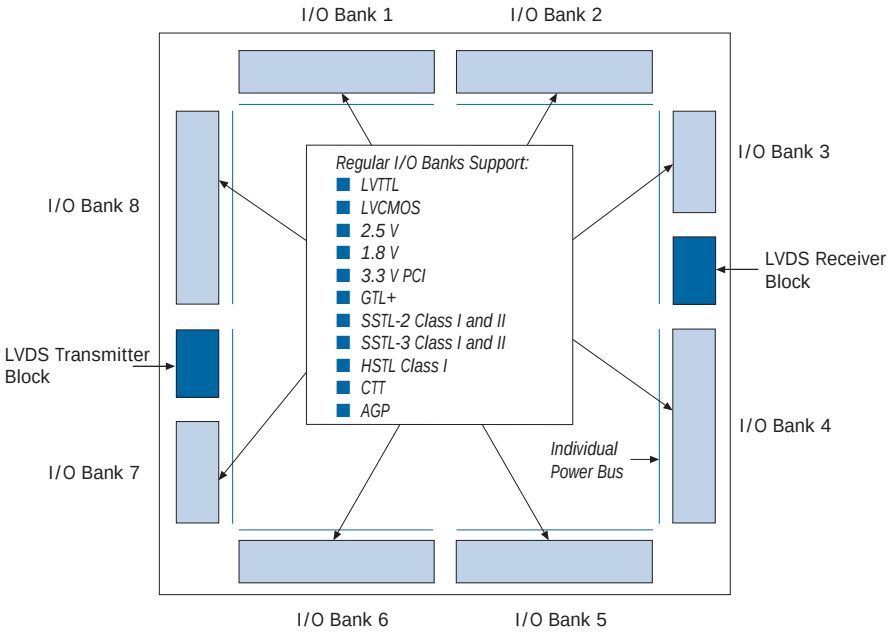
APEX 20KE I/O Structure

APEX 20KE devices have eight programmable I/O banks and two dedicated LVDS I/O blocks. Figure 16 shows a representation of the APEX 20KE I/O banks. The LVDS receiver block is located on the right, and the transmitter block is located on the left.

APEX 20KE devices EP20K400E and larger support using LVDS on dedicated clock signals, LVDS data in bypass (x1) mode, and dedicated serializer and deserializer in x4, x7, and x8 modes. The EP20K400E and larger devices with an x-suffix in their ordering codes support LVDS in x4, x7, and x8 modes. The EP20K300E devices, which do not have an x-suffix in their ordering codes, support using LVDS on dedicated clock signals and LVDS data in bypass (x1) mode in the 652-pin ball-grid array (BGA) and 672-pin FineLine BGA™ packages.

The EP20K200E and smaller devices support using LVDS on dedicated clock signals. For the EP20K200E and smaller devices, the x-suffix indicates PLL-enabled support. All APEX 20KE devices, including devices without an x-suffix in their ordering codes, support LVDS on dedicated clocks.

Figure 16. APEX 20KE I/O Blocks



The LVDS transmitter and receiver blocks support all of the I/O standards and can be used as input, output, or bi-directional pins at 3.3-V, 2.5-V, and 1.8-V. The first two I/O pins that border the LVDS blocks are input only to maintain an acceptable noise level on the V_{CCIO} plane.

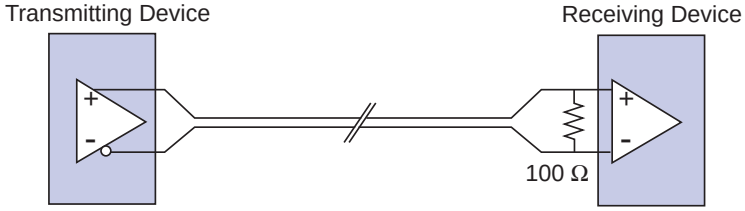
The programmable input/output element (IOE) blocks have individual power planes with separate VCCIO pins for each I/O bank. The V_{CCIO} planes support 3.3-V, 2.5-V, and 1.8-V levels. If the I/O pins are used for LVDS I/O standards, always connect the LVDS power bus-associated VCCIO pins to 3.3 V. The two LVDS I/O blocks support all of the standards supported by APEX 20KE devices.

When not using LVDS, power can be conserved by powering-down the LVDS VCCIO power pins. The LVDS blocks have their own VCCIO pins.

Board Termination

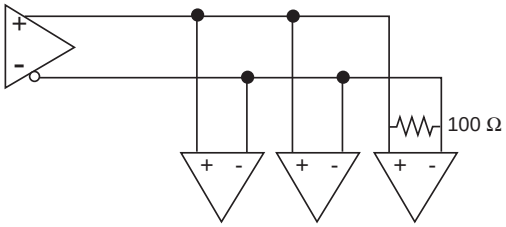
The LVDS I/O standard requires a termination resistor between the signals at the receiver side. This termination resistor generates the differential output voltage (V_{OD}) across the resistive termination load at the receiver input. The termination resistor should match the differential load impedance of the bus (typically 100 Ω, but the values may range between 90 Ω and 110 Ω). Figure 18 shows LVDS board termination at the receiver.

Figure 17. LVDS Board Termination at the Receiver



For multi-drop configurations where one transmitter drives multiple receivers, only one termination resistor is allowed, and it should be placed at the furthest receiver from the transmitter device, as shown in Figure 18.

Figure 18. Multi-Drop Configuration Termination



LVDS Design Recommendations

Because of the high data rates used with LVDS, skew can be a problem. To prevent skew and maintain signal integrity, follow the recommendations below:

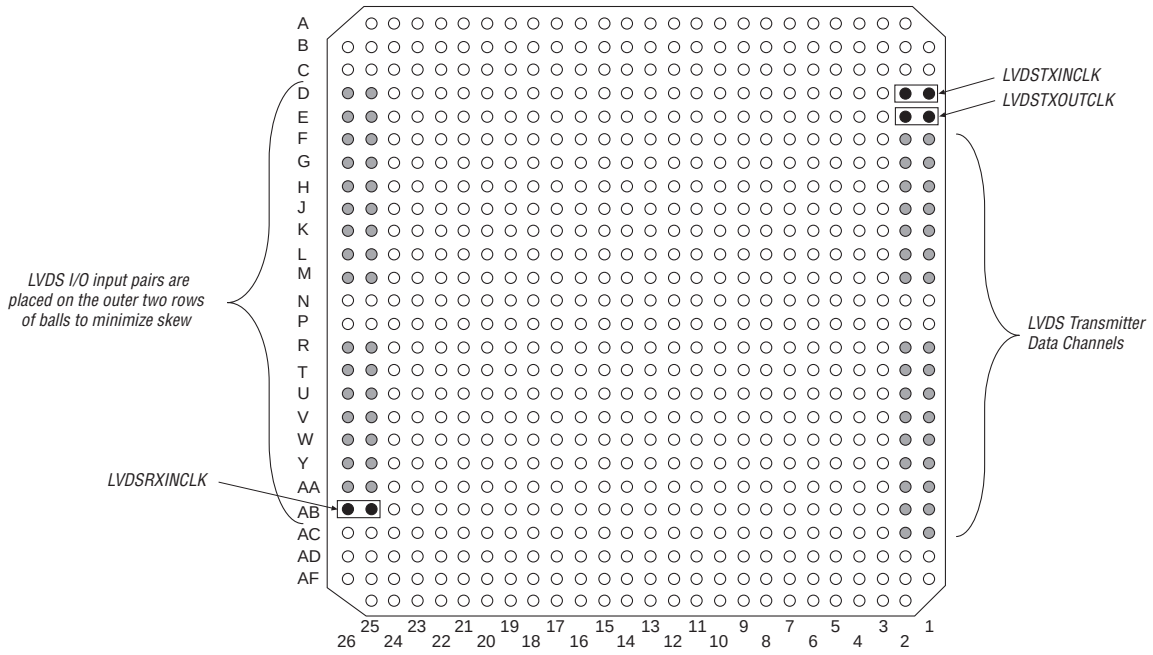
- Stub lengths must be kept less than 12mm (0.5 in)
- Place drivers and receivers as close to connectors as possible
- Match the electrical lengths of all bus LVDS lines to avoid skew
- Minimize the distance between traces of a pair of LVDS lines to maximize CMRR
- Separate TTL/CMOS signals from LVDS signals onto different board layers
- Use a multi-layer printed circuit board (PCB) with ground plane beneath LVDS bus lines
- Avoid 90 degree PCB bends & multiple vias. Use the same number of bends and vias for each signal pair to match delays
- Use good decoupling techniques. Use four surface mount bypass capacitors (2.2uF, 0.1uF, 0.01uF, and 0.001uF) placed close to the GND_CKLK2/VCC_CKLK2 and GND_CKLK3/VCC_CKLK3 pairs to eliminate switching noise
- Place a parallel termination resistor at the receiver input

Packaging

Because of the high frequency effects on packages, the LVDS feature is available in 1.27-mm BGA and 1.0-mm FineLine BGA packages.

It is important to keep the signal paths the same length and as short as possible. The balls used for LVDS signals are located on the outer two rows of balls on the FineLine BGA package. Figure 19 shows the LVDS ball placement on a 672-pin FineLine BGA package for EP20K400E and EP20K600E devices. The marked pins include the 16 LVDS input signals and LVDS clock input on the left of the package (bottom view). The 16 LVDS output signals, clock signal, and clock output signal are shown on the right of the package.

Figure 19. Location of LVDS I/O Balls on a 672-Pin FineLine BGA Package



Applications

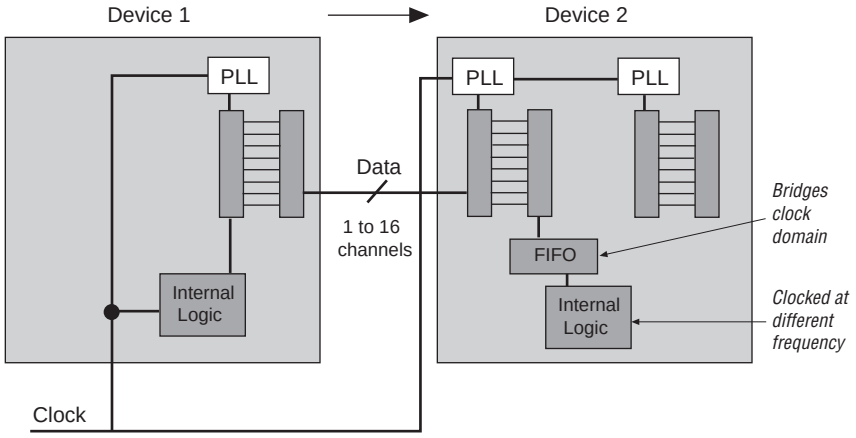
This section will discuss various LVDS topologies. There are various methods of interfacing multiple LVDS devices. APEX devices offer different PLL modes with multiple ways to connect the receiver and transmitter LVDS PLLs. The following LVDS applications are supported with APEX 20KE devices:

- Point-to-Point Configurations
- 1:N Multi-Drop LVDS
- Bypassing the Dedicated LVDS Converter Circuitry

Point-to-Point Configurations

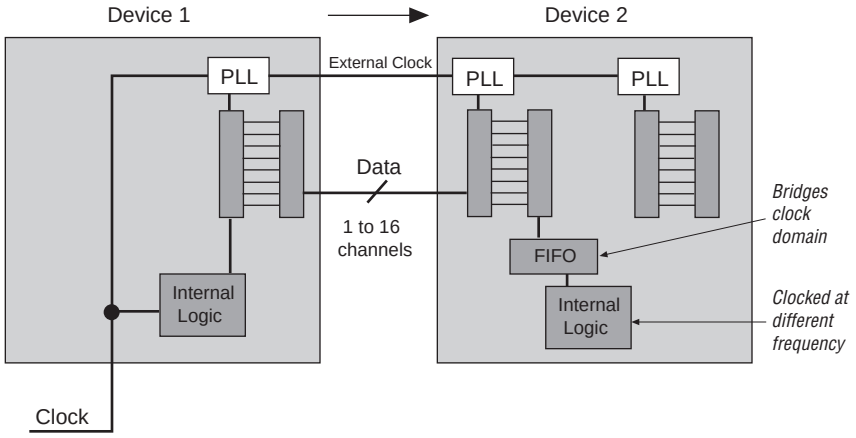
Point-to-point LVDS applications involve two devices communicating data via LVDS. For point-to-point communication, the receiver PLL can be clocked from two sources: the same source as the D1 transmitter, and the PLL output clock generated by the D1 transmitter. Figures 20 and 21 show both cases.

Figure 20. Receiver PLLs Clocked by Board Clock



The I/O timing parameters (setup time and clock-to-output) must be taken into consideration for the application shown in Figure 20. Using the source synchronous clocking scheme shown in Figure 21 is recommended. For the source synchronous application, designers need to follow the LVDS timing budget defined in "Timing Budget and Definitions" on page 5.

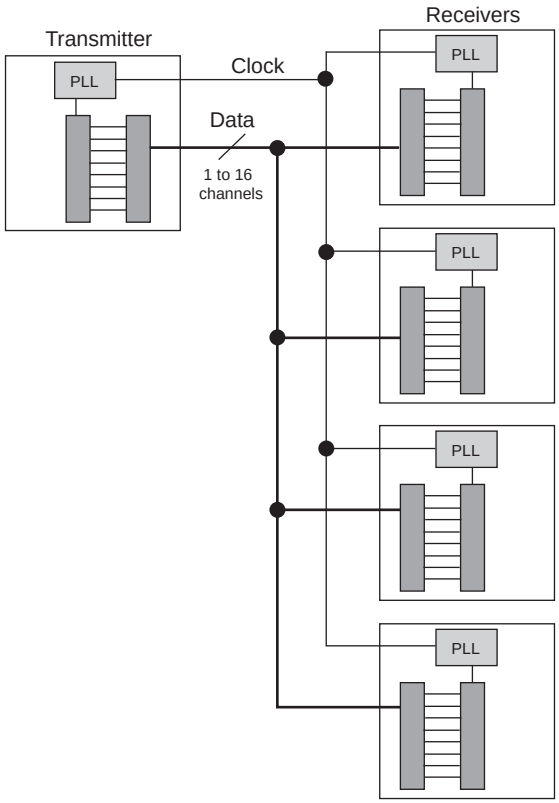
Figure 21. Transmitter PLL Clocks Receiver PLL (Source Synchronous Clocking Scheme)



Multi-Drop Configurations

The Multi-Drop Configuration has one transmitter and multiple receivers. The transmitter clock from the source device is used to clock the LVDS PLLs in the receiving devices. The performance will be affected by the number of loads that transmitter is required to drive. Preliminary information shows that an APEX 20KE device can support up to 16 loads at 400 MHz. Contact Altera Applications for up-to-date information on the Multi-Drop Configuration. Figure 22 shows a Multi-Drop Configuration with 4 loads.

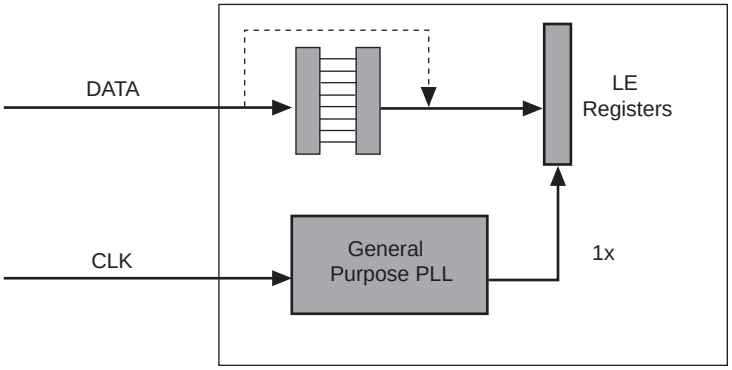
Figure 22. Multi-Drop Configuration



Bypassing the Dedicated LVDS Converter Circuitry

For low data rate LVDS signals that are less than 155 Mbps, data can bypass the dedicated serial-to-parallel converters and feed LEs directly, as shown in Figure 23. The setup and hold times are sufficient to meet the 155 Mbps requirements. In this application, the clock and data are running at the same rate. The clock can be any standard, but one of the general-purpose PLLs should be used in 1x mode to clock the LE registers. The general-purpose PLL supports LVDS signals and can operate up to an input frequency of 160 MHz.

Figure 23. Data Can Feed LEs directly for frequencies less than or equal to 155 MHz



Summary

The APEX 20KE device is the first PLD to offer an on-chip LVDS solution. The LVDS I/O standard simplifies board design by minimizing the number of devices used to interface with backplanes. APEX 20KE devices also offer increased I/O performance with increased data rates (622.08 Mbps data transfer).

References:

■ Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, ANSI/TIA/EIA-644, American National Standards Institute/Telecommunication Industry Association/Electronic Industries Association.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com