FP-MCU AG1F1 Device Datasheet

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Agate Logic, Inc.

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Contents

About This Datasheet

This datasheet provides comprehensive information about the Agate Logic FP-MCU AG1F1 devices.

Typographic Conventions

The following typographic conventions are used in this document.

Visual Cue	Meaning
Bold	Headings, figure and table indexes, figure titles, and table items. Example: **Figure 2.3.1 8051 Mode**
Italic Bold	Table titles. Example: ***Table 1.1 FP-MCU AG1F1 Features***
Helvetica	Text and figures in tables. Example: Core Voltage
Arial	Note reminders. Example: Notes for above tables
Palatino Linotype in italic	Reference to sections within this document. Example: *Clock Bundle Control Logic*
●	A list of items whose sequence is not important
(1), (2)……	Numbers in a note instruction
√	A procedure that consists of one step only.

Additional Resources

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Introduction

This document provides designers with the datasheet specifications for a special member of the Agate Logic Configurable Logic Device Product family: AG1F1, the first product generation of FP-MCU series. These sections contain feature definitions of the internal architecture, configuration, DC operating conditions, pinout information, etc.

Overview

AG1F1 is a configurable system-on-chip device and optimized for embedded systems applications. With a unique combination of over 1K logic cells (LUT/Register), 36K bits dual-port embedded memory (DPRAM), one configurable PLL, plus a high-performance 8051 MCU and 32K+8K bytes internal RAM, the MCU 8051 is integrated with the FP core logic, not just a bonus additional IP. The AG1F1 devices are designed to offer exceptional functionality, performance and value.

For flexible application, the AG1F1 devices deliver a perfect union of a high-performance 8051 microcontroller and the FP logic cell, which gives designers multiple channels for information getting. For steady and fast performance, a non-volatile SPI flash combined with the AG1F1 devices stores the 8051's user code and FP's configuration data, and the user's code can be copied to and executed from the internal SRAM.

Features

AG1F1 devices offer the following features:

- Configurable System-on-Chip (CSoC) platform
- More than 1K Field Programmable LUT/Register Logic Cells
- High-performance, industry-standard 8051-compatible microcontroller
- Stand-alone operation from a single external memory (code + configuration)
- 36K bits of configurable dual-port RAM in 9K bits blocks
- 32K + 8K bytes single-port RAM, dedicated for 8051
- Various Configuration (bootstrapping) modes, to support different application requirements
- 1 PLL (Phase-Locked) with clock multiplication and division
- Up to 16 low skew global clocks and reset trees

- Software Programmable IOs (SPIOs) and General Purpose IOs (GPIOs)

Table 1.1 summarizes the features of the AG1F1 devices.

Table 1.1 FP-MCU AG1F1 Features		
Parameter	**AG1F1**	
Core Voltage	1.2 V	
GPIOs Voltage	3.3 V	
SPIOs Voltage	3.3 V, 2.5 V, 1.8 V, 1.5 V	
Process Technology	130-nm	
LC (Logic Cells)	1,024	
User I/O Pins	100	
RAM8K Blocks	4	
PLL	1	
IO Standards Support	GPIOs	LVCMOS 3.3V
	SPIOs	LVCMOS/LVTTL 3.3V/2.5V/1.8V/1.5V, LVDS

Integrating 1K Field Programmable LUT/Register Logic Cells, an embedded high-performance 8051-based microcontroller and a large block of RAM, the FP-MCU AG1F1 is optimized for low-cost, more flexible industrial control applications. This section provides comprehensive information about the architecture of Agate AG1F1 device.

Top Level Architecture Overview

Figure 2.1.1 shows the top level architecture for AG1F1.

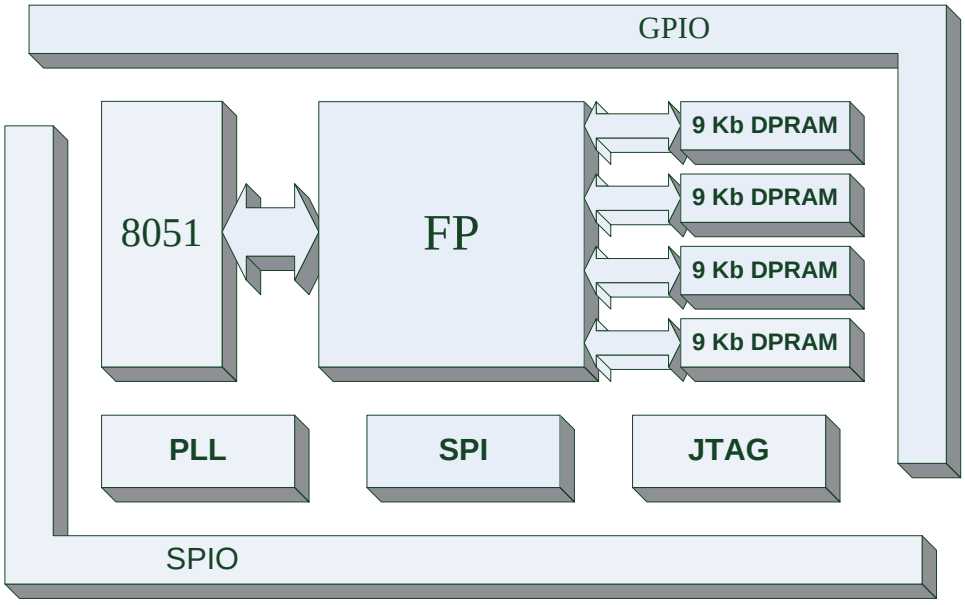

Figure 2.1.1 Top Level Architecture

Note:

(1) SPIO means software programmable IO. GPIO means general purpose IO.

The AG1F1 device architecture contains the following fundamental elements.

The 1K logic cells which is also called FP (Field Programmable) core cells provides "derivative on demand" system customization. Same as the general FPGA, these logic cells can perform various potential functions, including combinatorial and sequential logic.

The IO blocks provide the interface between external functions and the internal system bus or configurable system logic. The SPIOs offer advanced IO configuration options such as selectable output current driven strength, single-end IO standard and differential IO standard. The general purpose IO can be programmed to input, output, or inout at LVCMOS3.3V level.

Four blocks of 9Kb DPRAM can be configured to multiplicate data width types from 1 bit to 36 bits. The DPRAM blocks support a parity bit for each byte which can implement parity checking for error detection.

There is also a configurable PLL provided for clock multiplication and division.

The FP's configuration data and 8051's user code can be stored in a unique SPI Flash. In this mode, the user's code is copied to and executed from the internal SRAM. Using serial interface Flash frees numbers of device IOs. Configuration programs can also be downloaded directly through the JTAG port and written to external Flash via JTAG interface.

The embedded high-performance 8051-based microcontroller is instruction-compatible with industry-standard 8051-based devices. There is a protected watchdog timer integrated in 8051 MCU. The 8051 MCU is connected with FP directly as shown in **Figure 2.1.2**. All 8051 signals can go through FP to use IO resource. The special interface for FP extension can be used to extend external data RAM or to access DPRAM resource. A large block of fast, byte-wide SRAM provides internal storage for temporary data storage or for code storage.

Figure 2.1.2 provides the connection information of 8051 and FP.

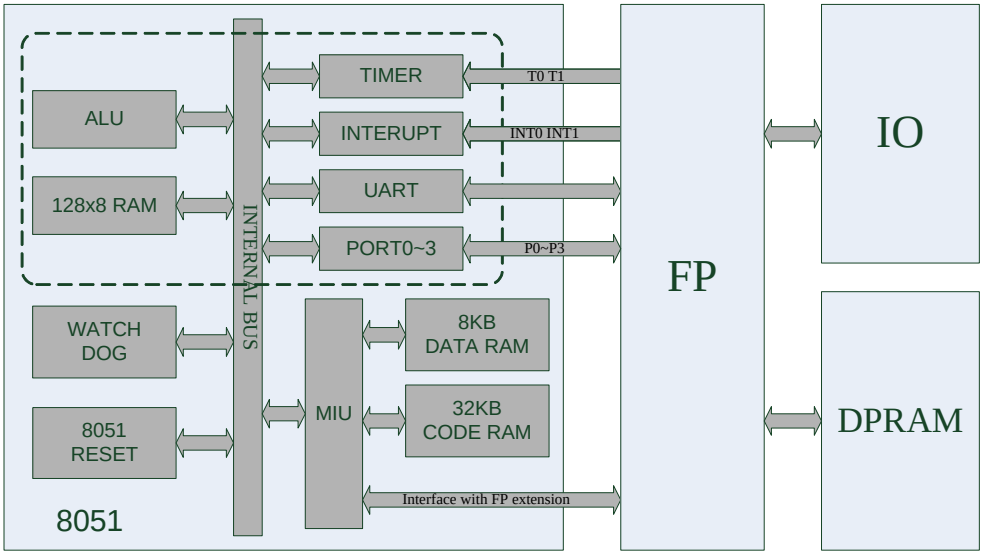

Figure 2.1.2 Connections of 8051 and FP

Field Programmable (FP) Core

Features

As the first product of Agate Logic, FP-MCU AG1F1 devices contain an array of field programmable (FP) logic blocks. Features of the FP are described as follows:

- 1024 logic cells
- 16 global signals available for register clock and reset signals
- 2048 D-type flip-flops available, each cell has two flip-flops
- Every two adjacent logic cells can be combined to function as one 8-input AND, or 8-input OR, or 8-input XOR
- Dedicated arithmetic circuitry

FP Logic Cell

The architecture of the logic cell is shown in **Figure 2.2.1**. The logic cell contains a 4-input Look-Up table (LUT) and 2 logic paths: path0 and path1. Each path leads to a logic cell output that drives the routing fabric. The path1 output is also considered as an auxiliary output and can drive other components in AG1F1 devices, such as SPIO, PLL, and 8051 IP, etc. Path0 has a configurable option to receive the auxiliary input (which can be driven by the output of SPIO, PLL, and 8051, etc) and send it directly to the routing fabric. Each path can be configured independently as a registered path, either registered by a D-type flip-flop. Or, each path can be configured to bypass the registers if the logic cell represents a level of logic in a multi-level logic cone.

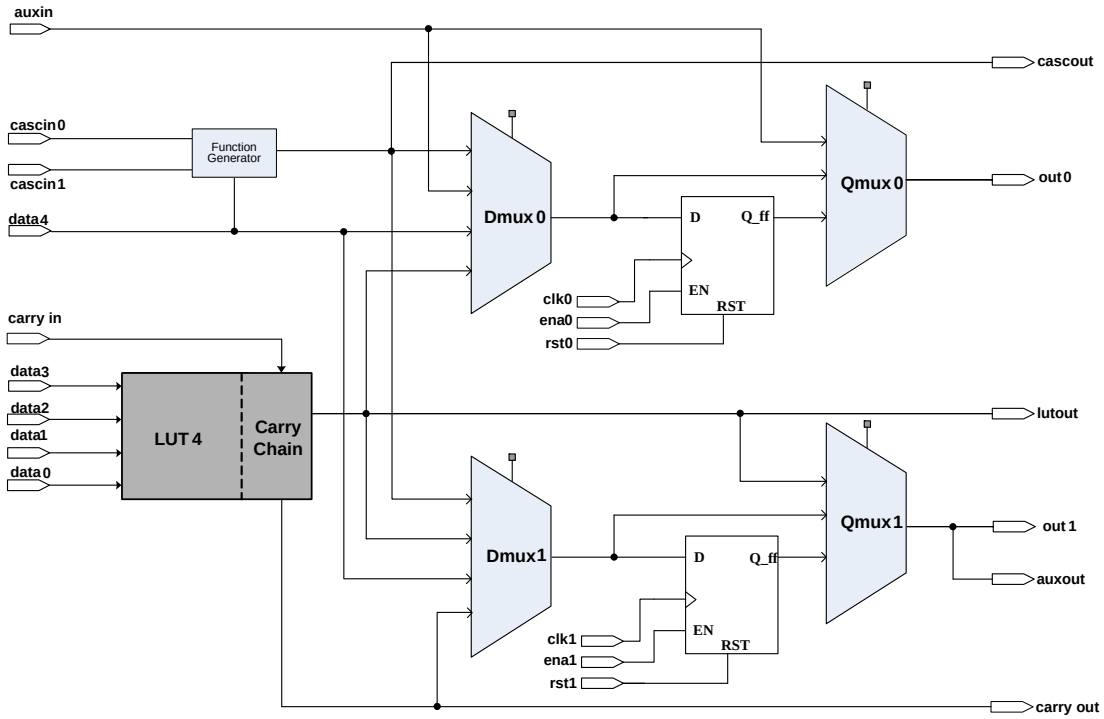

Figure 2.2.1 FP Logic Cell

The D-type flip-flop (DFF) in path0 use a clock, a reset, and a clock enable coming from that logic cell's clock bundle control unit, the DFF in path1 use a clock, a reset, and a clock enable that are independent of the global signals driving the path0 register elements. Clocks entering the logic cells trigger the DFF's on the rising-edge when the logic level is VDD. Resets entering the logic cells are asynchronous and active-high. Clock enables entering the logic cells are active-high. For more information on clock, reset and clock enable signal, see the *Clock Bundle Control Logic* section.

Normal Mode

The logic cell in normal mode contains a 4-input LUT and one DFF. User design can be synthesized friendly based on the basic cell. **Figure 2.2.2** shows the logic cell in normal mode.

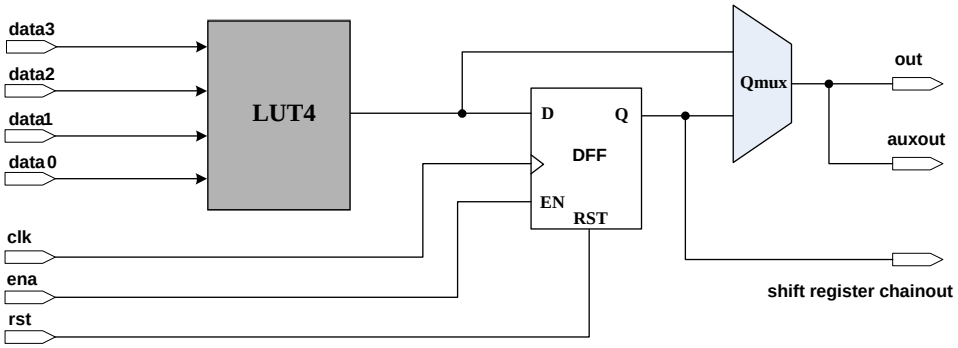

Figure 2.2.2 Normal Mode

The 4-input LUT is used as a whole to realize a LUT4 function: the output of LUT4 can lead to routing fabric directly, or pass through DFF to routing fabric then drive the auxout. Output of the register can be the input of shift register in next level.

Arithmetic Mode

The arithmetic mode is idea for implementing adders and subtractors. The operands are 2 of the 4 inputs to the LUT4 function.

Carry Chains

An arbitrary number of contiguous logic cells can be configured to realize an adder or subtracter function with carry. **Figure 2.2.3** shows a series of logic cells configured as an adder.

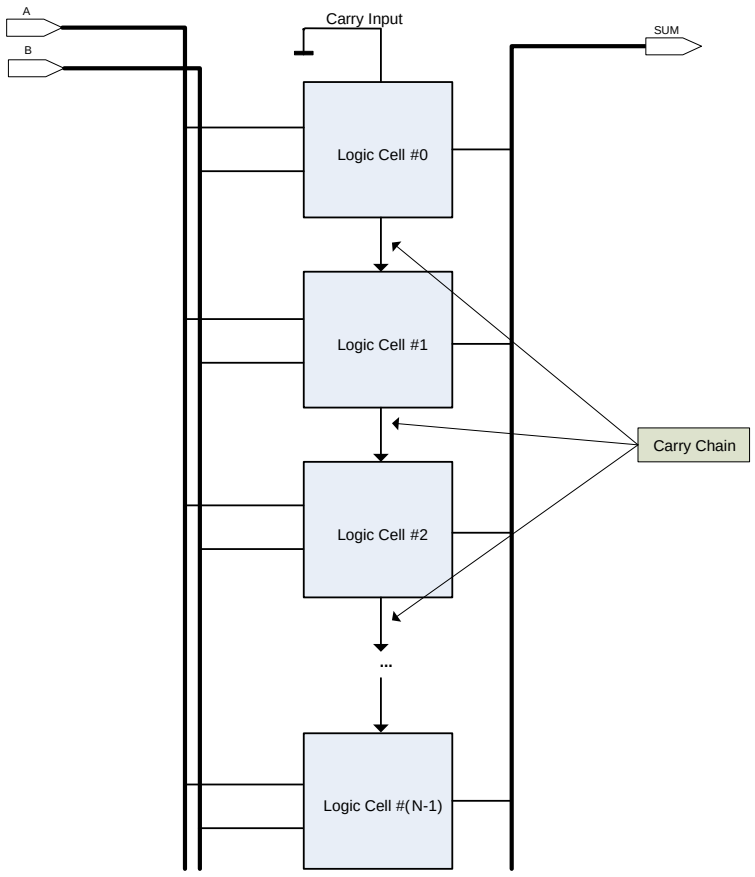

Figure 2.2.3 FP Adder

Here, an N-length adder is configured where, at each logic cell, 2 of the 4 inputs to the LUT are allocated for the adder operands.

Function Generator

The Function Generator allows the logic cell to efficiently implement some logic functions of five or more inputs. Each individual Function Generator module can be configured to be AND, OR, XOR, or MUX. The two inputs for the AND, OR, and XOR gates are the LUT outputs as are the data inputs to the MUX. The “data4” input of the logic cell is used as the select input of the mux with the 0 select value choosing the “even” input and the 1 selecting the “odd” input. **Figure 2.2.4** describes an example of Dual logic cell functions: 8-input AND.

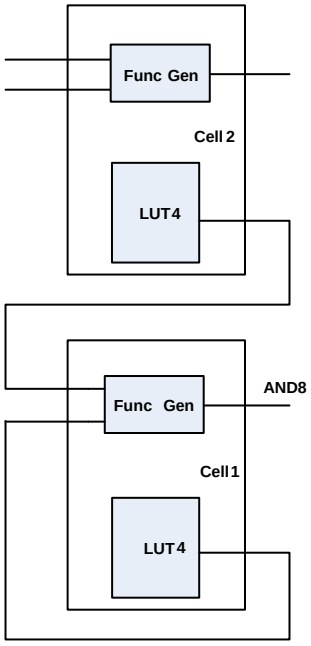

Figure 2.2.4 Dual Logic Cell Function

Figure 2.2.5 shows how to combine to LUT5, LUT6, and LUT7.

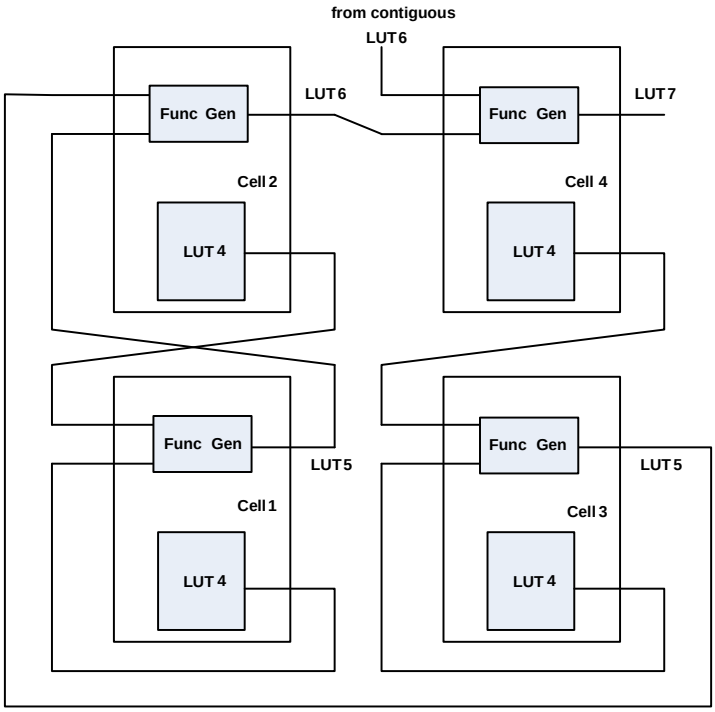

Figure 2.2.5 Combined LUTS

Table 2.2.1 lists the multiple logic cells functions supported and the number of contiguous logic cells required.

Table 2.2.1 Multiple Logic Cell Functions

Function	Number of Logic Cells
LUT5	2
LUT6	4
AND8	2
OR8	2
XOR8	2

There are 4 special logic functions that require 2 adjacent logic cells. The logic cell at the even position (if cells are numbered starting with 0 at one end of the routing tree) produces the function result and takes the AND, OR, XOR, or MUX of the LUT results from the 2 logic cells involved.

Clock Bundle Control Logic

A clock control unit exists for every 16 logic cells. This unit contains configurable muxes to select the source of the logic cell register clocks, resets, and enables for the 16 logic cells associated with it. **Figure 2.2.6** shows the logic composition of the clock control unit.

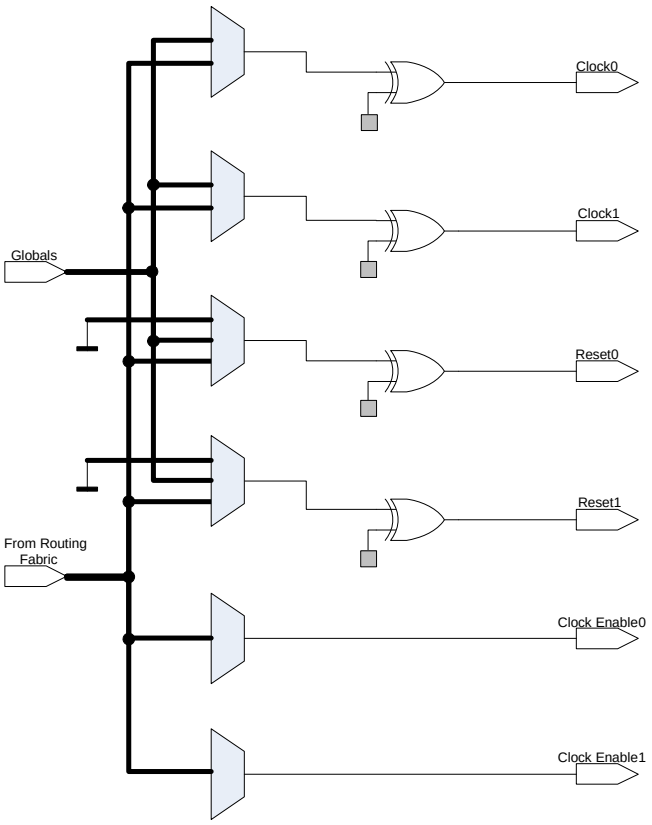

Figure 2.2.6 FP Clock Control

The squares in gray indicate configuration memory bits that control the selection of active logic level of the clocks and resets. The path0 clock, reset, and enables fan-out to 16 logic cells clustered near the clock control, driving the path0 registers in each of those cells. Likewise, the path1 clock, reset, and enables fan-out to those same logic cells but drive the path1 registers.

Each clock mux can be configured to select 1 out of 16 global signals and 4 routing fabric wires to use as logic cell register clocks. The same global signals can also be configured at each reset mux to use as logic cell register asynchronous resets. In addition, the reset muxes can select 1 out of 32 of the 36 available routing lines for resets generated by configured logic elsewhere in the core. The 16 upper-most selects at each reset mux are grounded. The clock enable muxes can select 1 out of 32 of the same 36 routing lines. The assignment of routing lines at each reset or clock enable mux varies.

Following each clock mux is an XOR gate that, under configuration, can reverse the polarity of the clock. By default, clocks are rising-edge triggering for DFF's. If the configuration bit at the XOR gate is set, the clock at that point becomes falling-edge triggering or active low. Similarly, each reset mux is followed by an XOR under configuration control for determining the active logic level of the selected reset. By default, resets are active-high. If the configuration bit is set, the reset at that point

becomes active-low. Clock enables are always active-high signals.

Routing Architecture

The FP core consists of an array of configurable logic cells and configurable routing muxes that interconnect the logic cells in a hierarchical architecture. The routing architecture resembles a tree where the logic cells are at the leaf nodes of the tree and the routing muxes are at all other nodes. Muxes propagating signals from the logic cells up the tree towards the apex are referred to as output (direction relative to logic cells) or up muxes. Muxes propagating signals towards the logic cells and away from the apex are referred to as input or down muxes.

Figure 2.2.7 illustrates the tree structure of the routing architecture.

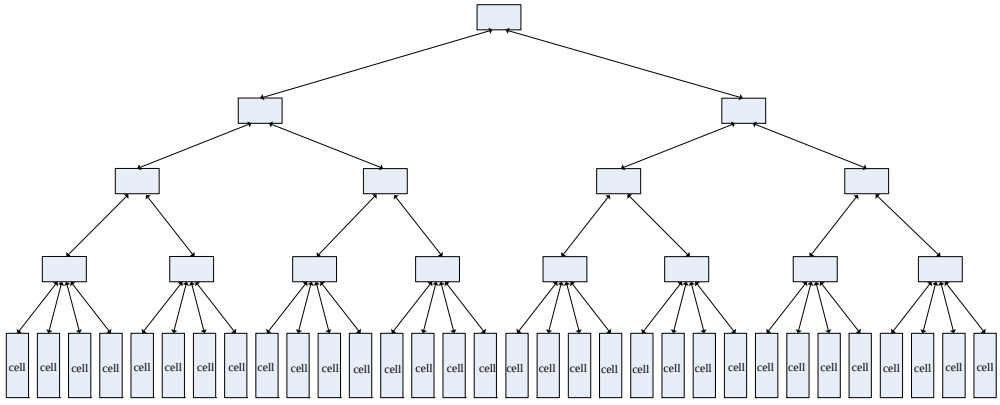

Figure 2.2.7 FP Routing Tree

The illustration provides a rough view of the routing architecture and how signals are propagated from logic cell to logic cell. Depending on the distance of the receiving cell from the sending cell, signals are driven from the sender onto the routing fabric, typically through some number of up muxes until turning at a node to a down mux (turns shown as arcs in the diagram), then traversing through the same number of down muxes until the receiver is reached. The specific details are much more elaborate than what **Figure 2.2.7** can show, but the diagram does show the basic idea of how logic is interconnected in the FP core.

Embedded Memory

The AG1F1 embedded memory consists of columns of RAM8K memory blocks. Each RAM8K block can implement various types of memory with or without parity, including true dual-port and single-port RAM.

The RAM8K blocks support the following features:

- 9,216 RAM bits
- True dual-port memory
- Single-port memory
- Mixed clock mode
- Byte enable
- Parity bits
- Support the following DPRAM width configurations: 8k × 1, 9k × 1, 4k × 2, 2k × 4, 1k × 8, 1k × 9, 512 × 16, 512 × 18, 256 × 32, 256 × 36

Memory Modes

The RAM8K memory blocks include input registers that synchronize writes. Each RAM8K block offers a true dual-port mode to support any combination of two-port operations: two reads, two writes, or one read and one write at two different clock frequencies. **Figure 2.2.8** shows true dual-port memory.

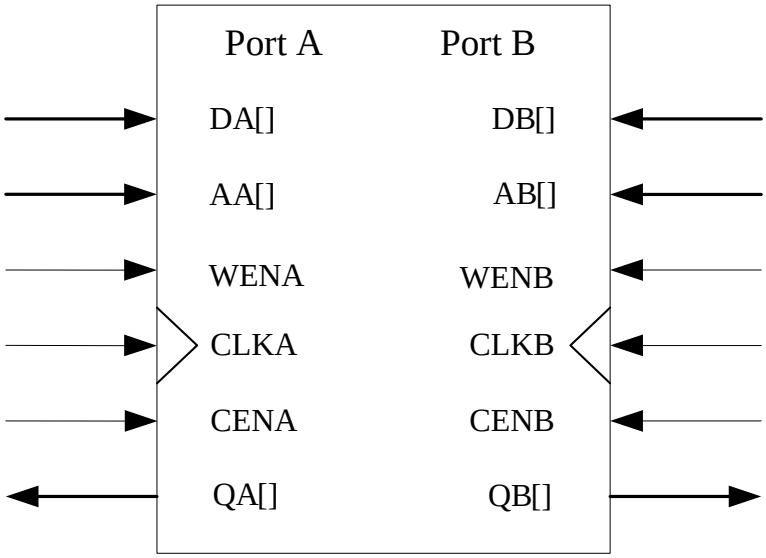

Figure 2.2.8 True Dual-port Memory Mode

The following tables summarize the ports and the function of true dual-port memory mode.

Table 2.2.2 shows a logic table of true dual-port memory mode function.

Table 2.2.2 Logic Table of True Dual-port Memory Mode Function				
Inputs			**Outputs**	
CENA (B)	**WENA (B)**	**CLK**	**Status**	**QA (B)**
0	X	X	HOLD	Data stored in the memory is retained.
1	0	↑	READ	Data is read from the memory location specified by the address bus.
1	1	↑	WRITE	DA (B)

Table 2.2.3 shows the pin descriptions of true dual-port memory mode.

Table 2.2.3 Pin Descriptions of True Dual-port Memory Mode		
Name	**Type**	**Description**
AA (B)	Input	Port A (B) Address.
DA (B)	Input	Port A (B) Data Input.
QA (B)	Output	Port A (B) Data Output.
WENA (B)	Input	Port A (B) Write Enable. Data is written into the dual-port SRAM upon the rising edge of the clock when both WENA (B) and CENA (B) are high.
CENA (B)	Input	Port A (B) Enable. When CENA (B) is high and WENA (B) is low, data read from the dual-port SRAM address AA (B) is available upon the next rising edge of CLKA (B). If CENA (B) is low, QA (B) retains its value.
CLKA (B)	Input	Port A (B) Clock.

Read and write operation waveforms of true dual-port memory mode are shown in **Figure 2.2.9**.

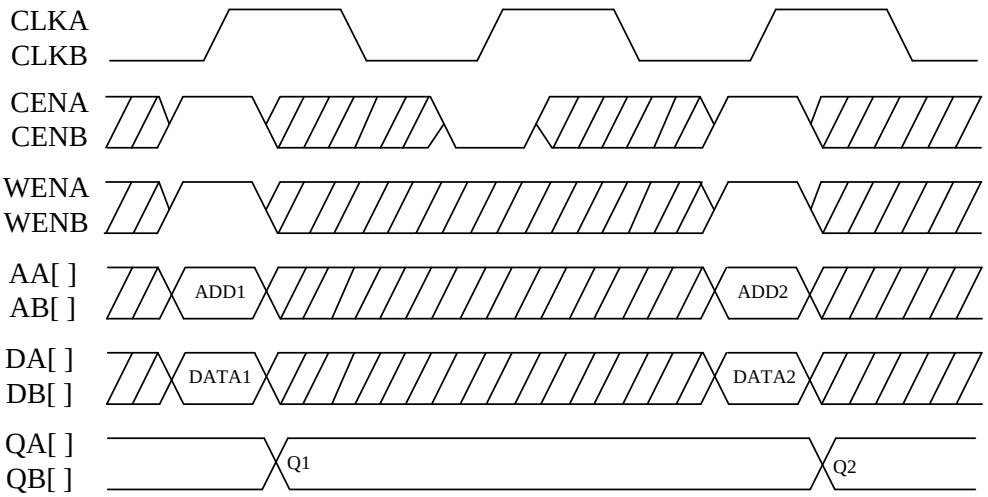

Figure 2.2.9 True Dual-Port Memory Read-Write Waveform

In addition to true dual-port memory mode, the RAM8K memory blocks support single-port memory modes. **Figure 2.2.10** shows single-port memory mode of AG1F1

RAM8K memory blocks.

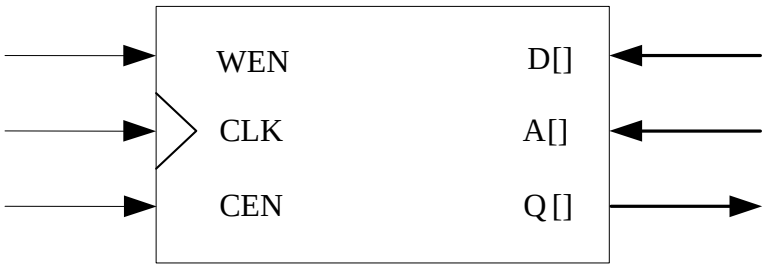

Figure 2.2.10 Single-port Memory Mode

Figure 2.2.11 gives the waveforms of read and write operations in this mode.

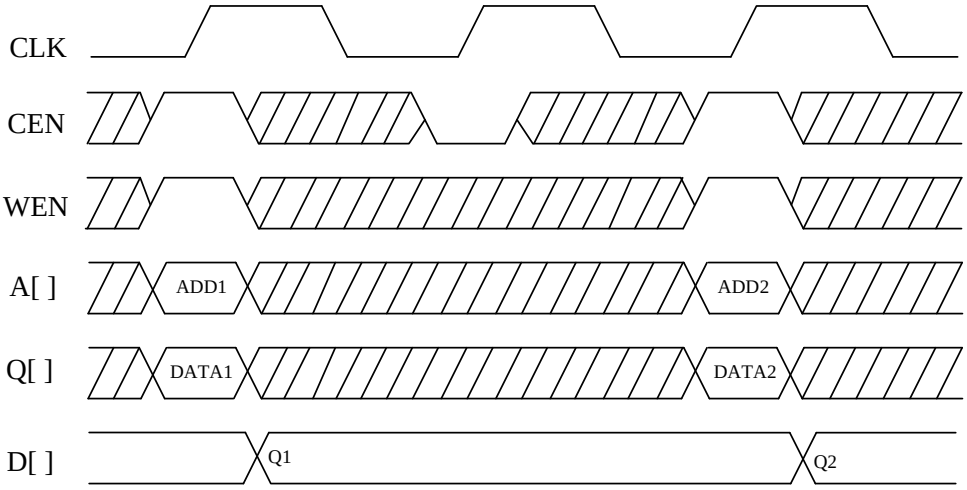

Figure 2.2.11 Single-Port Memory Read-Write Waveform

The memory blocks also enable mixed-width data ports for reading and writing to the RAM ports in dual-port RAM configuration. For example, the memory block can be written in × 1 mode at port A and read out in × 16 mode from port B.

Conflict Avoidance

For dual-port memory modes, both ports can access any memory address at any time. When both ports access the same address, the read and write behaviour should observe certain clock timing restrictions. These restrictions are adaptable to both synchronous and asynchronous clock.

Figure 2.2.12, **Figure 2.2.13**, and **Figure 2.2.14** illustrate the clock timings that may cause conflict in read and write operations with dual-port memory modes.

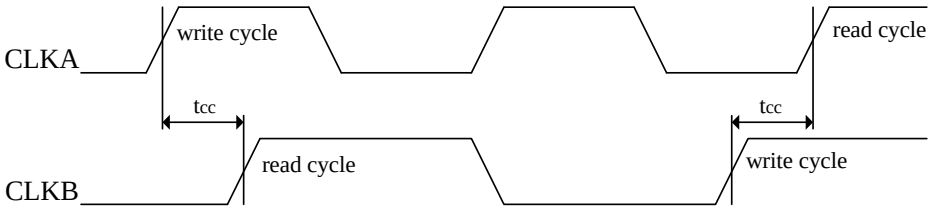

Figure 2.2.12 Dual-port memory Write-Read Clock Timing

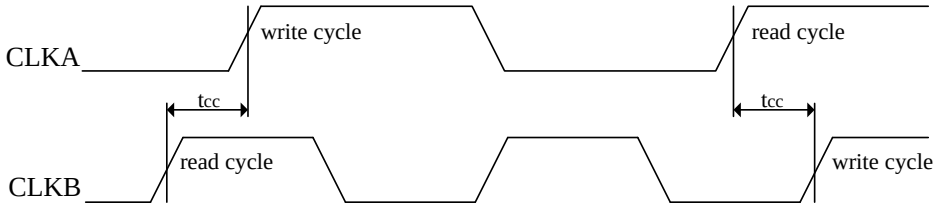

Figure 2.2.13 Dual-port memory Read-Write Clock Timing

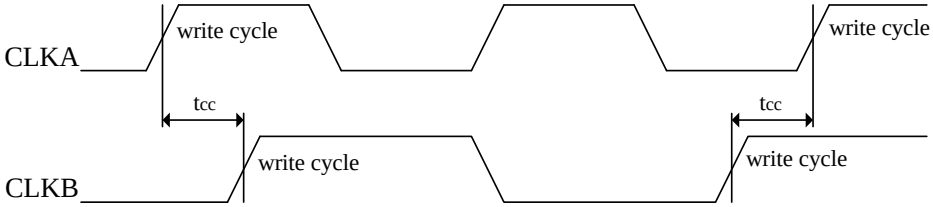

Figure 2.2.14 Dual-port memory Write-Write Clock Timing

Note for **Figure 2.2.12** to **Figure 2.2.14**:

(1) tcc means clock collision. The Min value of it is 0.748 ns based on the conditions of temperature = 25 ^{o}C, power supply = 1.2 V.

Table 2.2.4 shows read and write behaviour during clock conflicts, when both ports access the same address.

Table 2.2.4 Dual-port Memory Read and Write Behaviour when accessing the same address

Action	Condition	Behaviour
Write from one port then read from the other port	t_{cc} is satisfied (see **Figure 2.2.12**)	Write OK D-to-Q write through OK Read (new data) OK
	t_{cc} is not satisfied (see **Figure 2.2.12**)	Write fails D-to-Q write through OK Read fails
Read from one port then write from the other port	t_{cc} is satisfied (see **Figure 2.2.13**)	Write OK D-to-Q write through OK Read (old data) OK
	t_{cc} is not satisfied	Write fails

Table 2.2.4 Dual-port Memory Read and Write Behaviour when accessing the same address		
Action	**Condition**	**Behaviour**
	(see **Figure 2.2.13**)	D-to-Q write through OK Read fails
Write from one port then write from the other port	t_{cc} is satisfied (see **Figure 2.2.14**)	Both writes OK (second write overwrites first write) D-to-Q write through OK
	t_{cc} is not satisfied (see **Figure 2.2.14**)	Both writes fail D-to-Q write through OK
Read from one port then read from the other port	No restriction	Both reads OK

Parity Bit Support

The RAM8K blocks support a parity bit for each byte. The parity bit, along with internal FP Logic cell, can implement parity checking for error detection to ensure data integrity. You can also use parity-size data words to store user-specified control bits. Byte enables are also available for data input masking during write operations.

Memory Configuration Sizes

The memory address depths and output widths can be configured as 8,192 × 1, 9,216 × 1, 4,096 × 2, 2,048 × 4, 1,024 × 8 (or 1,024 × 9 bits), 512 × 16 (or 512 × 18 bits), and 256 × 32 (or 256 × 36 bits).

Table 2.2.5 summarizes the possible RAM8K block configurations.

Table 2.2.5 RAM8K Block Configurations (True Dual-Port)										
Port A	**Port B**									
	8K × 1	**4K × 2**	**2K × 4**	**1K × 8**	**512 × 16**	**256 × 32**	**9 k × 1**	**1K × 9**	**512 × 18**	**256 × 36**
8K × 1	√									
4K × 2		√								
2K × 4			√							
1K × 8				√						
512 × 16					√					
256 × 32						√				
9K × 1							√			
1K × 9								√		
512 × 18									√	
256 × 36										√

Byte Enables

RAM8K blocks support byte writes when the write port has a data width of 16, 18, 32, or 36 bits. The byte enables allow the input data to be masked so the device can write to specific bytes. The unwritten bytes retain the previous written value.

Table 2.2.6 summarizes the byte selection.

Table 2.2.6 Byte Enable for RAM8K Blocks

byteena[3..0]	datain ×18	datain ×36
[0] = 1	[8..0]	[8..0]
[1] = 1	[17..9]	[17..9]
[2] = 1	–	[26..18]
[3] = 1	–	[35..27]

PLL

FP-MCU AG1F1 PLL provides general-purpose clocks with clock multiplication and division. AG1F1 device contains one PLL.

Table 2.2.7 shows the PLL features in AG1F1. **Figure 2.2.15** shows FP-MCU AG1F1 PLL.

Table 2.2.7 PLL Features

Parameter	Value
Input reference frequency range	2MHz - 50MHz
Output frequency range	2.34 MHz - 450 MHz
VCO output frequency range	150MHz - 450MHz
Reference divider values	1 - 64
Feedback divider values	1 - 4096
Output divider values	1 - 64
Output phase separation	6.25% VCO cycle

Following is the FP-MCU AG1F1 PLL diagram.

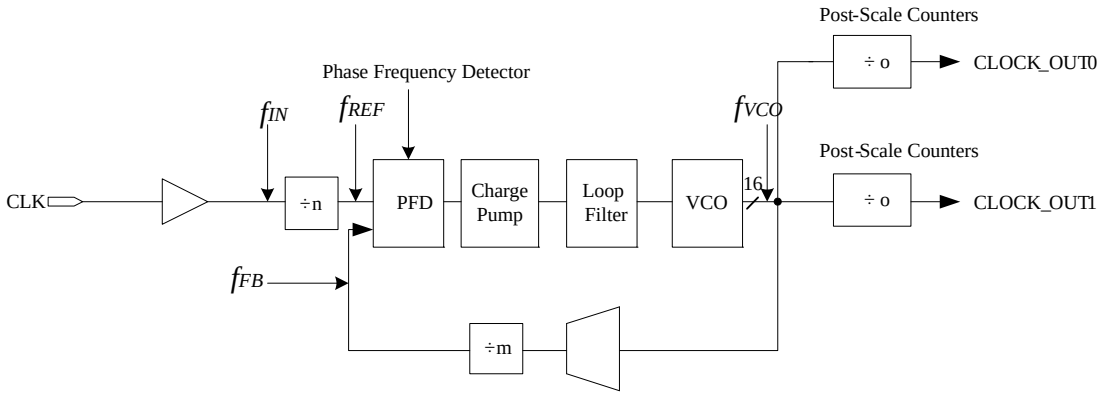

Figure 2.2.15 AG1F1 PLL

Clock Multiplication and Division

FP-MCU AG1F1 PLL provides clock synthesis for PLL two output ports, both using m/(n x o) scaling factors. The input clock is divided by a reference divider, *n*, and is then multiplied by the *m* feedback factor. The control loop drives the VCO to match $f_{IN} \times (m/n)$. Then the port0 and port1 have a post-scale counter to divide down the high-frequency VCO. The frequency of port1, port0 is divided by a post-scale divider, o.

PLL has one reference divider, *n*, that can range in value from 1 to 64. PLL also has one multiply divider, *m*, which can range in value from 1 to 4096. The pose-scale divider has a value range from 1 to 64.

PLL Control Signals

There are three control signals: RESET，PWRDN，and BYPASS. You can use these signals to control PLL resynchronization and the ability to gate PLL output clocks for low-power applications.

When the RESET signal is high, the PLL counter will reset, clearing the PLL output and placing the PLL out of lock. And it will be in resting mode when PWRDN is driven high. PLL signal will be bypassed if BYPASS goes high. At this time, the output signal equals the input signal.

Introduction

The Agate 8051 processor core is binary compatible to the well known 8051 processor from Intel. It offers faster program execution compared to the original 8051 devices since the processor's architecture have been optimized. In Agate 8051, instructions need only one to four clock cycles.

Features

- Fully synchronous circuit design , single clock
- Instruction set compatible to the industry standard 8051 microcontroller with new optimized architecture. Only one to four clock cycles per one OP code
- 128 bytes scratchpad RAM
- 8K bytes internal Data RAM
- 32K bytes internal Program RAM
- Separate address spaces for code and data
- 4, 8-bit wide, output ports (byte or bit addressable)
- 4, 8-bit wide, input ports (byte or bit addressable)
- Two 16-bit Timer/Counters
- Five Interrupt Sources
- Programmable Serial Channel
- Average performance is about (0.5~1) MIPS/MHz, which is about 8.4 times against original 8051
- Maximum working frequency is about 50 MHz
- Programmable Watchdog Timer
- ISD51 supported

Model and Signals

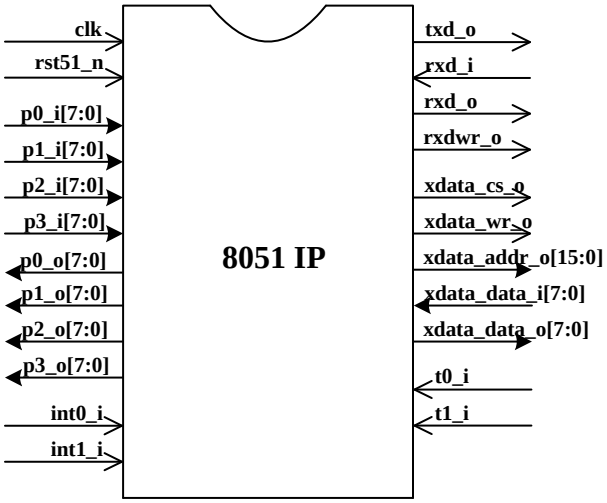

Figure 2.3.1 8051 Model

All signals are connected with FP directly. Any application can be implemented with FP logic expediently. See description of signals definition in **Table 2.3.1**.

Table 2.3.1 Signals Definition (Part i）

Port	Width	Direction	Description
clk	1	input	Clock
rst51_n	1	input	Reset signal, low active
p0_i	8	input	Parallel port 0 input
p1_i	8	input	Parallel port 1 input
p2_i	8	input	Parallel port 2 input
p3_i	8	input	Parallel port 3 input
p0_o	8	output	Parallel port 0 output
p1_o	8	output	Parallel port 1 output
p2_o	8	output	Parallel port 2 output
p3_o	8	output	Parallel port 3 output
int0_i	1	input	External interrupt 0 input
int1_i	1	input	External interrupt 1 input
txd_o	1	output	Serial port output (transmit)
rxd_i	1	input	Serial port input (receive)

Table 2.3.1 Signals Definition (Part ii)

Port	Width	Direction	Description
rxd_o	1	output	Serial port output (transmit in mode 0)
rxdwr_o	1	output	Serial port output enable (for RXD)
xdata_cs_o	1	output	Data memory extension chip selection
xdata_wr_o	1	output	Data memory extension write strobe
xdata_addr_o	16	output	Data memory extension address
xdata_data_i	8	input	Data memory extension read data
xdata_data_o	8	output	Data memory extension write data
t0_i	1	input	Timer 0 external clock input
t1_i	1	input	Timer 1 external clock input

Note:

(1) Inputs and outputs of port 0~3 are separated.

Memory Organization

The Agate 8051 uses a Harvard Architecture with separate address spaces for program and data memory. Memory in the Agate 8051 is organized into three distinct areas:

- 256 bytes Internal Data memory space (SFRs and 128 bytes scratchpad RAM)
- Up to 64K bytes External Data memory space (8K bytes SRAM on-chip)
- 32K bytes Program memory space (All on-chip)

Internal Data Memory

The Agate 8051 contains 128 bytes of general SRAM data memory and 128 bytes of Special Function Register (SFR) space. The total internal data memory space is 256 bytes as shown in **Figure 2.3.2**.

- The upper 128 bytes contain the Special Function Registers. This area is accessible only by direct addressing. See Register Space and Register Description sections for detail description.
- The lower 128 bytes contain work registers and bit-addressable memory. The lower 48 bytes of this area of memory space are further divided as follows:
  - ✓ The lower 32 bytes (00h-1Fh) form four banks of eight registers (R0-R7). The RS0 and RS1 bits in the Program Status Word register (PSW) select which bank is currently in use.

- ✓ The next 16 bytes (20h-2Fh) form a block of bit-addressable memory space, covering the bit address range 00h-7Fh.

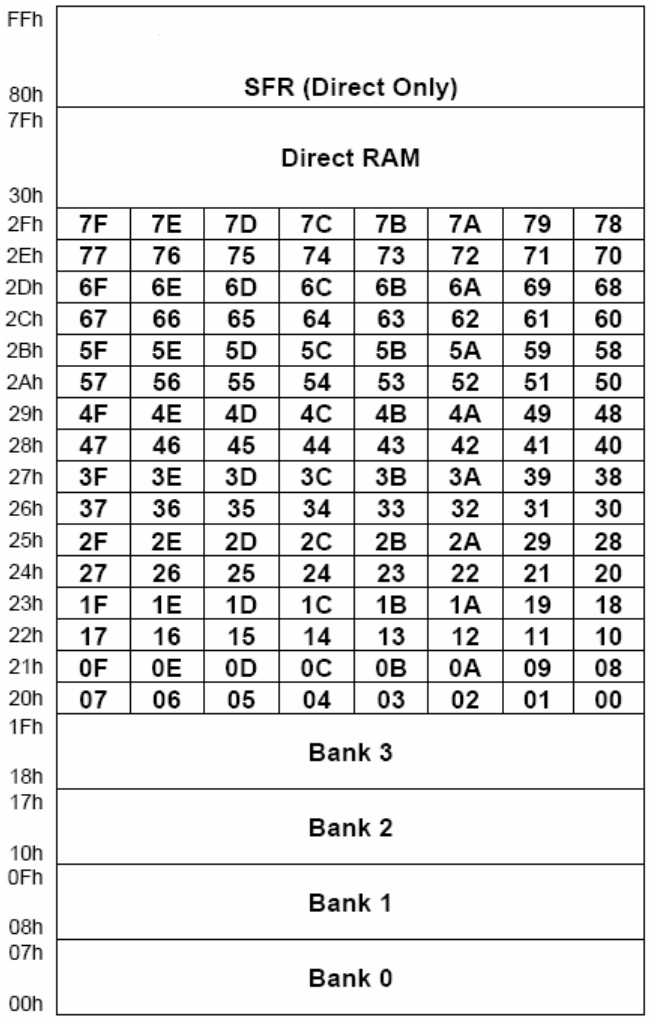

Figure 2.3.2 256 bytes Internal Data Memory Space

External Data Memory

The Agate 8051 supports a regular linear address space for up to 64K bytes data memory space. The external Data memory space can be accessed directly, through the 16 bit Data Pointer Register (DPTR).

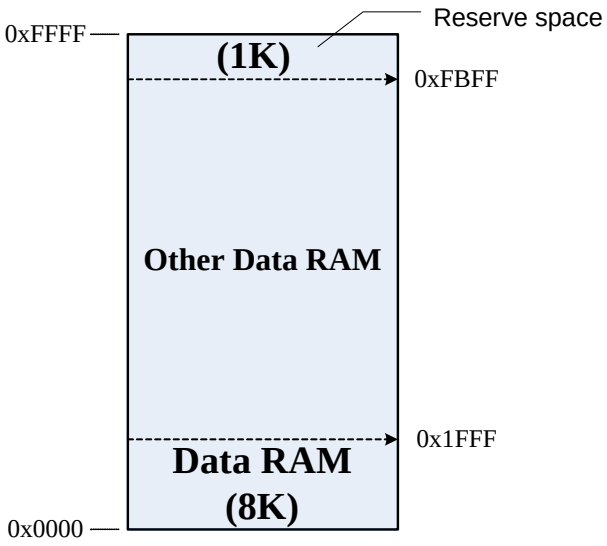

Figure 2.3.3 64K Bytes External Data Memory Space

The External Data memory space is divided as **Figure 2.3.3**. The lower 8K Data RAM is on-chip SRAM. For extension, other Data RAM must be assigned through FP connection.

Table 2.3.2 External Data Memory Address Space Assignment	
Address Space	**Description**
0x0000 ~ 0x1FFF	Internal 8K Data RAM space
0x2000 ~ 0xFBFF	Other Extension Data RAM space. User can add available RAM size through FP connected other Internal or External RAM.
0xFC00 ~ 0xFFFF	Reserved

Note:

(1) Watchdog register address is included in 0xFC00 ~ 0xFFFF address space.

Program Memory

Now the Agate 8051 supports a regular linear address space for 32K bytes program memory space. And all the 32K bytes program memory is implemented by on-chip SRAM. The program memory space can be accessed directly.

Data RAM Extension

As shown in **Figure 2.3.3**, when the Data RAM address is upper than 8K space, the read/write operation will occur on data memory extension port (the ones with prefix

xdata in **Table 2.3.1**). Use OP code 'MOVX @DPTR, A' or 'MOVX @RI, A' for write operation, and use 'MOVX A, @DPTR' or 'MOVX A, @RI' for read operation. The write and read operation waveforms are shown as below.

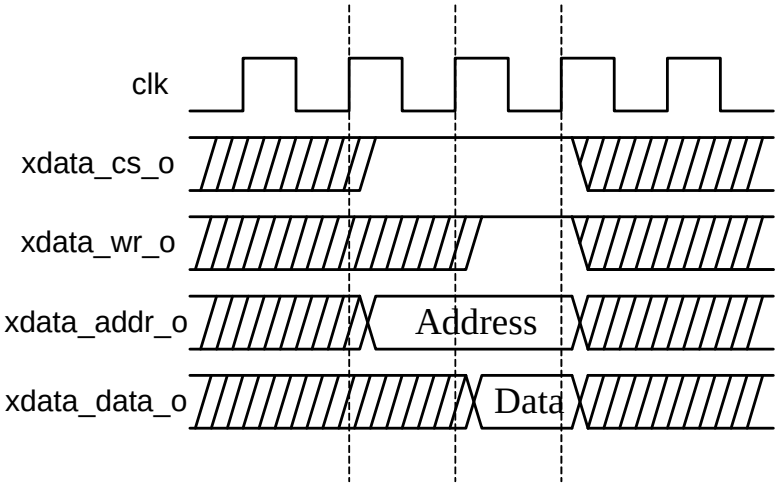

Figure 2.3.4 Extension Port Write Operation Waveform

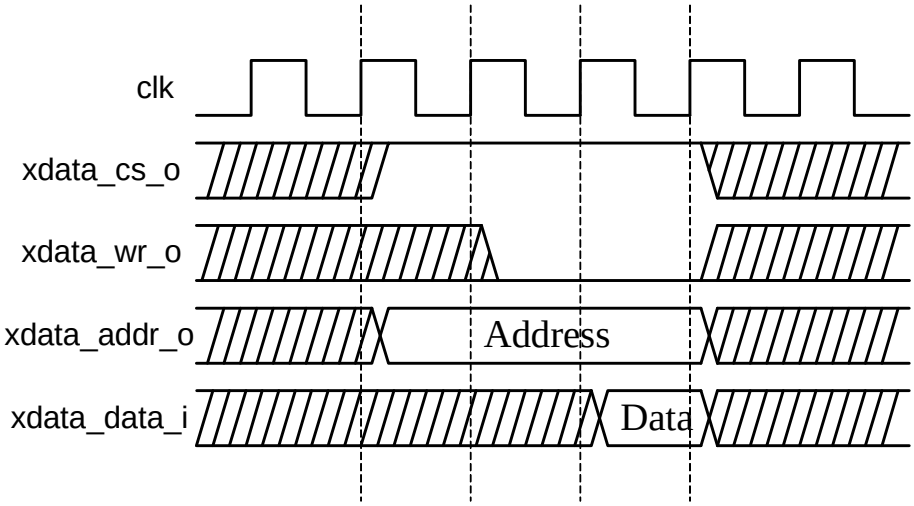

Figure 2.3.5 Extension Port Read Operation Waveform

Register Space

Register Space Assignment

The Agate 8051 uses Special Function Registers (SFRs) to control and monitor peripherals and their modes. The SFRs reside in the locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This allows a program to modify a particular bit without changing the others. The bit-addressable SFRs are those with addresses that end in 0 or 8. The list of the SFRs is shown in **Table 2.3.3**

with eight locations per row. Empty locations indicate that these are no SFR registers at these locations.

Table 2.3.3 Special Function Register (SFR) Assignment

F8h								
F0h	**B**							
E8h								
E0h	**ACC**							
D8h								
D0h	**PSW**							
C8h								
C0h								
B8h	**IP**							
B0h	**P3**							
A8h	**IE**							
A0h	**P2**							
98h	**SCON**	**SBUF**						
90h	**P1**							
88h	**TCON**	**TMOD**	**TL0**	**TL1**	**TH0**	**TH1**		
80h	**P0**	**SP**	**DPL**	**DPH**				**PCON**

The Agate 8051 system offers a programmable Watchdog Timer (WDT) for fail-safe protection against software deadlock and automatic recovery. WDT registers are not in SFR space. **Table 2.3.4** shows the corresponding address assignment.

Table 2.3.4 WDT Register Assignment

FC10h	**WDTC**
FC11h	**WDT_INT**

Register Reset Value

Table 2.3.5 Contents of the Registers after Reset

Register Name	Reset Value	Register Name	Reset Value
ACC	0000_0000	P0	1111_1111
B	0000_0000	P1	1111_1111
PSW	0000_0000	P2	1111_1111
SP	0000_0111	P3	1111_1111
IP	0000_0000	DPH	0000_0000
IE	0000_0000	DPL	0000_0000
TMOD	0000_0000	PCON	0000_0000
TCON	0000_0000	WDTC	0000_0000
SBUF	0000_0000	WDT_INT	0000_0000
SCON	0000_0000	-	-

Register Description

Accumulator Register (ACC)

Most instructions use the Accumulator to hold the operand. The mnemonics for accumulator-specific instructions, however, refer to the accumulator simply as A.

B Register

To improve the performance of Agate 8051, DIV and MUL commands are not implemented. So the B register will be only used as a scratch-pad register to hold temporary data.

Program Status Word Register (PSW)

The PSW register contains program status information as detailed in **Table 2.3.6**. Note the contents of (RS1, RS0) enable the working register banks as shown in **Table 2.3.7**.

Table2.3. 6 Program Status Word Register (PSW)

Bit	Symbol	Function
PSW.7	CY	Carry flag
PSW.6	AC	Auxiliary Carry flag
PSW.5	F1	Flag 0 available to the user for general purpose
PSW.4	RS1	Register bank select control bit 1 (See Table 2.3.7)
PSW.3	RS0	Register bank select control bit 0 (See Table 2.3.7)
PSW.2	OV	Overflow flag
PSW.1	F0	User definable flag
PSW.0	P	Parity flag. Set / Cleared by hardware each instruction cycle to indicate an odd / even number of '1' bits in the accumulator

Table2.3.7 Bank Selection

RS1	RS0	Register Bank	Address
0	0	Bank 0	00H-07H
0	1	Bank 1	08H-0FH
1	0	Bank 2	10H-17H
1	1	Bank 3	18H-1FH

Stack Pointer Register (SP)

The Stack Pointer is a 1-byte register. It is initialized to 07H after reset, and this causes the stack to begin at location 08H. It is incremented before data is stored during PUSH and CALL executions.

Data Pointer Registers (DPL and DPH)

The Data Pointer (DPTR) consists of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address. It may be manipulated as a 16-bit register or as two independent 8-bit registers.

Ports 0 to 3 Registers

P0, P1, P2 and P3 are the SFR latches of Ports 0, 1, 2, 3. The contents of the SFR can be access through corresponding SFR access interface.

Interrupt Registers

The Agate 8051 provides five interrupt sources.

The External Interrupts INT0 and INT1 can be either level-activated or transition-activated, depending on corresponding register setting. The flags that actually generate these interrupts are bits IE0 and IE1. These flags will be cleared by hardware when the service routine is vectored to only if the interrupt was transition-activated. If the interrupt is level-activated, the external requesting source will control the request flag, rather than the on-chip hardware.

The Timer 0 and Timer 1 Interrupts are indicated as bits TF0 and TF1, which are set by a rollover in their respective Timer/Counter registers. The flag will be cleared by the on-chip hardware when the service routine is vectored to.

The Serial Port Interrupt is generated by the logic OR of RI and TI. These flags can only be cleared by software.

Special Function Register IP, IE contains the control and status bits for the interrupt system. The detail description about them is shown as below.

Table 2.3.8 Interrupt Enable register (IE)		
Bit	**Symbol**	**Function**
IE.7	EA	Enable or disable all interrupts. If EA = 0, no interrupt will be acknowledge. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
IE.6	-	Not implemented, reserved for future use
IE.5	-	Not implemented, reserved for future use
IE.4	ES	Enable or disable the Serial port interrupt
IE.3	ET1	Enable or disable the Timer 1 overflow interrupt
IE.2	EX1	Enable or disable External Interrupt 1
IE.1	ET0	Enable or disable the Timer 0 overflow interrupt
IE.0	EX0	Enable or disable External Interrupt 0

Table 2.3.9 Interrupt Priority register (IP)		
Bit	**Symbol**	**Function**
IP.7	-	Not implemented, reserved for future use
IP.6	-	Not implemented, reserved for future use
IP.5	-	Not implemented, reserved for future use
IP.4	PS	Defines the Serial Port interrupt priority level.
IP.3	PT1	Defines the Timer 1 interrupt priority level.
IP.2	PX1	Defines the External Interrupt 1 priority level.
IP.1	PT0	Defines the Timer 0 interrupt priority level.
IP.0	PX0	Defines the External Interrupt 0 priority level.

If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced, this polling sequence is a second priority structure defined as follows in **Table 2.3.10**.

Table 2.3.10 Interrupt Priority Level		
Number	**Source**	**Priority Level**
1	IE0	Highest
2	TF0	
3	IE1	
4	TF1	
5	RI or TI	Lowest

Timers/Counters Registers

The Agate 8051 has two 16-bit timer/counter registers: Timer 0 and Timer 1. Both can be configured for counter or timer operations.

In timer mode, the register is incremented every 12 clock cycles.

In counter mode, a sample operation happens in every 12 clock cycles. The register is incremented when the falling edge is observed at the corresponding input pin T0 or T1. Since it takes 24 clock cycles to recognize a 1-to-0 event, the maximum input count rate is 1/24 of the external clock frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least 12 clock cycles.

Four operating modes can be selected for Timer 0 and Timer 1. Two Special Function Registers (TMOD and TCON) are used to select the appropriate mode.

Special Function Register TH0, TL0, TH1, TL1, TCON, TMOD contains the control and status bits for the timer/counters. The detailed description about them is shown as below.

Table 2.3.11 Timer 0 High Byte register (TH0)

Bit	Function
TH0[7:0]	High Byte of Timer 0

Table 2.3.12. Timer 0 Low Byte register (TL0)

Bit	Function
TL0[7:0]	Low Byte of Timer 0

Table 2.3.13 Timer 1 High Byte register (TH1)

Bit	Function
TH1[7:0]	High Byte of Timer 1

Table 2.3.14 Timer 1 Low Byte register (TL1)

Bit	Function
TL1[7:0]	Low Byte of Timer 1

Table 2.3.15 Timer/Counter Control register (TCON) (Part i)

Bit	Symbol	Function
TCON.7	TF1	Timer/Counter 1 overflow flag. Set by hardware when Timer/Counter 1 overflows. Cleared by hardware as processor vectors to the interrupt service routine
TCON.6	TR1	Timer/Counter 1 Run control bit. Set/Cleared by software to turn Timer/Counter 1 ON/OFF.
TCON.5	TF0	Timer/Counter 0 overflow flag. Set by hardware when Timer/Counter 0 overflows. Cleared by hardware as processor vectors to the interrupt service routine
TCON.4	TR0	Timer/Counter 0 Run control bit. Set/Cleared by software to turn Timer/Counter 0 ON/OFF.

Table 2.3.15 Timer/Counter Control register (TCON) (Part ii)		
Bit	**Symbol**	**Function**
TCON.3	IE1	External Interrupt 1 edge flag. Set by hardware when an edge/level is detected on INT1_i. Cleared by hardware when the service routine is vectored only if the interrupt was edge triggered. Otherwise, it will follow the pin.
TCON.2	IT1	Interrupt 1 type control bit. Set/cleared by software to specify falling edge/high level triggered External Interrupt.
TCON.1	IE0	External Interrupt 0 edge flag. Set by hardware when an edge/level is detected on INT1_i. Cleared by hardware when the service routine is vectored only if the interrupt was edge triggered. Otherwise, it will follow the pin.
TCON.0	IT0	Interrupt 0 type control bit. Set/cleared by software to specify falling edge/high level triggered External Interrupt.

Table 2.3.16 Timer/Counter Mode Control register (TMOD)		
Bit	**Symbol**	**Function**
TMOD.7	GATE	When TR1 (in TCON) is set and GATE = 1, Timer/Counter1 will run only when INT1 pin is high (hardware control). When GATE = 0, Timer/Counter1 will run only when TR1 = 1 (software control).
TMOD.6	C/T	Timer or Counter selector for Timer 1. Clear for Timer operation (input from internal system clock). Set for Counter operation (input from t1_i input pin).
TMOD.5	M1	Timer/Counter 1 mode select bit 1.
TMOD.4	M0	Timer/Counter 1 mode select bit 0.
TMOD.3	GATE	When TR0 (in TCON) is set and GATE = 1, Timer/Counter0 will run only when INT0 pin is high (hardware control). When GATE = 0, Timer/Counter0 will run only when TR0 = 1 (software control).
TMOD.2	C/T	Timer or Counter selector for Timer 0. Clear for Timer operation (input from internal system clock). Set for Counter operation (input from t0_i input pin).
TMOD.1	M1	Timer/Counter 0 mode select bit 1.
TMOD.0	M0	Timer/Counter 0 mode select bit 0.

There are four timer/counter modes supported for the two timers. The mode is determined by the state of bits M1 and M0 in the TMOD register. The set method is shown in **Table 2.3.17**.

Table 2.3.17 Mode Set Method		
M1	**M0**	**Timer/Counter Mode**
0	0	Mode 0
0	1	Mode 1
1	0	Mode 2
1	1	Mode 3

- Timer/Counter Mode 0

When in Mode 0, the Timer/Counter is set to 13 bits. If the Timer/Counter is enabled, it will count from its set value (set by software) up to 1FFFh, at which point TFx is set to 1 to indicate overflow. Hardware then resets this value to 0 after TimerX Interrupt Service routine is processed.

When overflow occurs, the Timer/Counter will roll over to 0000h and continue to count up to 1FFFh, at which point TFx is set to 1 once again. This cycle continues until the Timer/Counter is disabled.

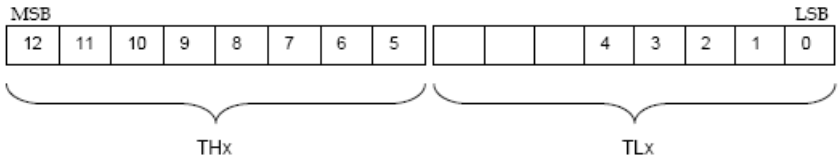

Figure 2.3.6 Timer/Counter in Mode 0

- Timer/Counter Mode 1

When in Mode 1, the Timer/Counter is set to 16 bits. The operation of the Timer/Counter in this mode is comparable to that in Mode 0. However, for this mode all 8 bits of the TLx register are used and therefore, the maximum value before overflow is FFFFh.

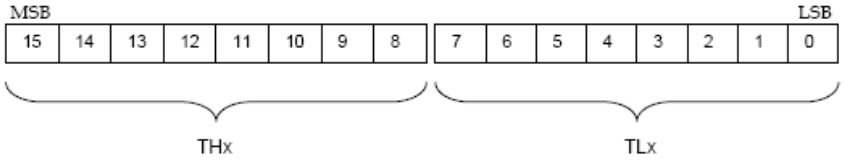

Figure 2.3.7 Timer/Counter in Mode 1

- Timer/Counter Mode 2

When in Mode 2, the Timer/Counter is set to 8 bits. This mode enables the Timer/Counter to be reloaded with its set value immediately after overflow. The two timing registers THx and TLx are used differently.

In this mode, THx hold the reload value, which is copied to TLx after overflow is detected, whereas TLx is the 8-bit dedicated Timer/Counter.

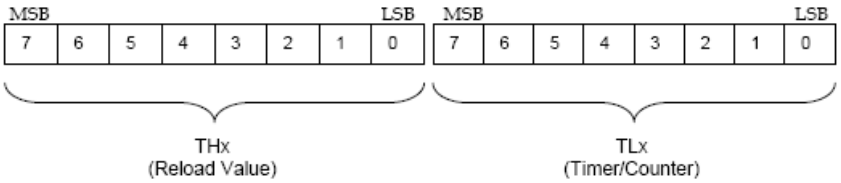

Figure 2.3.8 Timer/Counter in Mode 2

- Timer/Counter Mode 3

When Timer/Counter 0 works on Mode 3, the TH0 and TL0 registers operate independently of each other as follows:

TL0 operates as an 8-bit Timer/Counter, controlled by Timer/Counter 0 mode control bits TMOD.3 and TMOD.2.

TH0 operates as a dedicated 8-bit Timer, controlled by Timer/Counter 1 mode control bits TMOD.7 and TMOD.6, with no external gate control.

In this condition, Timer/Counter 1 can be defined as Mode 0, Mode 1 or Mode 2. But the interrupt TF1 cannot be used by Timer/Counter 1.

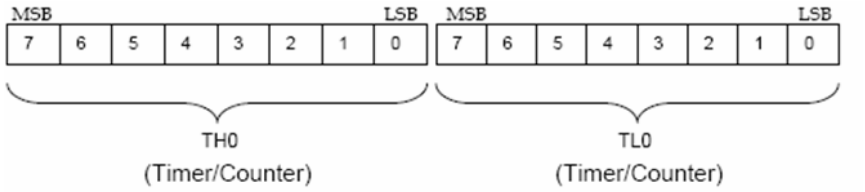

Figure 2.3.9 Timer/Counter in Mode 3

Serial Interface Registers

The serial interface provides both synchronous (In mode 0) and asynchronous (In mode 1, 2, 3) modes. Asynchronous transmission and reception can occur simultaneously, even at different baud rates.

It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. (However, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost). The serial port receive and transmit registers are both accessed at Special Function Register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses the receive register.

Four Modes of Serial Port Operation

- Mode 0

When in mode 0, Serial data enter and exit through rxd_i and rxd_o. The txd_o exports the shift clock. Eight bits are transmitted with LSB first. The baud rate is fixed at 1/12 of the 8051 work clock frequency.

- Mode 1

When in mode 1, Serial data enter and exit through rxd_i and txd_o. No external shift clock is used. 10 bits are transmitted: a start bit 0, 8 data bits (LSB first), and a stop bit 1. On reception, the start bit synchronizes the transmission, 8 data bits are made available by reading SBUF, and the stop bit sets the flag RB8 in the Special Function Register SCON.

- Mode 2

This mode is similar to Mode 1, with two differences. The baud rate is fixed at 1/32 or 1/64 of oscillator frequency, and 11 bits are transmitted or received: a start bit 0, 8 data bits (LSB first), a programmable 9th bit, and a stop bit 1. The 9th bit can be used to control the parity of the serial interface: at transmission, bit TB8 in SCON is output as the 9th bit, and at reception, the 9th bit affects RB8 in the Special Function Register SCON.

- Mode 3

The only difference between Mode 2 and Mode 3 is that the baud rate is variable in Mode 3.

Multiprocessor Communication

The feature of receiving 9 bits in Modes 2 and 3 can be used for multiprocessor communication. In this case, the slave processors have bit SM2 in SCON set to 1. When the master processor outputs a slave's address, it sets the 9th bit to 1, causing a serial port to receive interrupt in all the slaves. The slave processors compare the received byte with their network address. If there is a match, the addressed slave will clear SM2 and receive the rest of the message, while other slaves will leave the SM2 bit unaffected and ignore the message. After addressing the slave, the host will output the rest of the message with the 9th bit set to 0, so no serial port receiving interrupt will be generated in unselected slaves.

Registers

Special Function Register SBUF, PCON, SCON contains the control and status bits for the serial port.

The Serial Data Buffer (SBUF) is actually two separate registers, a transmit buffer register and a receive buffer register. When data is moved to SBUF, it goes to the transmit buffer where it is held for serial transmission. When data is moved from SBUF, it comes from the receive buffer.

The detail description about PCON and SCON is shown as below tables.

Table 2.3.18 Power Control Register (PCON)

Bit	Symbol	Function
PCON.7	SMOD	Double baud rate bit. If Timer 1 is used to generate the baud rate and SMOD = 1, the baud rate is doubled when the Serial Port is used in modes 1,2 or 3
PCON.6	-	Not implemented, reserved for future use
PCON.5	-	Not implemented, reserved for future use
PCON.4	-	Not implemented, reserved for future use
PCON.3	-	Not implemented, reserved for future use
PCON.2	-	Not implemented, reserved for future use
PCON.1	-	Not implemented, reserved for future use
PCON.0	-	Not implemented, reserved for future use

Table 2.3.19 Serial Port Control registers (SCON)

Bit	Symbol	Function
SCON.7	SM0	Serial Port mode select bit 0.
SCON.6	SM1	Serial Port mode select bit 1.
SCON.5	SM2	Enables multiprocessor communication feature in mode 2 & 3. In mode 2 or 3, if SM2 is set to 1, RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1 then RI will not be activated if a valid stop bit was not received. In mode 0, SM2 should be 0.
SCON.4	REN	Set / Cleared by software to Enable / Disable reception
SCON.3	TB8	This is the 9th bit to be transmitted in mode 2 and 3. This bit is set and cleared by software as desired.
SCON.2	RB8	In Modes 2 and 3, it is the 9th bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit. In Mode 0, RB8 is not used.
SCON.1	TI	Transmit interrupt flag, set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in the other modes. Must be cleared by software.
SCON.0	RI	Receive interrupt flag, set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bit time in the other modes. Must be cleared by software.

Serial Baud Rates

The baud rate in Mode 0 is fixed, a twelfth of the 8051 work frequency.

The baud rate in Mode 2 depends on the value of bit SMOD in Special Function Register PCON. If SMOD = 0, the baud rate is 1/64 of the 8051 work frequency. If SMOD = 1, the baud rate is 1/32 of the 8051 work frequency.

In Mode 1 and 3, the Timer 1 overflow rate is used to generate baud rate. If Timer 1 is configured in mode 2, the baud rate is determined by the following equation.

$$\text{Baud Rate} = \frac{2^{SMOD} \times F_{CLK}}{32 \times 12 \times (256 - TH1)}$$

Figure 2.3.10 Baud Rate Equation

Watchdog Timer Registers

To protect the system against software deadlock, the user software must refresh the WDT within a time period when Watchdog Timer is enabled. If the software fails to do this periodical refreshing, an internal hardware reset will be initiated if reset is enabled. The software can be designed such that the WDT times out if the program does not work properly.

Descriptions of two WDT registers are shown as the following tables.

Table 2.3.20 Watch Dog Timing Control Register (WDTC)

Bit	Access	Description
[7:5]	RW	Reserved
[4:2]	RW	WDT duration selection bits. 000:1time, 001:2times, 010:4times, 011:8times, 100:16times, 101:32times, 110:64times, 111: 128times
[1]	RW	Watch Dog reset output enable control: 1, enable; 0, disable
[0]	RW	Watch Dog enable control: 1, enable; 0, disable

Note:

(1) One time equals to two mcu clock cycles.

Table 2.3.21 Watch Dog Timing Interrupt Status Register (WDT_INT)

Bit	Access	Description
[7:1]	RW	Reserved
[0]	RW	Watch Dog Interrupt Status indication: 1, Interrupt Status; 0, No Interrupt Status

Performance Improvement

Table 2.3.22 Performance Comparison with Original 8051 (Part i)

Instruction	Program Bytes	Original 8051 Instruction Cycles	Original 8051 Clock Cycles	Agate 8051 Clock Cycles	Performance Advantage
ACALL	2	2	24	2	12
ADD A, @RI	1	1	12	2	6
ADD A, ADDR	2	1	12	3	4
ADD A, DATA	2	1	12	2	6
ADD A, R	1	1	12	2	6
ADDC A, @RI	1	1	12	2	6
ADDC A, ADDR	2	1	12	3	4
ADDC A, DATA	2	1	12	2	6
ADDC A, R	1	1	12	2	6
AJMP	2	2	24	2	12
ANL A, @RI	1	1	12	2	6
ANL A, ADDR	2	1	12	3	4
ANL A, DATA	2	1	12	2	6
ANL A, R	1	1	12	2	6
ANL ADDR, A	2	1	12	3	4
ANL ADDR, DATA	3	2	24	3	8
ANL C, BIT	2	2	24	3	8
ANL C, NBIT	2	2	24	3	8
CJNE @RI, DATA	3	2	24	3	8
CJNE A, ADDR	3	2	24	3	8
CJNE A, DATA	3	2	24	3	8
CJNE R, DATA	3	2	24	3	8
CLR A	1	1	12	1	12
CLR BIT	2	1	12	2	6
CLR C	1	1	12	1	12
CPL A	1	1	12	1	12
CPL BIT	2	1	12	3	4
CPL C	1	1	12	1	12
DA A	1	1	12	1	12
DEC @RI	1	1	12	2	6
DEC A	1	1	12	1	12
DEC ADDR	2	1	12	3	4
DEC R	1	1	12	2	6
DJNZ ADDR	3	2	24	3	8

Table 2.3.22 Performance Comparison with Original 8051 (Part ii)

Instruction	Program Bytes	Original 8051 Instruction Cycles	Original 8051 Clock Cycles	Agate 8051 Clock Cycles	Performance Advantage
DJNZ R	2	2	24	2	12
INC @RI	1	1	12	2	6
INC A	1	1	12	1	12
INC ADDR	2	1	12	3	4
INC DPTR	1	2	24	4	6
INC R	1	1	12	2	6
JB	3	2	24	3	8
JBC	3	2	24	3	8
JC	2	2	24	2	12
JMP A, DPTR	1	2	24	1	24
JNB	3	2	24	3	8
JNC	2	2	24	2	12
JNZ	2	2	24	2	12
JZ	2	2	24	2	12
LCALL	3	2	24	3	8
LJMP	3	2	24	3	8
MOV @RI, A	1	1	12	1	12
MOV @RI, ADDR	2	2	24	3	8
MOV @RI, DATA	2	1	12	2	6
MOV A, @RI	1	1	12	2	6
MOV A, ADDR	2	1	12	3	4
MOV A, DATA	2	1	12	2	6
MOV A, R	1	1	12	2	6
MOV ADDR, @RI	2	2	24	2	12
MOV ADDR, A	2	1	12	2	6
MOV ADDR, ADDR	3	2	24	3	8
MOV ADDR, DATA	3	2	24	3	8
MOV ADDR, R	2	2	24	2	12
MOV BIT, C	2	2	24	2	12
MOV C, BIT	2	1	12	3	4
MOV DPTR, DATA	3	2	24	3	8
MOV R, A	1	1	12	1	12
MOV R, ADDR	2	2	24	3	8
MOV R, DATA	2	1	12	2	6
MOVC A, @DPTR	1	2	24	2	12
MOVC A, ATPC	1	2	24	2	12
MOVX @DPTR, A	1	2	24	1	24
MOVX @RI, A	1	1	12	1	12

Table 2.3.22 Performance Comparison with Original 8051 (Part iii)

Instruction	Program Bytes	Original 8051 Instruction Cycles	Original 8051 Clock Cycles	Agate 8051 Clock Cycles	Performance Advantage
MOVX A, @DPTR	1	2	24	2	12
MOVX A, @RI	1	2	24	2	12
NOP	1	1	12	1	12
ORL A, @RI	1	1	12	2	6
ORL A, ADDR	2	1	12	3	4
ORL A, DATA	2	1	12	2	6
ORL A, R	1	1	12	2	6
ORL ADDR, A	2	1	12	3	4
ORL ADDR, DATA	3	2	24	3	8
ORL C, BIT	2	2	24	3	8
ORL C, NBIT	2	2	24	3	8
POP	2	2	24	2	12
PUSH	2	2	24	3	8
RET	1	2	24	3	8
RETI	1	2	24	3	8
RL A	1	1	12	1	12
RLC A	1	1	12	1	12
RR A	1	1	12	1	12
RRC A	1	1	12	1	12
SETB BIT	2	1	12	2	6
SETB C	1	1	12	1	12
SJMP	2	2	24	2	12
SUBB A, @RI	1	1	12	2	6
SUBB A, ADDR	2	1	12	3	4
SUBB A, DATA	2	1	12	2	6
SUBB A, R	1	1	12	2	6
SWAP A	1	1	12	1	12
XCH A, @RI	1	1	12	3	4
XCH A, ADDR	2	1	12	4	3
XCH A, R	1	1	12	3	4
XCHD A, @RI	1	1	12	3	4
XRL A, @RI	1	1	12	2	6
XRL A, ADDR	2	1	12	3	4
XRL A, DATA	2	1	12	2	6
XRL A, R	1	1	12	2	6
XRL ADDR, A	2	1	12	3	4
XRL ADDR, DATA	3	2	24	3	8

Overview

The FP logic cells of Agate Logic FP-MCU AG1F1 devices use SRAM cells to store configuration data. Since SRAM memory is volatile, configuration data must be downloaded to FP-MCU device each time the device powers up. You can download configuration data to AG1F1 devices using the SPI, or JTAG interfaces.

Figure 3.1 shows the pin connection information of SPI configuration scheme and JTAG-based configuration for FP-MCU AG1F1 device.

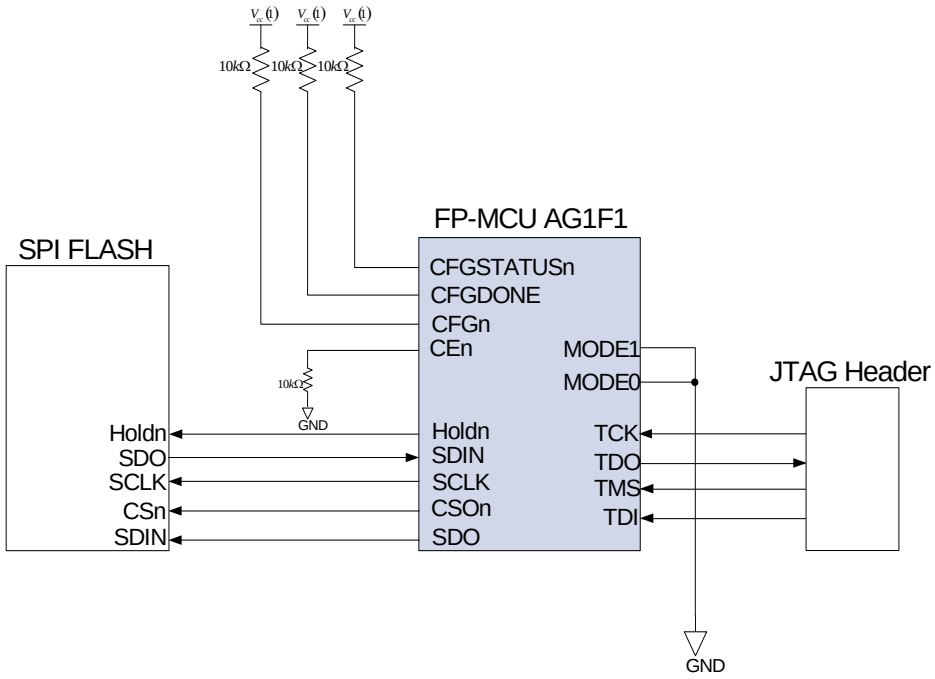

Figure 3.1 SPI and JTAG Configuration

JTAG-Based Configuration

You can select the JTAG-based configuration scheme for your application by driving AG1F1 MODE1 and MODE0 pins either high (1) or low (0).

During JTAG configuration, data is downloaded to the device on the board through

download cable. Configuring devices through a cable is similar to programming devices in-system.

FP-MCU AG1F1 devices are designed such that JTAG instructions have precede CEn over any device operating modes. So JTAG configuration can take place without waiting for other configuration to complete (e.g. configuration with serial or enhanced configuration devices). If you attempt JTAG configuration in AG1F1 devices during non-JTAG configuration, non-JTAG configuration is terminated and JTAG configuration is initiated.

SPI Configuration

Active Serial (AS) SPI Configuration

In the AS configuration scheme, AG1F1 MODE1 pin should be set to 0 and MODE0 should be set to 0. AG1F1 devices are configured using the industry-standard SPI serial devices. These configuration devices are low cost devices with non-volatile memory that feature a simple few pin interface and a small form factor. These features make serial configuration devices an ideal solution for configuring the low-cost FP-MCU devices.

Serial configuration devices provide a serial interface to access configuration data. During device configuration, AG1F1 devices read configuration data via the serial interface, and configure their SRAM cells. This scheme is referred to as an AS configuration scheme because the device controls the configuration interface.

Passive Serial (PS) SPI Configuration

In the PS scheme, an external host (configuration device, embedded processor, or host PC) controls configuration. Configuration data is input to the target AG1F1 devices via the SDI pin at each rising edge of SCLK.

You should select the PS configuration scheme for your application by setting FP-MCU AG1F1 MODE1 as 0 and MODE0 as 1.

SPIO DC Specifications

This section mainly describes the DC specifications of Agate Logic AG1F1 devices. Both SPIO and GPIO DC specifications are listed in the following tables.

LVCMOS33 D.C. Specifications

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	VCCO	3.0	3.3	3.45	V
Output Sink Current	IOL	-12	-	-	mA
Output Source Current	IOH	12	-	-	mA
Input Voltage Low	VIL	-0.5	-	0.8	V
Input Voltage High	VIH	2.0	-	3.95	V
Output Voltage Low	VOL	-	-	0.5	V
Output Voltage High	VOH	2.4	-	-	V

LVCMOS25 D.C. Specifications

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	VCCO	2.3	2.5	2.7	V
Output Sink Current	IOL	-12	-	-	mA
Output Source Current	IOH	12	-	-	mA
Input Voltage Low	VIL	-0.5	-	0.7	V
Input Voltage High	VIH	1.7	-	3.2	V
Output Voltage Low	VOL	-	-	0.4	V
Output Voltage High	VOH	1.9	-	-	V

LVCMOS18 D.C. Specifications

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	VCCO	1.7	1.8	1. 9	V
Output Sink Current	IOL	-12	-	-	mA
Output Source Current	IOH	12	-	-	mA
Input Voltage Low	VIL	-0.5	-	35% VCCO	V
Input Voltage High	VIH	65% VCCO	-	2.4	V
Output Voltage Low	VOL	-	-	0.4	V
Output Voltage High	VOH	VCCO - 0.4	-	-	V

LVCMOS15 D.C. Specifications

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	VCCO	1.4	1.5	1.6	V
Output Sink Current	IOL	-8	-	-	mA
Output Source Current	IOH	8	-	-	mA
Input Voltage Low	VIL	-0.5	-	35% VCCO	V
Input Voltage High	VIH	65% VCCO	-	2.1	V
Output Voltage Low	VOL	-	-	0.4	V
Output Voltage High	VOH	VCCO - 0.4	-	-	V

Different IO Driven Strength

I/O Standard (V)	Driven Strength(mA)			
3.3	12	8	4	2
2.5	12	8	4	2
1.8	12	8	4	2
1.5	-	8	4	2

GPIO DC Specifications

LVCMOS33 D.C. Specifications

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	VCCO	3.15	3.3	3.45	V
Output Sink Current	IOL	4	-	-	mA
Output Source Current	IOH	4	-	-	mA
Input Voltage Low	VIL	-0.5	-	0.8	V
Input Voltage High	VIH	2.0	-	3.6	V
Output Voltage Low	VOL	-	-	0.4	V
Output Voltage High	VOH	2.4	-	-	V

Notes for above tables:

(1) Descriptions of the symbols used in these tables are as follows:
VCCO – Supply voltage for single-ended inputs and for output drivers
VREF – Reference voltage for setting the input switching threshold
IOL – Output current condition under which VOL is tested
IOH – Output current condition under which VOH is tested
VIL – Input voltage that indicates a low logic level
VIH – Input voltage that indicates a high logic level
VOL – Output voltage that indicates a low logic level
VOH – Output voltage that indicates a high logic level

(2) Absolute maximum ratings are stress ratings. Continuously operating at or beyond these ratings listed above may cause unrecoverable damage to the device.

Overview

The AG1F1 devices are available in the quad flat package style, QFP144. This section mainly describes the various pins on FP-MCU AG1F1 and how they connect within the supported component packages.

Pin Types

As described in the FP-MCU family datasheet, most pins of AG1F1 are general-purpose, user-defined I/O pins. There are, however, up to 3 different functional types of pins on AG1F1 packages, as outlined in **Table 5.1**.

Table5.1 Types of Pins on AG1F1 (Part i)

Type	Pin Name	Pin Type	Pin Description
Power Supply and Voltage Reference Pins	VDDIO[1..4]	Power	I/O supply voltage pins for bank1 through bank4. Each bank can support a different voltage level. VDDIO supplies power to the output buffers for all I/O. VDDIO also supply voltage to the input buffers used for LVTTL,LVCMOS, 1.5V, 1.8V, 2.5 V and 3.3V.
	VDDINT	Power	Internal voltage supply pins. VDDINT also supplies power to the input buffers used for LVDS, SSTL2 and SSTL3 I/O standard.
	VSS	Ground	Digital Ground
	VDDA_PLL	Power	Analog power for PLL. It should connect to 1.5V even if PLL is not used
	VSSA_PLL	Ground	Analog ground for PLL. It can connect to Ground plan on the board
Clock and PLL Pins	CLOCK0	Input,	Dedicated global clock input.
	CLOCK1	Input,	Dedicated global clock input.

Table5.1 Types of Pins on AG1F1 (Part ii)

Type	Pin Name	Pin Type	Pin Description
Configuration and JTAG Pins	CFGDONE	Bidirectional (open drain)	This is a dedicated configuration status pin , not user I/O
	CFGSTATUSn	Bidirectional (open drain)	This is a dedicated configuration status pin , not user I/O
	CFGn	Input(Global Reset)	Dedicated configuration control pin. A low transition resets the target device; a low-to-high transition begins configuration. ALL I/O pins tri-state when CFGn is driven low.
	SCLK	Input(PS), output (AS)	In passive serial configuration mode, SCLK is a clock input used to clock configuration data from external device source into CLD device. In active serial configuration mode, SCLK is a clock output from CLD device. (The CLD is a master in this mode). This is a dedicated pin used for configuration.
	SDIN	Input	Dedicated configuration data input pin.
	CEn	Input	Active low chip enable. Dedicated chip enable input used to detect which device is active in a chain of devices. When CEn is low, the device is enable and high when it is disabled.
	CEOn	Output	Output that drive low when device configuration is completed. During multi device configuration, this pin feeds a subsequence device's CEn pin.
	HOLDn	Output	It is used as hold signal for SPI flash during SPI programming.
	SDO	I/O, Output	Active serial data output from the CLD device. In passive serial configuration, this pin becomes user I/O pin.
	CSOn	I/O, Output	Chip select output to enable/disable a serial configuration device. This output is used during active serial configuration mode. In passive serial configuration mode this pin become user I/O.
	MODE1/MODE0	Input	Dedicated mode select control pins for the configuration mode for the device: 00: Active Serial (Auto Configuration), 01: Passive Serial. If JTAG is selected then bits are ignored.
	TMS	Input	JTAG input pin.
	TDI	Input	JTAG input pin.
	TCK	Input	JTAG input pin.
	TDO	Output	JTAG output pin.

LQFP144: 144-lead Low Profile Quad Flat Package

AG1F1 is available in the 144-lead low profile quad flat package, LQFP144. **Table 5.2** lists all the package pins. They are arranged in pin number and sorted by bank number.

Table5.2 144-lead Low Profile Quad Flat Package Pins on AG1F1 (Part i)

Pin Number	Pin Name (Hardware Name)	Pin Number	Pin Name (Hardware Name)	Pin Number	Pin Name (Hardware Name)
1	IO1 (INTDONE)	28	IO28 (PLL1CLKo)	55	IO55
2	IO2	29	IO29	56	IO56
3	IO3	30	IO30	57	IO57
4	IO4	31	IO31	58	IO58
5	IO5	32	IO32	59	IO59
6	IO6	33	IO33	60	IO60
7	IO7	34	IO34	61	VDDCORE1
8	IO8	35	IO35	62	VSSCORE1
9	VDDIO1_0	36	IO36	63	VSSIO2_2
10	VSSIO1_0	37	IO37	64	VDDIO2_2
11	IO11 (VREF0B1)	38	IO38	65	IO65 (VREF1B2)
12	IO12	39	IO39	66	IO66
13	IO13	40	IO40	67	IO67
14	IO14	41	IO41	68	IO68
15	IO15	42	IO42	69	IO69
16	IO16	43	VSSIO2_0	70	HOLDn (IO70)
17	IO17	44	VDDIO2_0	71	CEOn
18	IO18	45	VDDCORE0	72	CEn
19	IO19	46	VSSCORE0		
20	IO20	47	IO47 (VREF0B2)		
21	IO21	48	IO48		
22	IO22	49	IO49		
23	IO23	50	IO50		
24	IO24	51	IO51		
25	VDDIO1_2	52	IO52		
26	VSSIO1_2	53	IO53		
27	IO27 (VREF1B1)	54	IO54		

Table5.2 144-lead Low Profile Quad Flat Package Pins on AG1F1 (Part ii)

Pin Number	Pin Name (Hardware Name)	Pin Number	Pin Name (Hardware Name)	Pin Number	Pin Name (Hardware Name)
73	SCLK	97	IO97	121	IO121
74	SDIN	98	VSSIO3_2	122	IO122
75	SDO	99	VDDIO3_2	123	IO123
76	CSOn	100	IO100	124	IO124
77	IO77	101	IO101	125	IO125
78	IO78	102	IO102	126	IO126
79	IO79	103	IO103	127	IO127
80	IO80	104	IO104	128	IO128
81	IO81	105	IO105	129	IO129
82	IO82	106	IO106	130	IO130
83	VSSIO3_0	107	IO107	131	IO131
84	VDDIO3_0	108	IO108	132	TMS
85	IO85	109	CFGDONE	133	TDO
86	IO86	110	CFGSTATUSn	134	CFGn
87	IO87	111	MODE0	135	VSSIO4_2
88	IO88	112	MODE1	136	VDDIO4_2
89	IO89	113	VSS IO4_0	137	VDDCORE3
90	IO90	114	VDDIO4_0	138	VSSCORE3
91	IO91	115	VDDCORE2	139	TCK
92	IO92	116	VSSCORE2	140	TDI
93	IO93	117	IO117	141	CLOCK0
94	IO94	118	IO118	142	CLOCK1
95	IO95	119	IO119	143	VDDA_PLL1
96	IO96	120	IO120	144	VSSA_PLL1

Notes:

(1) Output of PLL in AG1F1 should be connected to a dedicated pin – IO28.

(2) Pin numbers in red indicate that these pins are General Purpose I/Os (GPIOs). They can be programmed to input, output, or inout at LVCMOS3.3V level.

(3) All the 144 pins are averagely distributed between the four I/O banks which are divided by bold lines shown in the table.

Revision History

This section shows the revision history for this document.

Date	Version	Revision
June, 2007.	0.5	Initial Agate Logic Release
November, 2007	0.51	Added read-write waveforms of true dual-port memory mode. Added diagram and read-write waveforms of single-port memory mode. Updated Table 2.2.2. Added Conflict Avoidance. Added notes to DC Characteristics section. Updated Table 5.2. Added note to Table 5.2. Added notes for GPIOs in Table 5.2.
February, 2008	0.52	Minor modification