Using the ATF1500(A) CPLD

The ATF1500(A) is a high-performance, high-density Flash-based complex PLD. It has flexible macrocells which allow implementation of complex logic functions. Registers can be configured as D- or T-type flip-flops or transparent latches. Register controls can be individually selected between global pins or individual product terms. A global bus provides 100% connectivity between macrocells. This eliminates routing bottlenecks, increases logic utilization and enables design changes while holding down pin placements. The single level signal routing provides predictable speed performance. The device also offers logic expansion capability to accommodate wide fan-in designs.

The ATF1500(A) has several power and speed management options, that can be used together or separately. First is the ATF1500L/AL device, which offers Atmel's unique low-power standby mode. When input transitions are not occurring, the "L" device will automatically power-down to a low-power mode. In addition, every ATF1500L/AL device has an optional pin-controlled power-down mode. In this mode, pin 4 (PLCC) is configured as a power-down pin, which is used to put the device in a zero power mode (10 µA typical). Each output also has individual slew rate control. Outputs that do not need to operate at the maximum speed can be slowed down, reducing system noise.

This application note describes the ATF1500(A) architecture, power/speed management features and software support. Examples are given to show how to use the macrocell features in the ABEL (or Atmel-ABEL) and CUPL (or Atmel-CUPL) high level description languages.

Architectural Overview

Block Diagram

A block diagram for the ATF1500(A) is shown in Figure 1. The ATF1500(A) has 32 I/O pins, each associated with a logic macrocell, and 4 input-only pins. The 4 input pins can be also be used for global clock, reset and output enables. Each macrocell also has a buried feedback, allowing the macrocell logic to be used even if the I/O pin is used as an input.

The macrocells are connected by a global bus which routes all of the inputs, I/Os and macrocell feedback signals. All signals on the global bus are available to all 32 macrocells. This eliminates any routing problems and maximizes logic utilization. Each macrocell can also generate a foldback logic term that goes to a regional bus. All foldback signals on each regional bus are available to the 16 macrocells within that region. In addition, the sum terms of up to eight adjacent macrocells can be cascaded together to create sum terms with up to 40 product terms. There are four such cascade "chains" or groups of macrocells.

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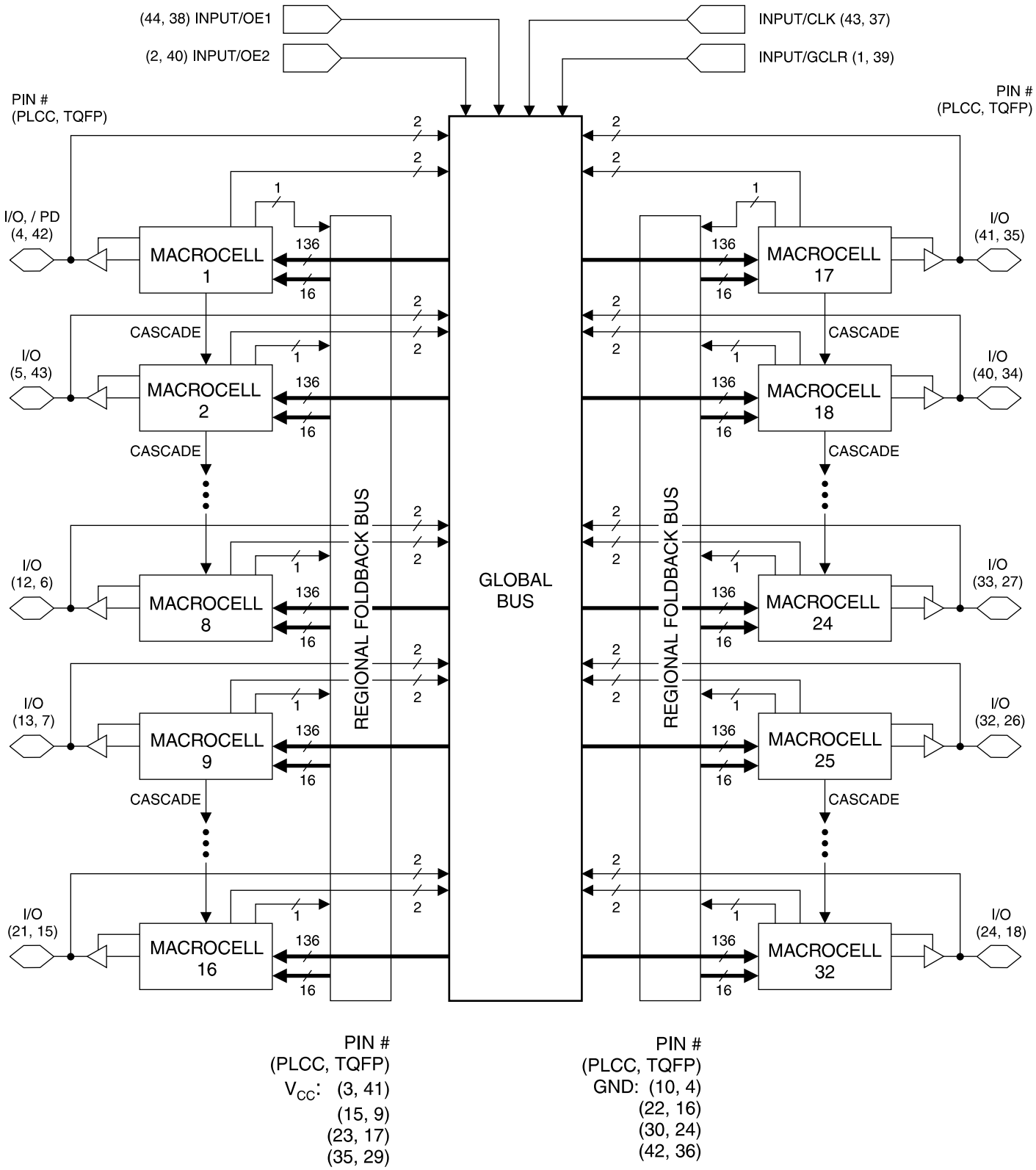
Figure 1. ATF1500(A) Block Diagram



Macrocell

The ATF1500(A) macrocell is shown in Figure 2. Each macrocell has a total of 5 product terms which can be used to implement logic or control functions. The product terms receive inputs from the global and regional buses. The product term select multiplexer will automatically allocate the product terms as needed, depending on the macrocell configuration.

Logic functions are implemented with the OR/XOR/CASCADE logic structure. Up to 5 product terms can be routed to the OR gate. This is used to create a sum-of-products for either a registered or combinatorial function. The OR gate is fed through an XOR gate, which can connect to the input of the register/latch or directly to the I/O pin.

The XOR can be used for different types of functions. When implementing compare or arithmetic functions, the equation can be mapped directly to the XOR, with one input coming from the OR gate and the other from a product term. The XOR can also be configured with OR gate as one input and a fixed one or zero as the other input. This allows it to be used for logic minimization or for output polarity control.

For wide fan-in functions, unused product terms from an adjacent macrocell can be added to the sum term via the CASIN input. The output of the OR gate can be routed to the CASOUT output, which is connected to the CASIN input of the OR gate in the next macrocell. Up to eight macrocells can be cascaded together for a total of 40 product terms. Each stage of the cascade chain will add a small delay. Figure 3 shows a CASCADE logic chain.

Figure 2. ATF1500(A) Macrocell

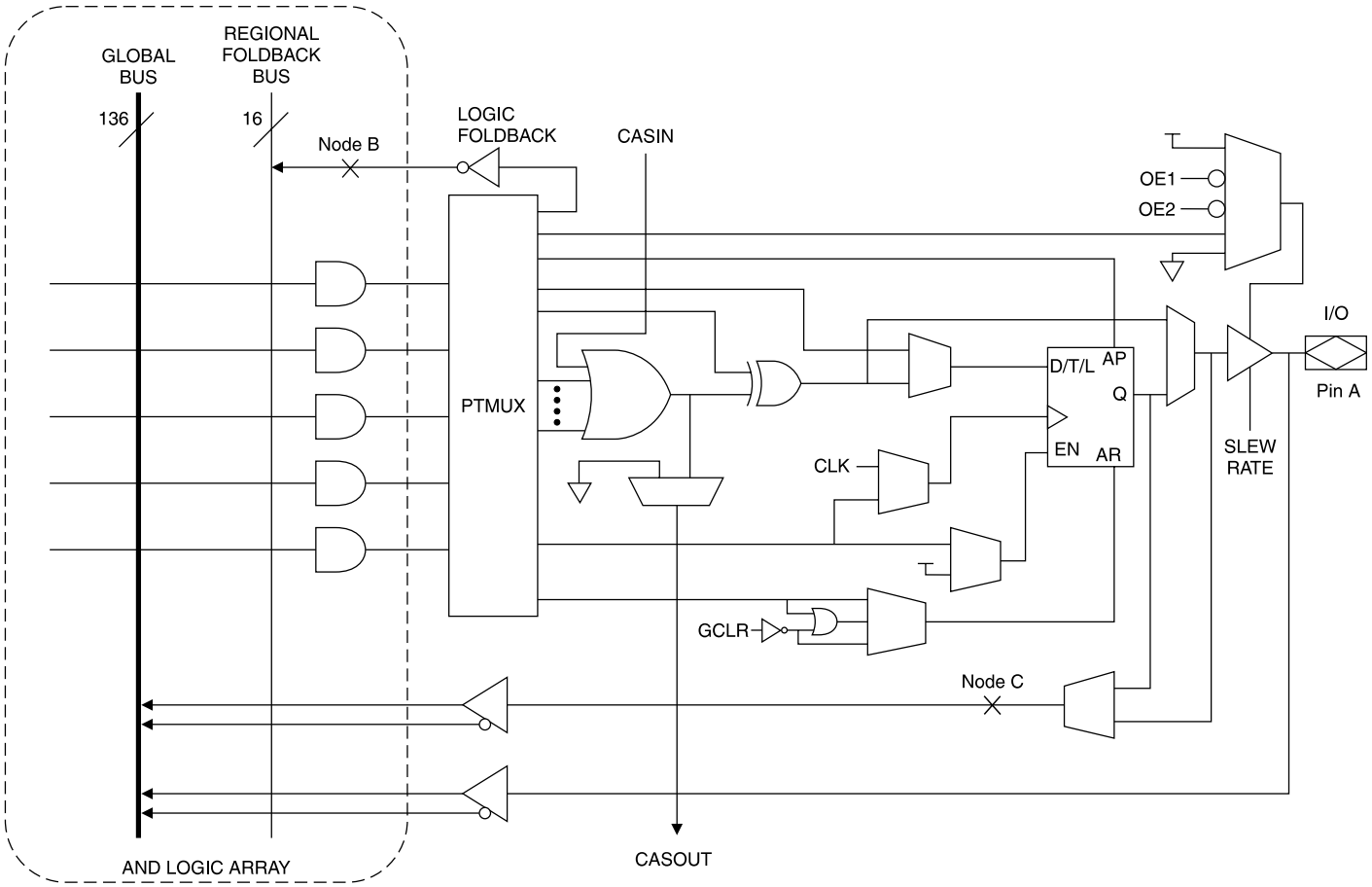
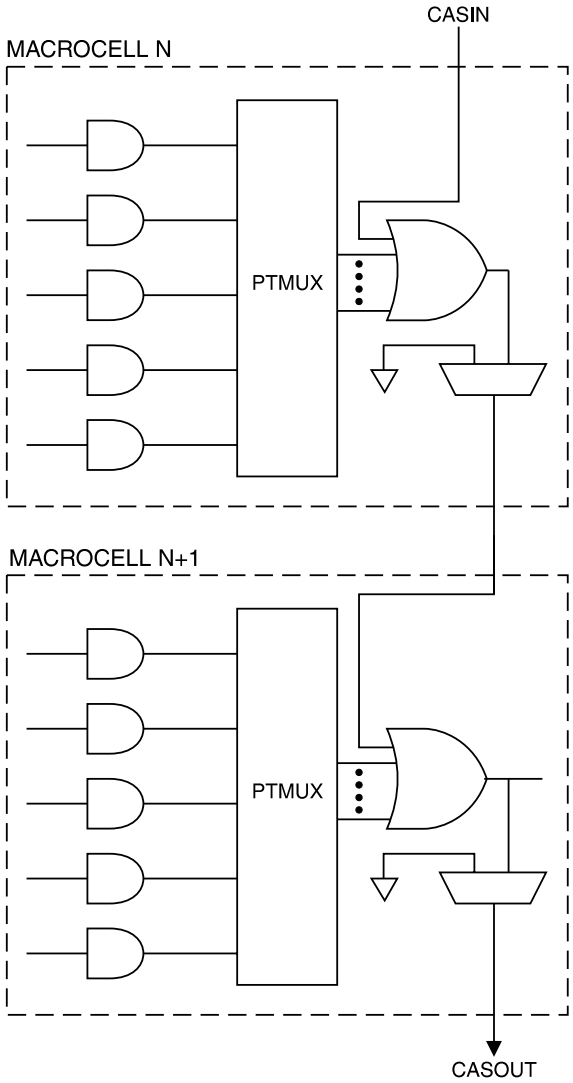


Figure 3. CASCADE Logic Chain



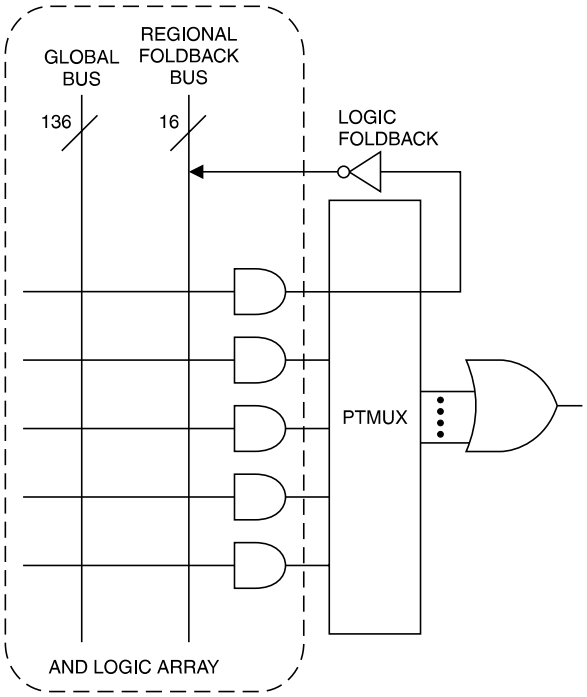
Each macrocell generates two feedbacks into the array, one from the I/O pin and one buried. The independent feedback paths allow multiple functions in the macrocell. In the pin-controlled power-down mode, or if the I/O is configured as an input pin, the macrocell can still be used as a buried node or for logic expansion with the foldback logic term or CASCADE logic. The ATF1500(A) also offers a unique macrocell configuration with a buried register plus an independent combinatorial output.

Each register can be individually configured as either a D- or T-type flip-flop, or a transparent latch. T-type flip-flops can be used to minimize the number of product terms required for functions such as counters. Transparent latches are useful for bus interface types of applications.

The clock, reset and output enable functions can be configured to use either a product term or a global pin. A product term can also be used as a register preset. The product term select mux will automatically allocate product terms for the control functions.

Each macrocell can generate a foldback logic term. This term implements a NAND function that is routed to the regional bus. There are 16 foldback logic terms in each region, which are available to the other macrocells in that region. The foldback logic terms are used primarily for logic expansion, adding a small additional delay. Figure 4 shows a foldback logic term.

Figure 4. Foldback Logic Term



Bus Friendly Pin-keeper Inputs and I/O's

All ATF1500(A) input and I/O pins have bus friendly pin-keeper circuits. The pin-keeper feature is fixed in the ATF1500, but is a programmable option in the ATF1500A device. When a pin is driven high or low, and then left floating, the pin-keeper circuit will keep the pin at the previous high or low level. For unused inputs and I/O pins, the pin-keeper circuit will cause the pin to go to a defined logic state, preventing it from floating to an intermediate voltage level. This reduces power consumption and system noise, and eliminates the need for external pull-up resistors.

The input and I/O pin diagrams are shown in Figure 5.

Power/Speed Management Features

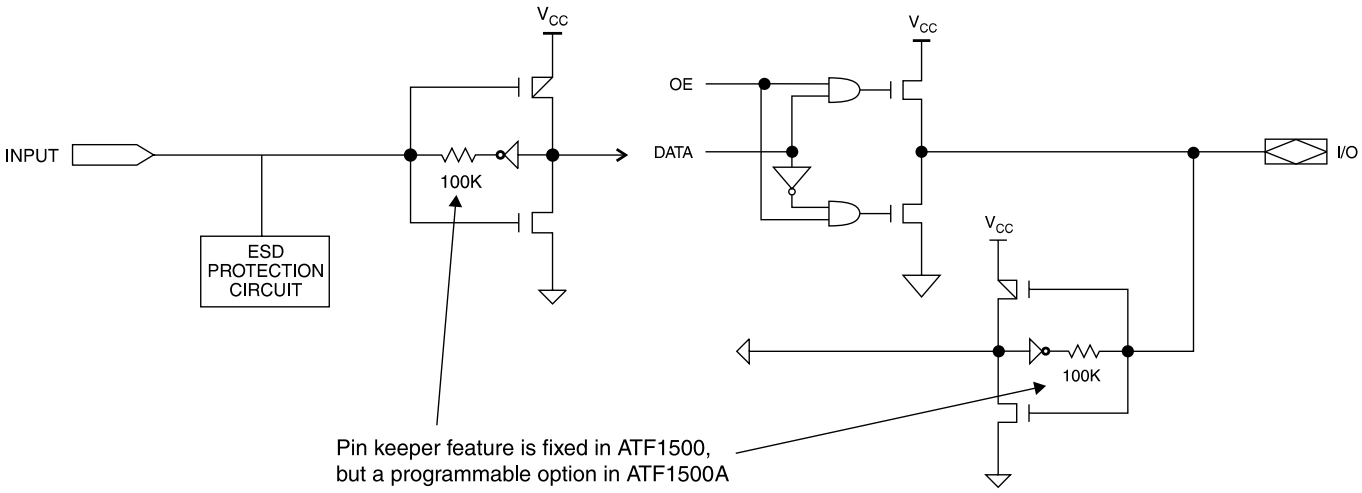
The ATF1500(A) offers several built-in power and speed management options.

The ATF1500L/AL has Atmel's unique Low Power feature. The part will automatically power-down to a low standby power mode when no transitions occur on the inputs or internal feedbacks for some period of time. When an input transition occurs, the device switches to an active mode and responds to the input change. At low frequencies, the device will switch between the standby and active modes, reducing the average current consumption. The delays for switching between the standby and active modes are included in the timing; there are no additional low-power adders. Please refer to the application note "Saving Power with Atmel PLDs" for more information on Atmel "L" devices.

All ATF1500(A) devices also have an optional pin-controlled power-down mode. In this mode, one of the pins is configured as a power-down pin. When the mode is enabled and the pin is high, the device will power-down to a zero power standby mode, dropping the current to 10 µA (typical). All signals are latched and held, and all input transitions are ignored. The pin-controlled power-down mode is specified in the design file.

For speed management, each output has an individual slew rate control. A slower output slew rate will reduce overall system noise. All outputs default to the slower slew rate, and outputs which need to switch at the faster rate must be specified in the design file.

Figure 5. Input and I/O Pin Diagrams



Software Support

The ATF1500(A) is supported by several third-party development tools, including ABEL, CUPL and Synario. An automatic fitter is used to assign pins and nodes, perform error checking and generate a JEDEC file for programming. The fitter defaults can be changed by either adding property statements, by using macros in the design file or by specifying options on the DOS command line. For example:

Property Statements

ABEL and Atmel-ABEL

```
ATMEL property 'DEDICATED_INPUT ON';     "property statement
```

CUPL and Atmel-CUPL

```
property ATMEL {DEDICATED_INPUT ON};     /*property statement */
```

Using Macros

ABEL and Atmel-ABEL

```
library'FIT1500';                        "include macro library
GLOBAL_ALL(ON);                          "use GLOBAL_ALL macro
```

CUPL and Atmel-CUPL

```
$include FIT1500.M                       /*include macro library (FIT1500.M must */
                                         /*reside in the project directory) */
GLOBAL_ALL(ON);                          /*use GLOBAL_ALL macro */
```

Using DOS Command Line

```
FIT1500 <design-file> -str dedicated_input on
```

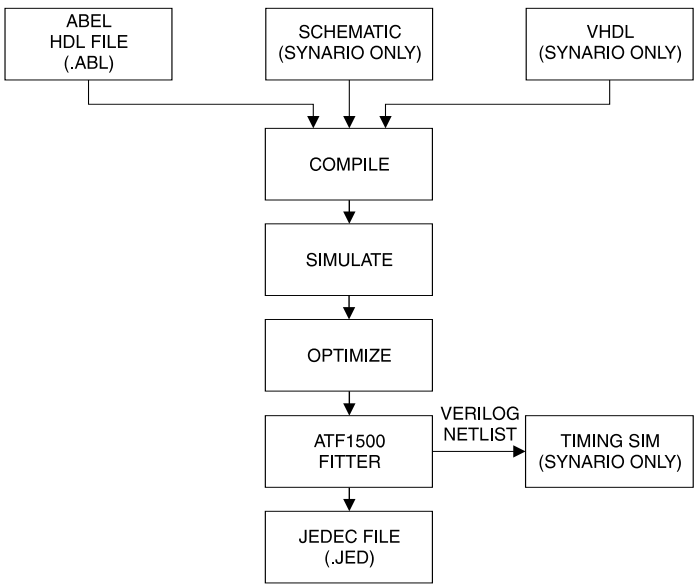
where <design-file> is the name of the ABEL or CUPL design source file.

Please refer to the ATF1500(A) Fitter Manual for a complete description of property statements, macros and details on using the fitter.

ATF1500(A) ABEL/Synario Design Flow

The ATF1500(A) design flow for ABEL or Synario is shown in Figure 6.

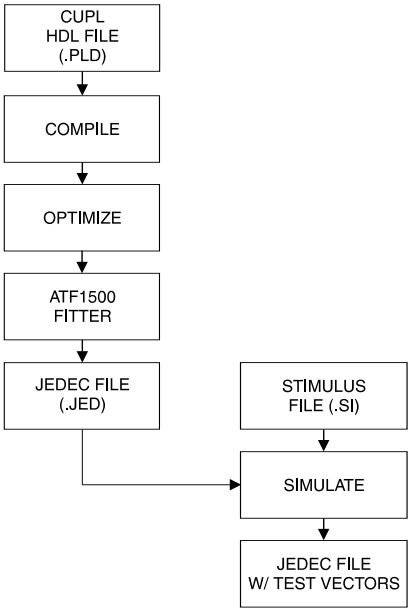
Figure 6. ABEL/Synario Design Flow



ATF1500(A) CUPL Design Flow

The ATF1500(A) design flow for CUPL is shown in Figure 7.

Figure 7. CUPL Design Flow



POF2JED Utility

The POF2JED utility will automatically convert the programming file from a compatible device to a ATF1500(A) JEDEC file. The design can be translated directly, with no speed loss. There are a few options that can be specified during the conversion to control some of the ATF1500(A) unique features:

```
- powerdown               turns ON the power down mode (defaults to OFF)
- slew [AUTO|slow|fast]   sets the slew rate for all outputs
                          AUTO: follows “turbo bit” settings from POF file (default condition)
                          slow: sets output slew rate to slow
                          fast: sets output slew rate to fast
- pinclk                  use global pin clock wherever possible
- race_cover_off          turns off hazard detection option (defaults to on)
```

Note: Executing POF2JED.EXE without any parameters will list the options available in the latest software revision.

Using the ATF1500(A) with ABEL and CUPL

Device Names and Pin/Node Numbers

The device names for the ATF1500(A) for ABEL and CUPL are shown in Table 1.

Table 1. Device Names

Device Type	ABEL Device Name	CUPL Device Name
ATF1500 PLCC	P1500	F1500
ATF1500 TQFP	P1500T	F1500T
ATF1500A PLCC	P1500A	F1500A
ATF1500A TQFP	P1500AT	F1500AT

The buried combinatorial or register nodes, and foldback logic terms are identified by node numbers, as shown in Table 2.

Table 2. Node Numbers

Macrocell #	Pin # PLCC (TQFP)[1]	Foldback Logic Term[2]	Buried COM/REG Node[3]
1	4(42)	45	77
2	5(43)	46	78
3	6(44)	47	79
4	7(1)	48	80
5	8(2)	49	81
6	9(3)	50	82
7	11(5)	51	83
8	12(6)	52	84
9	13(7)	53	85
10	14(8)	54	86
11	16(10)	55	87
12	17(11)	56	88
13	18(12)	57	89
14	19(13)	58	90
15	20(14)	59	91
16	21(15)	60	92
17	41(35)	61	93
18	40(34)	62	94
19	39(33)	63	95
20	38(32)	64	96
21	37(31)	65	97
22	36(30)	66	98
23	34(28)	67	99
24	33(27)	68	100
25	32(26)	69	101
26	31(25)	70	102
27	29(23)	71	103
28	28(22)	72	104
29	27(21)	73	105
30	26(20)	74	106
31	25(19)	75	107
32	24(18)	76	108

Pin numbers: PLCC (TQFP)

Notes: 1. Pin A in Figure 2.
2. Node B in Figure 2.
3. Node C in Figure 2.

The following examples show the device type specification and the pin and node assignments:

ABEL and Atmel-ABEL

```
device_id device 'P1500'; "device_id will be used for JEDEC filename
I1,I2,I43,I44 pin 1,2,43,44;
O4,O5,O6,O7 pin 4,5,6,7 istype 'reg_d,buffer';
O11,O12 pin 11,12 istype 'com';
O16B node 87 istype 'reg_d';
O17B node 88 istype 'com';
```

CUPL and Atmel-CUPL

```
device F1500;
pin [1,2,43,44] = [I1,I2,I43,I44];
pin [7,6,5,4] = [O7,O6,O5,O4];
pin [11,12] = [O11,O12];
pinnode [87,88] = [O16B,O17B];
```

Note that the ATF1500 or ATF1500A fitter will automatically assign pin and node numbers. The design can also be manually fit by assigning pin and node numbers in the source file. In this case, the fitter will perform error and resource checking.

Pin and Node Feedbacks

Each macrocell has two feedback paths to the global bus, one buried (before the output buffer) and one from the I/O pin. When the output is registered, the Q output of the register is fed back into the array on the buried feedback path. If the output is combinatorial, either the output of the XOR or the Q output of the register can be fed back on the buried feedback path. The following examples show how the different feedback paths are identified in the design file:

ABEL and Atmel-ABEL

```
O4.d = I1 # I2;
O11 = O4                "feedback from pin
      # O4.q;            "feedback from register(1)
```

Note: 1. For ABEL, either ".q" or ".fb" can be used to indicate the register feedback path.

CUPL and Atmel-CUPL

```
O4.d = I1 # I2;
O11 = O4.io             /* feedback from pin */
      # O4;             /* feedback from register */
```

D- or T-type Registers and Clock Options

For the ATF1500(A), each register can be configured as an edge-triggered D- or T-type flip-flop. In the flip-flop mode, the data is registered on the rising edge of the clock. Each register can be configured to use either the global CLK pin or an individual clock product term. If the CLK pin is used for the clock, a product term can be used as a clock enable. All clock edges are ignored when the clock enable is low. The following examples show the register and clock configuration options:

ABEL and Atmel-ABEL

```
GLOB_CLK pin 43;
CLK,EN pin 1,2;
O8 pin 8 istype 'reg_t';
O4.d = I1 & I2;           "D-type flip-flop
O8.t = I1 # I2;           "T-type flip-flop
O4.ck = GLOB_CLK;         "global clock pin
O5.ck = CLK & EN;         "clock product term
O8.ck = I2 & EN;          "global clock pin enabled by clock enable product term
O8.ce = GLOB_CLK;
```

CUPL and Atmel-CUPL

```
pin 43 = GLOB_CLK;
pin [2,3] = [CLK,EN];
pin 8 = O8;
O4.d = I1 & I2;           /*D-type flip-flop */
O8.t = I1 # I2;           /*T-type flip-flop */
O4.ck = GLOB_CLK;         /*global clock pin */
O5.ck = CLK & EN;         /*clock product term */
O6.ce = I2 & EN;          /*global clock pin enabled by clock enable product term */
O6.ck = GLOB_CLK;
```

Transparent Latch and Latch Enable

The register can also be configured as a level-triggered transparent latch. In the latch mode, data passes through when the latch enable is high and is latched when the latch enable is low. The latch enable can be configured to use either a product term or the global CLK pin. The following examples show how to define the latch and latch enable:

ABEL and Atmel-ABEL

```
O9,O11 pin 9,11 istype 'reg_g';
I44 pin 43;               "global clock inputs
O9.d = I43 & I44;         "latch input
O9.lh = I44;              "global latch enable
O11.d = I43 # I44;        "latch input
O11.lh = I1 & I2;         "product term latch enable
```

CUPL and Atmel-CUPL

```
pin [9,11] = [O9, O11];
pin 43 = I44;             /*global clock input*/
O9.l = I43 & I44;         /*latch input */
O9.le = I44;              /*global latch enable */
O11.l = I43 # I44;        /*latch input*/
O11.le = I1 & I2;         /*product term latch enable*/
```

Asynchronous Reset and Preset

The asynchronous reset for each register can be configured as either the global pin GCLR (active low), as a product term or disabled. The asynchronous preset for each register can be configured as either a product term or disabled. For the global reset, the register will reset when the pin is low (no clock edge required). For the product term reset or preset, the register will reset or preset when the product term is high (no clock edge required). If no equations are written for the reset or preset, they will default to disabled (always off). The following examples show how the asynchronous reset and preset functions are defined:

ABEL and Atmel-ABEL

```
GCLR pin 1;
O4.ar = !GCLR;            "global pin reset
O5.ar = GCLR;             "product term reset because GCLR is active high
O6.ar = I1 & I2;          "product term reset
O7.ap = I2;               "product term preset
```

CUPL and Atmel-CUPL

```
pin 1 = GCLR;
O4.ar = !GCLR;            /* global pin reset */
O5.ar = GCLR;             /* product term reset because GCLR is active high */
O6.ar = I1 & I2;          /* product term reset */
O7.ap = I2;               /* product term preset */
```

Output Enable

The output enable for each I/O pin can be configured as either one of the two global OE pins (active low), as an individual product term, always enabled (output only) or always disabled (input only). If no output enable equation is written for a declared output, the output will default to always enabled (output only). The output enable for an unused I/O will default to disabled (input only). The following examples show how the output enable functions are defined:

ABEL and Atmel-ABEL

```
OE1,OE2 pin 44,2;
O4.oe = !OE1;             “global pin OE1
O5.oe = !OE2;             “global pin OE2
O6.oe = OE1;              “product term OE because OE1 is active high
O7.oe = I1 & I2;          “product term OE
O8.oe = 1;                “always enabled (output only)
O9.oe = 0;                “always disabled (input only)
```

CUPL and Atmel-CUPL

```
pin [44,2] = [OE1,OE2];
O4.oe = !OE1;             /* global pin OE1 */
O5.oe = !OE2;             /* global pin OE2 */
O6.oe = OE1;              /* product term OE because OE1 is active high */
O7.oe = I1 & I2;          /* product term OE */
O8.oe = ’b’1;             /* always enabled (output only) */
O9.oe = ’b’0;             /* always disabled (input only) */
```

XOR Gate

The ATF1500(A) fitter will automatically map XOR equations to the macrocell XOR gate. The fitter can be forced to map equations directly to the XOR gate by defining the XOR inputs as nodes (without node numbers) as follows:

ABEL and Atmel-ABEL

```
XOR1,XOR2 node;
XOR1 = I1 & I2;
XOR2 = I43 & I44;
O4 = XOR1 $ XOR2;         “force XOR equation to O4 XOR gate
```

CUPL and Atmel-CUPL

```
pinnode   XOR1,XOR2;
XOR1 = I1 & I2;
XOR2 = I43 & I44;
O4 = XOR1 $ XOR2;         /*force XOR equation to O4 XOR gate */
```

The fitter can also use the XOR gate for logic minimization or for polarity control.

Foldback Logic

One of the five product terms in each macrocell can be used to generate a foldback logic term. The product term is inverted (creating a NAND function) and fed back onto the regional bus. The foldback logic term is normally generated automatically by the fitter for logic expansion. It can be specified manually by declaring a foldback logic term node (see node numbers table) or by using a macro or property statement. The equation must be written as a NAND function, for example:

ABEL and Atmel-ABEL

```
FB11 node 51;             “assign to node
FBx node;
ATMEL property ’FOLDBACK_LOGIC = FBx’;          “use  property statement
or
library ’FIT1500’;        “include macro library
FOLDBACK_LOGIC(FBx);      “use macro
FB11 = !(I1 & I2);        “foldback logic term
FBx = !(I43 & I44);       “foldback logic term
O4 = FB11 # FBx;
```

CUPL and Atmel-CUPL

```
pinnode 51 = FB11;        /* assign to node */
pinnode = FBx;
property ATMEL {FOLDBACK_LOGIC = FBx};          /* use property statement */
or
$include FIT1500.M        /* include macro library */
FOLDBACK_LOGIC(FBx)       /* use macro */
FB11 = !(I1 & I2);        /* foldback logic term */
FBx = !(I43 & I44);       /* foldback logic term */
O4 = FB11 # FBx;
```

Cascade Logic

Another way to add more product terms for wide fan-in functions is to use the CASCADE logic. CASCADE logic is used automatically by the fitter software for logic expansion. It is possible to force the fitter to use CASCADE logic for a particular macrocell[1] by using a macro or property statement in the design file. This will cause the fitter to use product terms from the adjacent macrocell via the CASOUT signal. For example:

ABEL and Atmel-ABEL

```
ATMEL property 'CASCADE_LOGIC=O5';              "force fitter to use CASOUT from O4
or
library 'FIT1500';          "include macro library
CASCADE_LOGIC(O5);          "force fitter to use CASOUT from O4
```

CUPL and Atmel-CUPL

```
property ATMEL {CASCADE_LOGIC=O5};              /*force fitter to use CASOUT from O4 */
or
$include FIT1500.M          /*include macro library */
CASCADE_LOGIC(O5);          /*force fitter to use CASOUT from O4 */
```

Note: 1. Macrocells 1, 9, 17, and 25 do not have CASIN inputs.

Creating a Buried Register with a Combinatorial Output

The ATF1500(A) macrocell provides a unique configuration with both a buried register and a combinatorial output in the same macrocell. A single product term is used for the register input, while the remaining product terms are available as inputs to the OR and XOR gates. The registered signal is fed back on the buried feedback path, and the combinatorial output is fed back from the pin. In this configuration, the register is only D-type. See Figure 8. Note that this configuration is automatically utilized by the fitter. The following examples show how to write the equations to manually create this macrocell configuration:

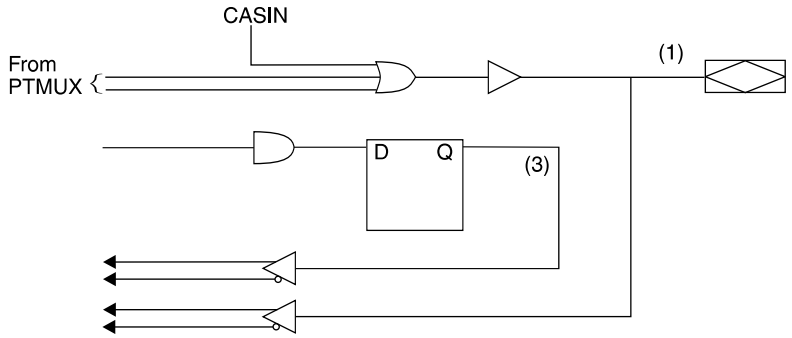
ABEL and Atmel-ABEL

```
O13 pin 13 istype 'com';
O13B node 85 istype 'reg_d'
O13 = I1 & I2;            "combinatorial output
O13B.d = I1 # I2;         "buried register
```

CUPL and Atmel-CUPL

```
pin 13 = O13;
pinnode 85 = O13B;
O13 = I1 & I2;            /*combinatorial output */
O13B.d = I1 # I2;         /*buried register */
```

Figure 8. Buried Register Plus Combinatorial Output Macrocell Configuration.



Pin-controlled Power-down

When the pin-controlled power-down mode is enabled (default is disabled), pin 4 (PLCC) is used as the power-down pin. The logic in the pin 4 (PLCC) macrocell is still available for buried logic functions or logic expansion. The mode is specified in the design file using a property statement or macro, as shown in the following examples:

ABEL and Atmel-ABEL

```
ATMEL property 'SLEEP ON';  "pin-controlled power-down mode enabled, default to pin label
                            "Powerdown. You can use customized pin
                            "label for the Powerdown pin by setting SLEEP = pin_label
or
library 'FIT1500';          "include macro library
SLEEP(ON);                  "pin-controlled power-down mode enabled
```

CUPL and Atmel-CUPL

```
property ATMEL {SLEEP ON};  /*pin-controlled power-down mode enabled */
or
$include FIT1500.M          /*include macro library */
SLEEP(ON);                  /*pin-controlled power-down mode enabled */
```

Slew Rate Control

Each I/O pin has an individual slew rate control. All outputs will default to slow switching. Outputs which need to switch faster must be specified in the design file using the property statement or macro, as shown in the following examples:

ABEL and Atmel-ABEL

```
ATMEL property 'OUTPUT_FAST ON';         "all outputs use fast slew rate
ATMEL property 'OUTPUT_FAST=O4,O5';      "O4,O5 outputs use fast slew rate
or
library 'FIT1500';                       "include macro library
TURBO(ON);                               "all outputs use fast slew rate
TURBO_OUTPUT(O4,O5);                     "O4,O5 outputs use fast slew rate
```

CUPL and Atmel-CUPL

```
property ATMEL {OUTPUT_FAST ON};         /*all outputs use fast slew rate */
property ATMEL {OUTPUT_FAST=O4,O5};      /*O4,O5 outputs use fast slew rate */
or
$include FIT1500.M                       /*include macro library */
TURBO(ON);                               /*all outputs use fast slew rate */
TURBO_OUTPUT(O4);                        /*O4 output use fast slew rate */
TURBO_OUTPUT(O5);                        /*O5 output use fast slew rate */
```

Device Resources

The ATF1500(A) offers a combination of flexible macrocells and global routing, making it predictable and easy to use. The macrocells allow complex logic functions to be implemented with a minimum of product terms. If more product terms are necessary, the CASCADE logic and foldback logic terms can be used for logic expansion, with minimal additional delay. Global routing means that logic can be placed in any macrocell.

Table 3. Device Resources

Inputs	4
I/O pins	32
Macrocells	32
Sum terms	32
Product terms	160
Registers/Latches	32
Max CASCADE product terms	40
Foldback logic terms (per region)	16

The ATF1500(A) fitter will check that the maximums are not exceeded. Since the device is globally routed, there are no limitations on the placement of the logic functions into the macrocells. For logic expansion, foldback logic terms are only available to other macrocells in the same region. The CASCADE logic is organized into four groups of eight adjacent macrocells. Figure 1 shows the CASCADE logic chains.

Timing Calculations

The global bus also simplifies timing calculations. Delays are uniform throughout the part, no matter where the logic is placed. The timing can be easily calculated by hand. The Synario tool also has timing simulation capability. The ATF1500(A) fitter can also output a Verilog timing model for simulation using other Verilog simulators.

Timing depends on the signal source (either an input or I/O pin or internal macrocell feedback path), and destination (I/O pin or internal feedback path). For synchronous logic, the register timing also depends on whether the global clock pin or clock product term is used. For the AR and OE controls, the timing depends on whether global pins or product terms are used. Each stage of CASCADE logic will add a small delay, tCAS. The foldback term delay, tFLD, needs to be added to the delay for inputs that go through the foldback term. If multiple foldback terms are used in parallel for the same logic function, the delay only needs to be added for the slowest input. Figure 9 shows a timing model for the ATF1500(A). Refer to the ATF1500 or ATF1500A datasheet for descriptions and delay values for all timing parameters.

1. Combinatorial output with one level of CASCADE logic: total $t_{PD} = t_{PD} + t_{CAS}$
2. Combinatorial output with multiple levels of CASCADE logic: total $t_{PD} = t_{PD} + nt_{CAS}$, where n = # of CASCADE levels
3. Registered output with one foldback term and slow slew rates outputs:
   total $t_{SU} = t_{FLD} + t_{SFS}$
   total $t_{CO} = t_{COS} + t_{SSO}$

The Power-down Timing model for the ATF1500(A) is shown on Figure 10. This timing depends on the logic state of the power-down pin (PD pin). The ATF1500(A) powers down when the PD pin goes high. All inputs, I/O's, clocks and OE control signals must meet valid time requirements before and after the PD pin goes high. A time delay adder is also required before all signal will be valid after the PD pin goes low. This delay adder does not depend on whether the pin or product clock or OE signal(s) are being used. Refer to the ATF1500 or ATF1500A datasheet for a description of delay values for all timing parameters.

1. Input valid time before PD goes HIGH:
   $t_{VALID} = t_{IVDH}$
2. Input hold time after PD goes HIGH:
   $t_{HOLD} = t_{DHIX}$
3. Output valid time after PD goes LOW:
   $t_{VALID} = t_{DLOV}$

Conclusion

The ATF1500(A) is a high-performance, high-density complex PLD. It combines a flexible macrocell, fully connected logic array, and variety of speed and power management features. The automatic fitter makes it easy to use. The ATF1500(A) uses Atmel's advanced Flash technology, providing reprogrammability and proven reliability. Programming is based on a serial algorithm, reducing programming time to less than 10 seconds.

Figure 9. ATF1500(A) Timing Model

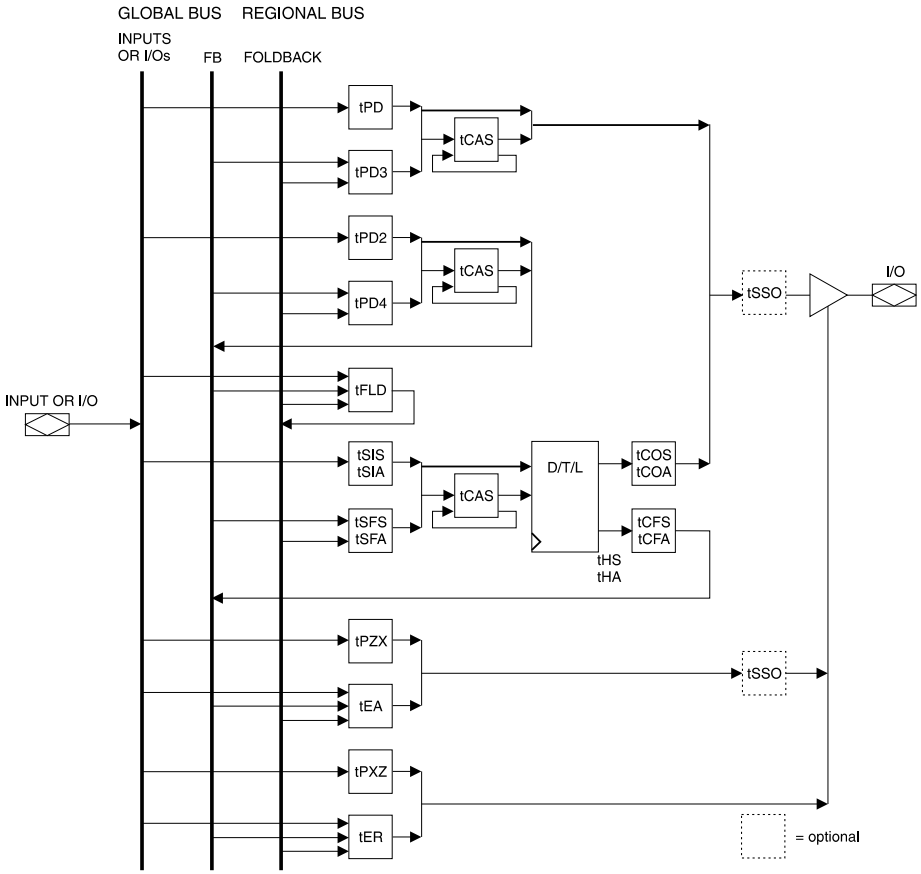
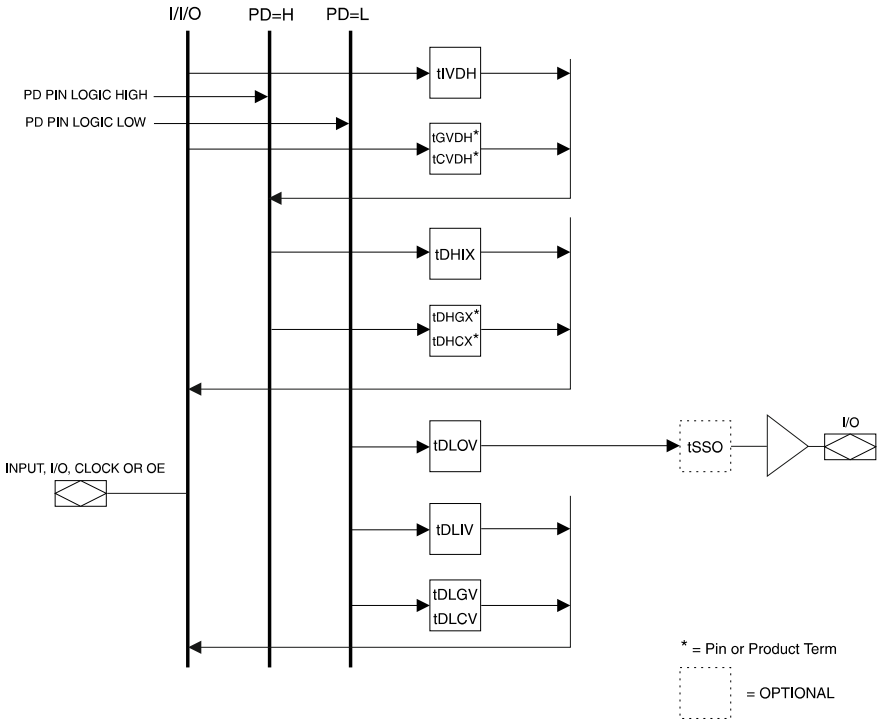


Figure 10. ATF1500(A) Power-down Timing Model



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