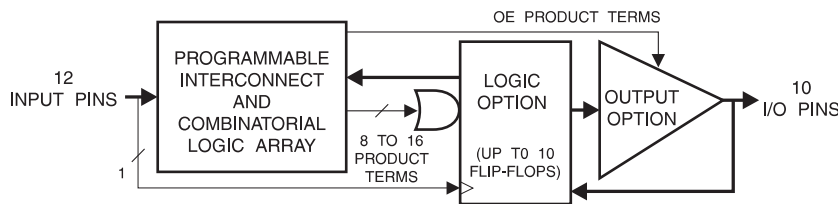


## Features

- 3.0V to 5.5V Operating Range
- Advanced Low-voltage, Zero-power, Electrically-erasable Programmable Logic Device
- Edge-sensing “Zero” Power
- Low-voltage Equivalent of ATF22V10CZ
- “Zero” Standby Power (25  $\mu$ A Maximum)
- Ideal for Battery Powered Systems
- 25 ns Maximum Propagation Delay
- CMOS and TTL Compatible Inputs and Outputs
- Latch Feature Hold Inputs to Previous Logic States
- Advanced EE Technology
  - Reprogrammable
  - 100% Tested
- High-reliability CMOS Process
  - 20 Year Data Retention
  - 100 Erase/Write Cycles
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Commercial and Industrial Temperature Ranges
- Dual-in-line and Surface Mount Standard Pinouts
- Inputs are 5V Tolerant

## Block Diagram

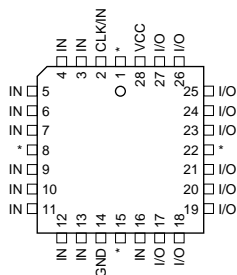


## Pin Configurations

All Pinouts Top View

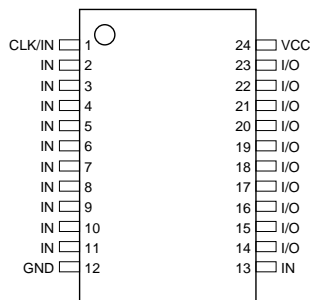
Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
VCC	(3 to 5.5V) Supply

PLCC



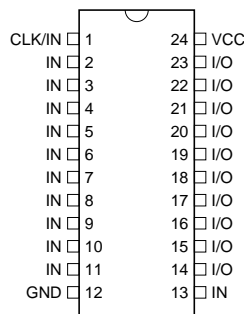
Note: For PLCC, pins 1, 8, 15, and 22 can be left unconnected. For superior performance, connect VCC to pin 1 and GND to pins 8, 15, and 22.

TSSOP



Note: TSSOP is the smallest package of SPLD offering.

DIP/SOIC



High-performance  
EE PLD

ATF22LV10CZ





## Description

The ATF22LV10CZ is a high-performance CMOS (Electrically-erasable) Programmable Logic Device (PLD) which utilizes Atmel's proven electrically-erasable Flash memory technology and provides 25 ns speed with stand-by current of 25  $\mu$ A maximum. All speed ranges are specified over the 3.0V to 5.5V range for industrial and commercial temperature ranges.

The ATF22LV10CZ provides a low-voltage and edge-sensing "zero" power CMOS PLD solution with "zero" standby power (5  $\mu$ A typical). The ATF22LV10CZ powers down automatically to the zero power mode through Atmel's patented Input Transition Detection (ITD) circuitry when the device is idle. The ATF22LV10CZ is capable of operating at supply voltages down to 3.0V. Pin "keeper" circuits on

input and output pins hold pins to their previous logic levels when idle, which eliminate static power consumed by pull-up resistors.

The ATF22LV10CZ macrocell incorporates a variable product term architecture. Each output is allocated from 8 to 16 product terms which allows highly complex logic functions to be realized. Two additional product terms are included to provide synchronous reset and asynchronous reset. These additional product terms are common to all 10 registers and are automatically cleared upon power-up. Register Preload simplifies testing. A Security Fuse prevents unauthorized copying of programmed fuse patterns.

## Absolute Maximum Ratings\*

Temperature Under Bias.....	-40°C to +85°C
Storage Temperature .....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground .....	-2.0V to +7.0V <sup>(1)</sup>
Voltage on Input Pins with Respect to Ground During Programming.....	-2.0V to +14.0V <sup>(1)</sup>
Programming Voltage with Respect to Ground .....	-2.0V to +14.0V <sup>(1)</sup>

\*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is  $V_{CC} + 0.75V$  DC, which may overshoot to 7.0V for pulses of less than 20 ns.

## DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient)	0°C - 70°C	-40°C - 85°C
VCC Power Supply	3.0V - 5.5V	3.0V - 5.5V

## Functional Logic Diagram Description

The Functional Logic Diagram describes the ATF22LV10CZ architecture.

The ATF22LV10CZ has 12 inputs and 10 I/O macrocells. Each macrocell can be configured into one of four output configurations: active-high/low or registered/combinatorial. The universal architecture of the ATF22LV10CZ can be programmed to emulate most 24-pin PAL devices.

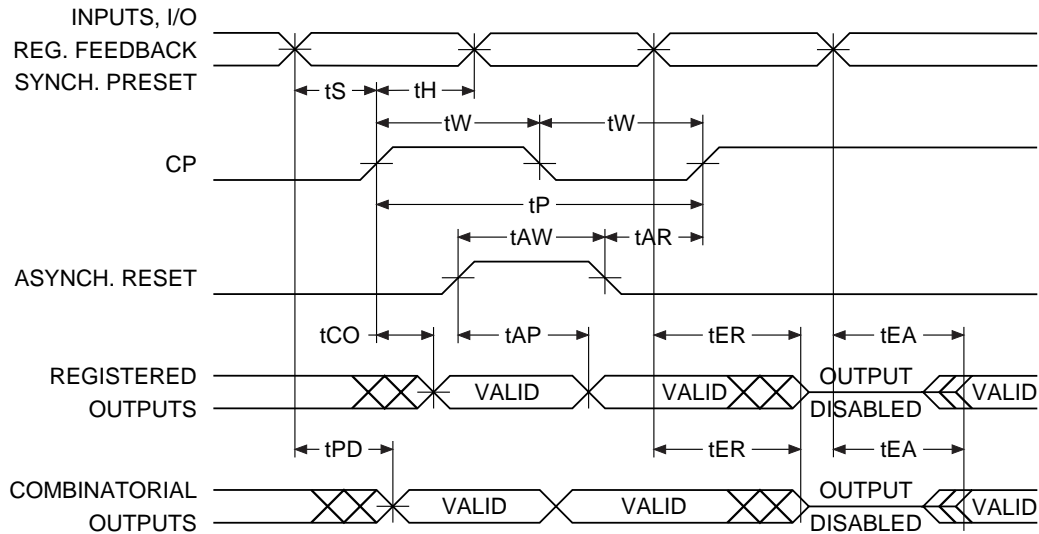
Unused product terms are automatically disabled by the compiler to decrease power consumption. A Security Fuse, when programmed, protects the contents of the ATF22LV10CZ. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the Security Fuse.

## DC Characteristics

Symbol	Parameter	Condition <sup>(2)</sup>	Min	Typ	Max	Units
$I_{IL}$	Input or I/O Low Leakage Current	$0 \leq V_{IN} \leq V_{IL} \text{ (Max)}$			-10	$\mu\text{A}$
$I_{IH}$	Input or I/O High Leakage Current	$(V_{CC} - 0.2)V \leq V_{IN} \leq V_{CC}$			10	$\mu\text{A}$
$I_{CC}$	Clocked Power Supply Current	$V_{CC} = \text{Max}$ Outputs Open, $f = 15 \text{ MHz}$	Com	55	85	$\text{mA}$
			Ind	60	90	$\text{mA}$
$I_{SB}$	Power Supply Current, Standby	$V_{CC} = \text{Max}$ $V_{IN} = \text{Max}$ Outputs Open	Com	5	25	$\mu\text{A}$
			Ind	5	50	$\mu\text{A}$
$I_{OS}^{(1)}$	Output Short Circuit Current	$V_{OUT} = 0.5V$			-130	$\text{mA}$
$V_{IL}$	Input Low Voltage		-0.5		0.8	V
$V_{IH}$	Input High Voltage		2.0		$V_{CC} + 0.75$	V
$V_{OL}$	Output Low Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CC} = \text{Min}$ , $I_{OL} = 16 \text{ mA}$	Com.		0.5	V
			Ind.			
$V_{OH}$	Output High Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CCIO} = \text{Min}$ , $I_{OH} = -2.0 \text{ mA}$	2.4			V
$V_{OH}$	Output High Voltage	$I_{OH} = -100 \mu\text{A}$	$V_{CC} - 0.2V$			V

- Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.  
2. For DC characterization, the test condition of  $V_{CC} = \text{Max}$  corresponds to 3.6V.

## AC Waveforms

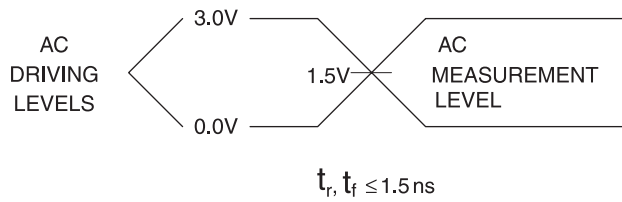


## AC Characteristics<sup>(1)</sup>

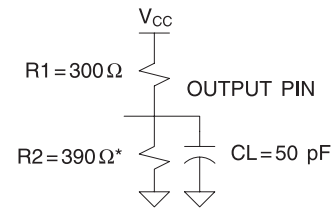
Symbol	Parameter	-25		Units
		Min	Max	
$t_{PD}$	Input or Feedback to Non-Registered Output	3	25	ns
$t_{CF}$	Clock to Feedback		13	ns
$t_{CO}$	Clock to Output	2	15	ns
$t_S$	Input or Feedback Setup Time	15		ns
$t_H$	Input Hold Time	0		ns
$t_P$	Clock Period	25		ns
$t_W$	Clock Width	12.5		ns
$F_{MAX}$	External Feedback $1/(t_S + t_{CO})$	33.3		MHz
	Internal Feedback $1/(t_S + t_{CF})$	35.7		MHz
	No Feedback $1/(t_P)$	40.0		MHz
$t_{EA}$	Input to Output Enable	3	25	ns
$t_{ER}$	Input to Output Disable	3	25	ns
$t_{AP}$	Input or I/O to Asynchronous Reset of Register	3	25	ns
$t_{SP}$	Setup Time, Synchronous Preset	15		ns
$t_{AW}$	Asynchronous Reset Width	25		ns
$t_{AR}$	Asynchronous Reset Recovery Time	25		ns
$t_{SPR}$	Synchronous Preset to Clock Recovery Time	15		ns

Note: 1. See ordering information for valid part numbers.

## Input Test Waveforms and Measurement Levels



## Output Test Loads



Note: Similar competitors devices are specified with slightly different loads. These load differences may affect output signals' delay and slew rate. Atmel devices are tested with sufficient margins to meet compatible device specification conditions.

## Pin Capacitance

$f = 1\text{ MHz}, T = 25^\circ\text{C}^{(1)}$

	Typ	Max	Units	Conditions
$C_{IN}$	5	8	pF	$V_{IN} = 0V$
$C_{I/O}$	6	8	pF	$V_{OUT} = 0V$

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

## Power-up Reset

The registers in the ATF22LV10CZ are designed to reset during power-up. At a point delayed slightly from VCC crossing VRST, all registers will be reset to the low state. The output state will depend on the polarity of the buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how VCC actually rises in the system, the following conditions are required:

1. The VCC rise must be monotonic and start below 0.7V
2. The clock must remain stable during TPR.
3. After TPR, all input and feedback setup times must be met before driving the clock pin high.

## Preload of Register Outputs

The ATF22LV10CZ's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

## Electronic Signature Word

There are 64 bits of programmable memory that are always available to the user, even if the device is secured. These bits can be used for user-specific data.

## Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF22LV10CZ fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

## Programming/Erasing

Programming/erasing is performed using standard PLD programmers. See CMOS PLD Programming Hardware & Software Support for information on software/programming.

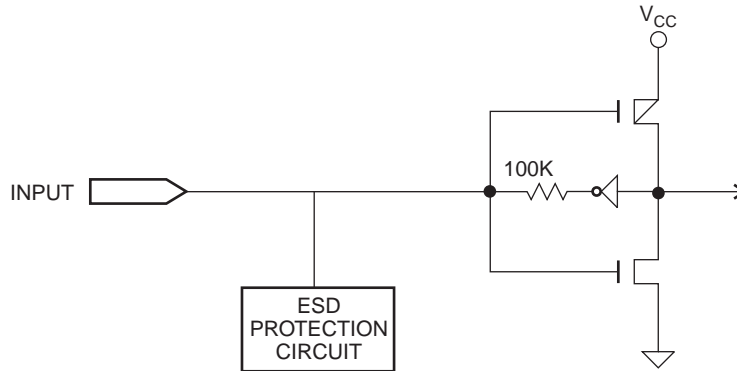
Parameter	Description	Typ	Max	Units
$T_{PR}$	Power-up Reset Time	600	1000	ns
$V_{RST}$	Power-up Reset Voltage	2.3	2.7	V

## Input and I/O Pin Keepers

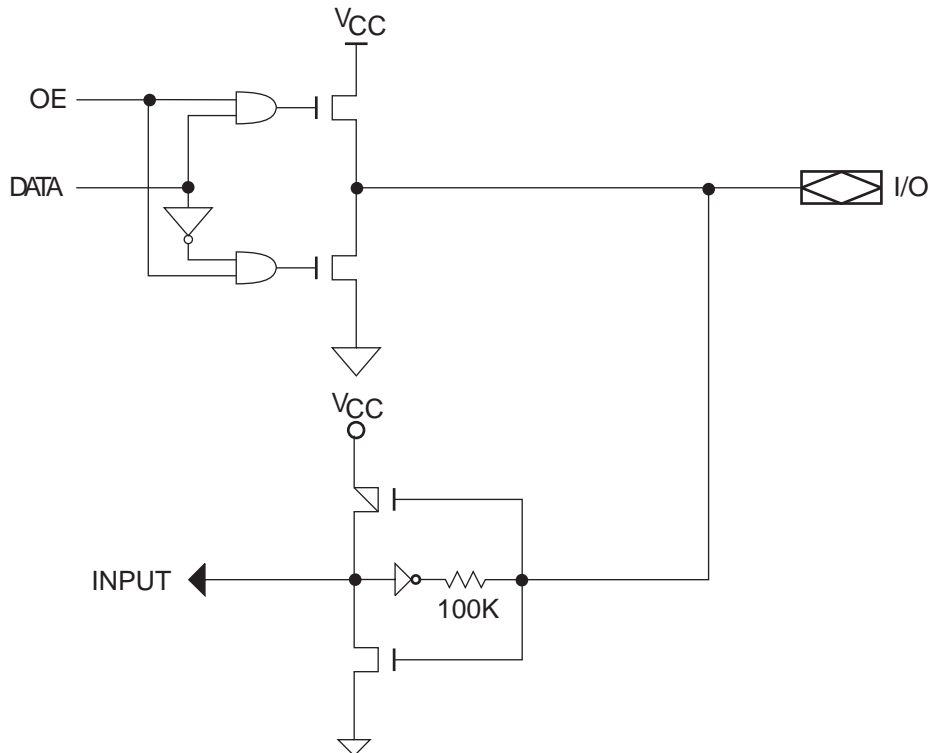
All ATF22LV10CZ family members have internal input and I/O pin-keeper circuits. Therefore, whenever inputs or I/Os are not being driven externally, they will maintain their last driven state. This ensures that all logic array inputs and

device outputs are at known states. These are relatively weak active circuits that can be easily overridden by TTL-compatible drivers (see input and I/O diagrams below).

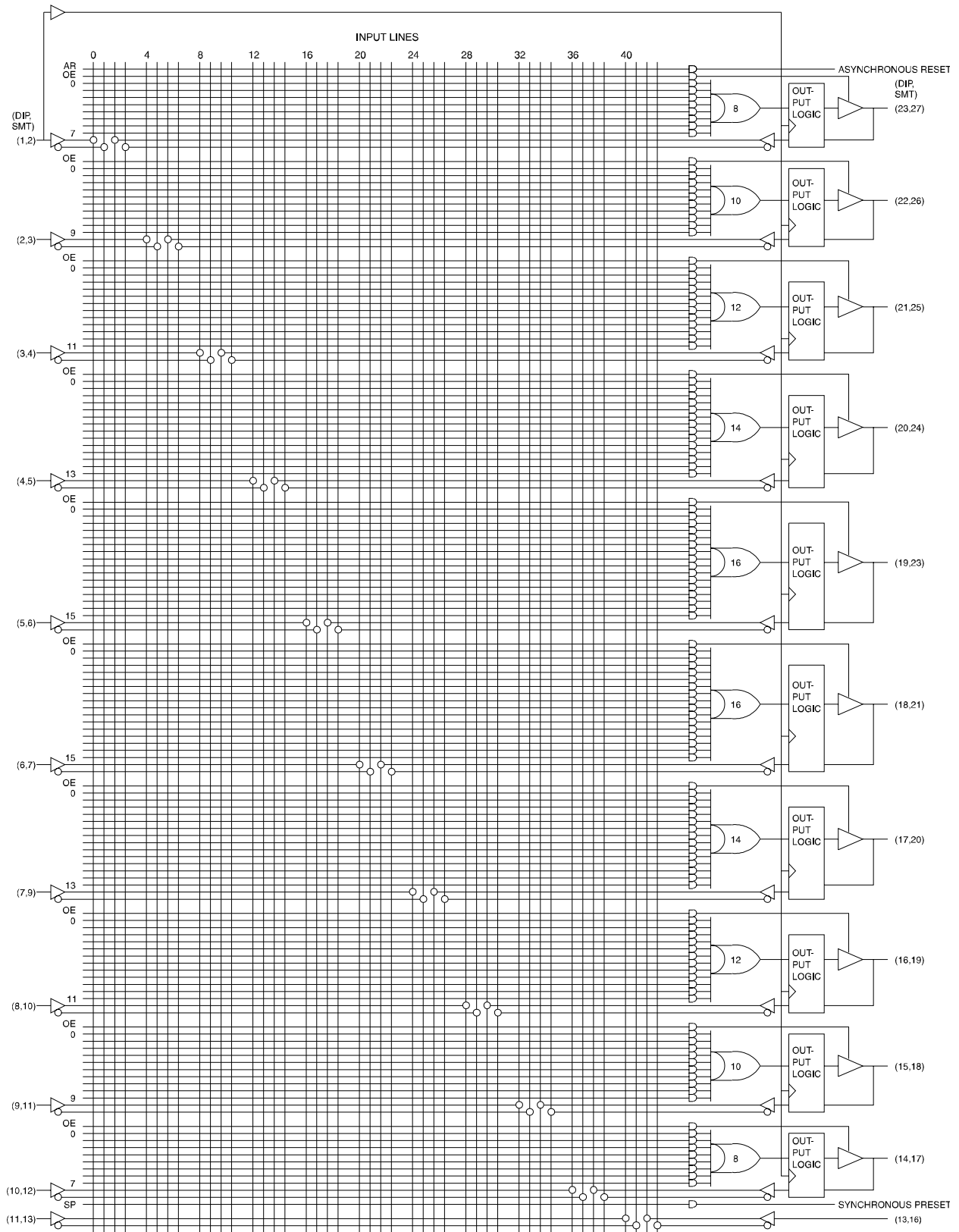
### Input Diagram



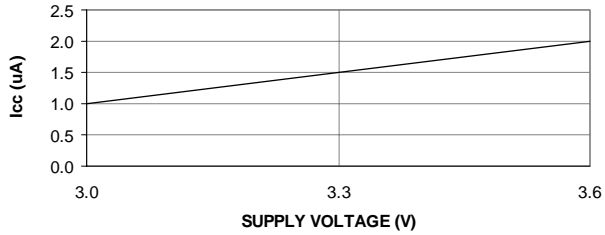
### I/O Diagram



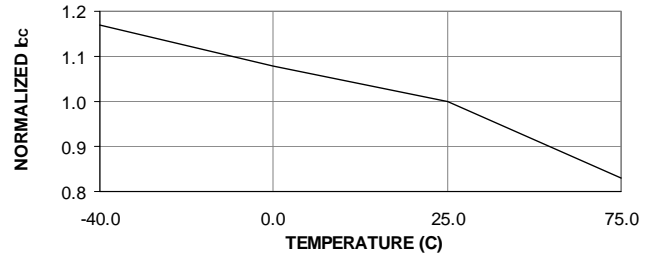
## Functional Logic Diagram ATF22LV10CZ



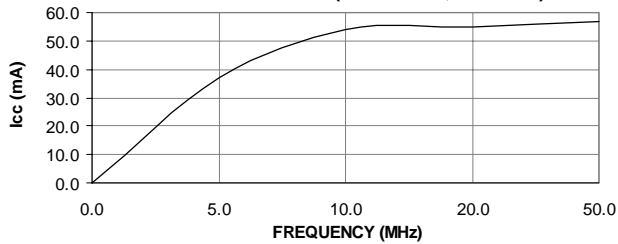
**ATF22LV10CZ SUPPLY CURRENT VS. SUPPLY VOLTAGE (TA = 25C)**



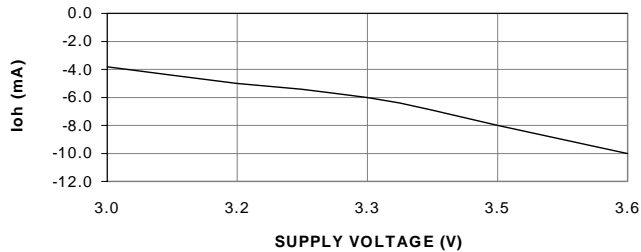
**NORMALIZED I<sub>CC</sub> vs. TEMP**



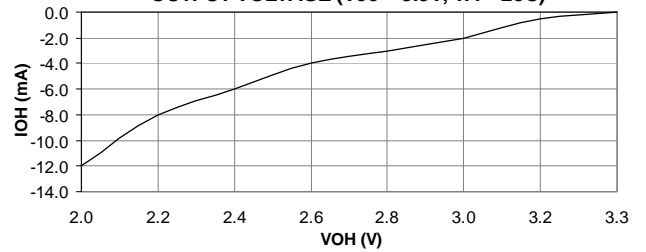
**ATF22LV10CZ SUPPLY CURRENT VS. INPUT FREQUENCY (VCC = 3.3V, TA = 25c)**



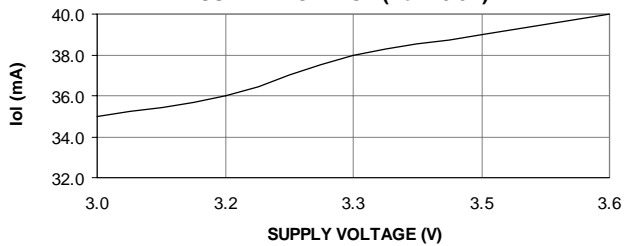
**ATF22LV10C/CZ SOURCE CURRENT VS. SUPPLY VOLTAGE (Voh = 2.4V)**



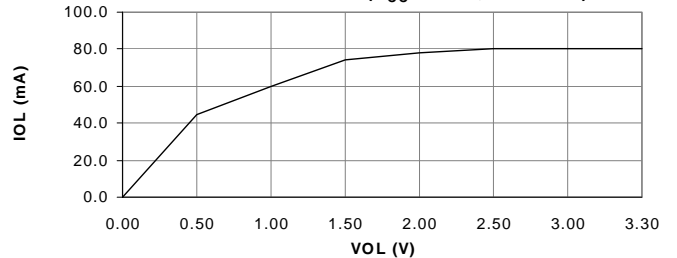
**ATF22LV10C/CZ OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE (Vcc = 3.3V, TA = 25C)**



**ATF22LV10C/CZ OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE (Vol = 0.5V)**

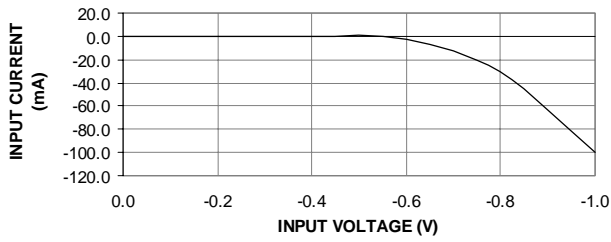


**ATF22LV10C/CZ OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE (Vcc = 3.3V, TA = 25C)**

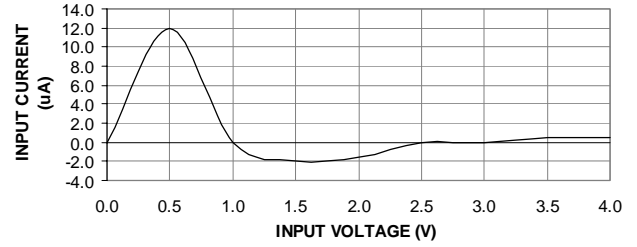




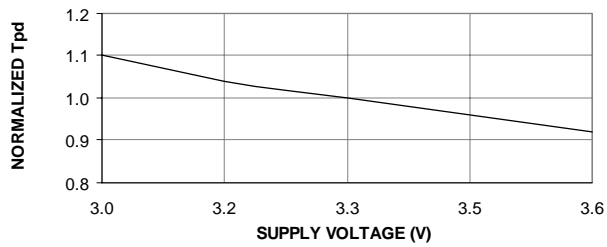
**ATF22LV10C/CZ INPUT CLAMP CURRENT VS. INPUT VOLTAGE ( $V_{CC} = 3.3V$ ,  $T_A = 25C$ )**



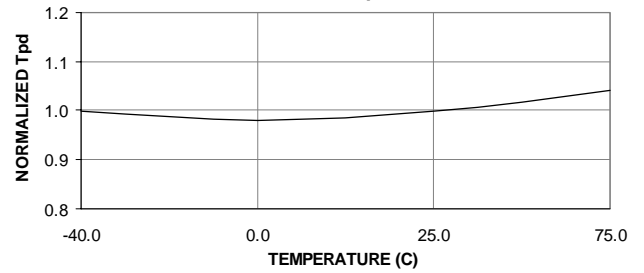
**ATF22LV10C/CZ INPUT CURRENT VS. INPUT VOLTAGE ( $V_{CC} = 3.3V$ ,  $T_A = 25C$ )**



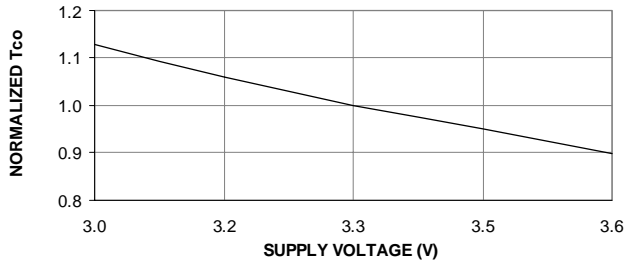
**NORMALIZED Tpd VS Vcc**



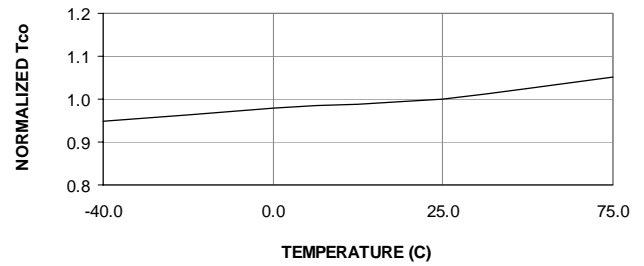
**NORMALIZED Tpd VS TEMP**



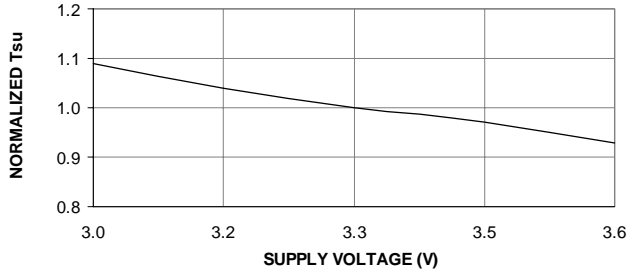
**NORMALIZED Tco VS Vcc**



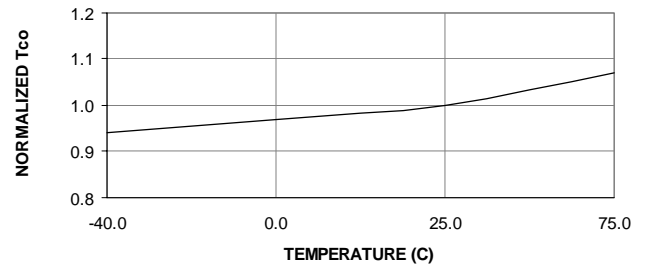
**NORMALIZED Tco VS TEMP**



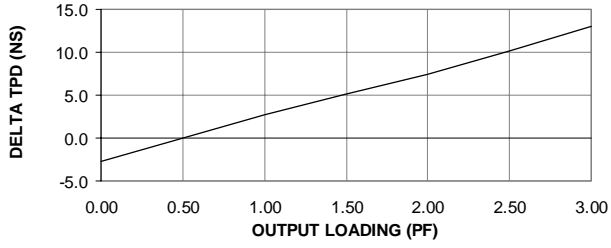
**NORMALIZED Tsu VS Vcc**



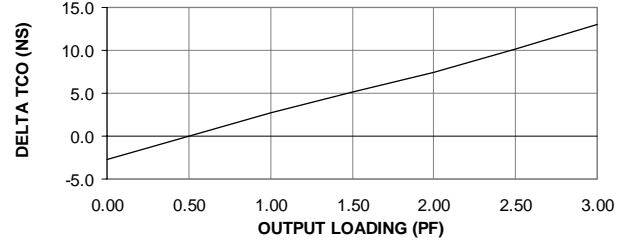
**NORMALIZED Tsu VS TEMP**



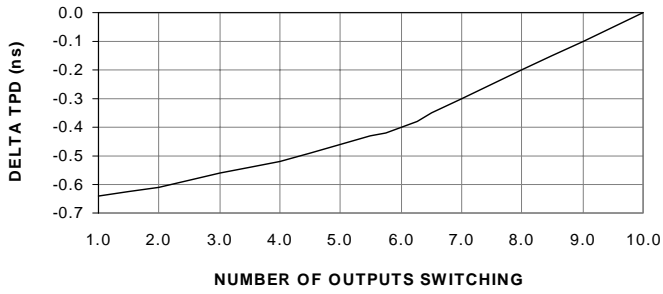
**22LV10C/CZ DELTA T<sub>PD</sub> vs.  
OUTPUT LOADING**



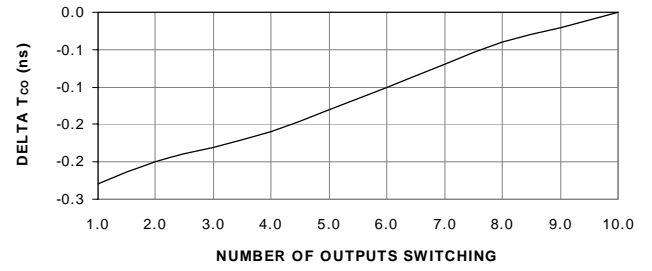
**22LV10C/CZ DELTA T<sub>CO</sub> vs.  
OUTPUT LOADING**



**DELTA T<sub>PD</sub> VS # OF OUTPUT SWITCHING**



**DELTA T<sub>CO</sub> VS # OF OUTPUT SWITCHING**



## Ordering Information

$t_{PD}$ (ns)	$t_S$ (ns)	$t_{CO}$ (ns)	Ordering Code	Package	Operation Range
25	15	15	ATF22LV10CZ-25JC ATF22LV10CZ-25PC ATF22LV10CZ-25SC ATF22LV10CZ-25XC	28J 24P3 24S 24X	Commercial (0°C to 70°C)
	15	15	ATF22LV10CZ-25JI ATF22LV10CZ-25PI ATF22LV10CZ-25SI ATF22LV10CZ-25XI	28J 24P3 24S 24X	Industrial (-40°C to +85°C)

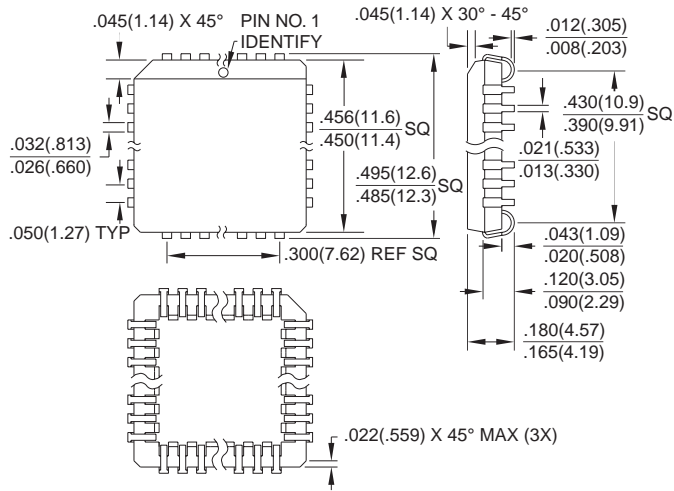
## Using “C” Product for Industrial

To use commercial product for industrial temperature ranges, simply de-rate  $I_{CC}$  by 15% on the “C” device. No speed de-rating is necessary.

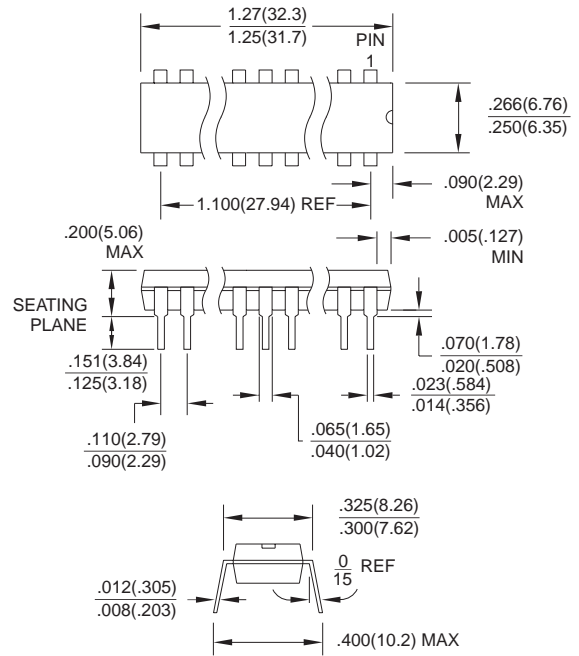
Package Type	
<b>28J</b>	28-lead, Plastic J-leaded Chip Carrier (PLCC)
<b>24P3</b>	24-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
<b>24S</b>	24-lead, 0.300" Wide, Plastic Gull-wing Small Outline (SOIC)
<b>24X</b>	24-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)

## Packaging Information

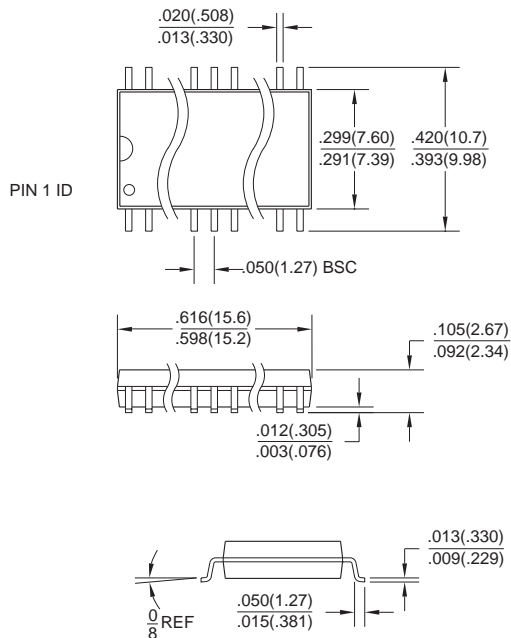
**28J**, 28-lead, Plastic J-leaded Chip Carrier (PLCC)  
 Dimensions in Inches and (Millimeters)  
 JEDEC STANDARD MS-018 AB



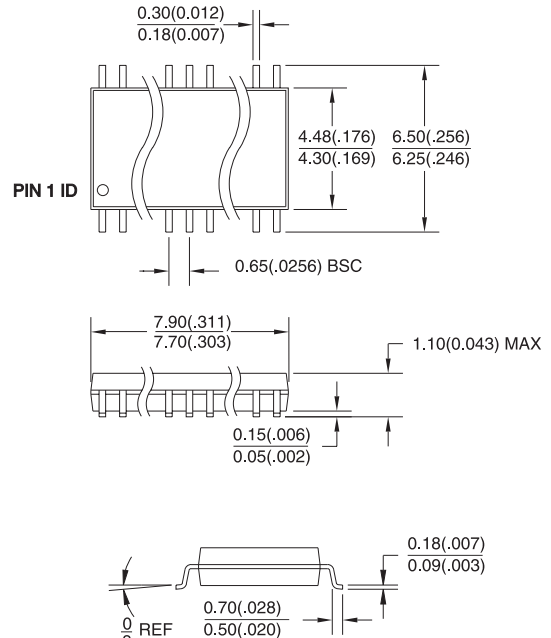
**24P3**, 24-lead, 0.300" Wide,  
 Plastic Dual Inline Package (PDIP)  
 Dimensions in Inches and (Millimeters)  
 JEDEC STANDARD MS-001 AF



**24S**, 24-lead, 0.300" Wide,  
 Plastic Gull-wing Small Outline (SOIC)  
 Dimensions in Inches and (Millimeters)



**24X**, 24-lead, 4.4 mm Wide, Plastic Thin Shrink  
 Small Outline (TSSOP)  
 Dimensions in Inches and (Millimeters)





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