CPLD Design Hints for Atmel-Synario

Introduction

Atmel-Synario is a versatile product capable of supporting mixed-mode (i.e. Schematic, ABEL and VHDL) entry with many levels of design hierarchy. It is an upgradable version of the Data-IO's Synario™ tool which specifically supports Atmel PLD and CPLD devices. This article will provide hints for new or experienced users on how to use Atmel-Synario to efficiently implement their designs into Atmel PLD and CPLD devices.

Preventing Node Collapsing

When Atmel-Synario flattens your design hierarchy it will, when necessary, automatically collapse any buried combinatorial nodes in the design. Because this process is device independent and does not take into account the architectural requirements of the target device, the flattened design may generate too many product terms to fit. A resolution to this is to prevent certain nodes such as; combinatorial nodes with multiple fanouts, many product term logic or flip-flop control signals, from being collapsed. Retaining these nodes can reduce the amount of product terms generated per node. Figure 1 shows a portion of a design with multiple product terms for the flip-flop reset signal(s). The output of the 2-to-1 multiplexer (net labeled MUX) is connected to the RST input of a 4-bit counter block. When collapsed by Atmel-Synario, this design generates two product terms for the asynchronous reset (AR) input for the counter's registers. If this design were targeted to devices with only one AR product term per register (i.e ATV750B, ATV2500B) it would not fit. To fit this design, select the net attribute for the MUX net and set the *Keep* attribute equal to Yes (Keep = y). Atmel-Synario will retain the MUX net as a buried combinatorial node and input this node to the AR product term. If this design were an ABEL file you can preserve the MUX net by defining it to be a node with the *Keep* istype attribute. For example,

```
MUX node istype `Keep';
```

@Carry Directive

The `@Carry` Directive can be used to reduce logic generated for adders, counters and comparators. This compiler directive can only be used in ABEL designs. The value, specified by the `@Carry` directive indicates the maximum bit width to use when synthesizing a logic function. For example, Figure 2 shows an ABEL file for an 8-bit equality comparator. This logic when synthesized would require 256 product terms, which can be difficult to fit for any device. By using the `@Carry` directive this comparator was broken up into a chain of four 2-bit comparators consisting of 16 product terms.

Atmel-Synario Generic and Atmel Specific Schematic Primitives

The schematic primitives symbols you use can affect the way Atmel-Synario will process your schematic. Using the Atmel-Synario Generic primitives allow you to port your design into any PLD or CPLD. However, to fully use the features and performance of Atmel CPLD's, you

Atmel-Synario Design Hints

Application Note

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Figure 1. Selecting the Keep Node Attribute

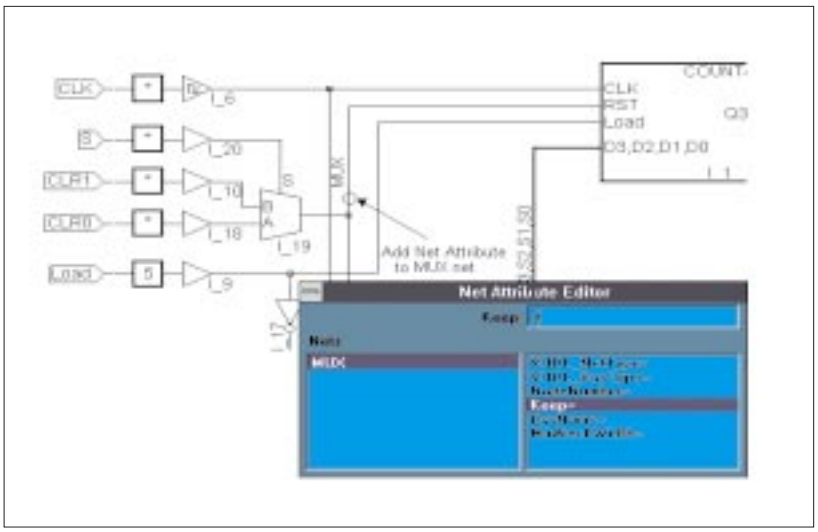

Figure 2. Using the `@Carry` Directive

```
module compare
title '8-bit bus interface equality comparator';

a7..a0  pin;
b7..b0  pin;
aeqb    pin istype 'com';

a = [a7..a0];
b = [b7..b0];

@CARRY 2;

"Generates a chain of 2-bit comparators to
"reduce product term count. Without this
"directive, 256 product terms are used.
"@Carry 4; would generate a chain of 4-bit
"comparators

Equations

aeqb = (a == b);

end
```

should use the Atmel-Specific primitives. The Atmel-Specific primitives save product terms and implement special clocking features unique to Atmel CPLD's. Figure 3 shows a design which uses both Atmel-Specific and Generic primitives and the compiled equations. Both flip-flops in the design are clocked by a pin with an enable signal. The Q1,Q0 outputs use the Atmel-Synario Generic and Atmel-Specific primitives respectively. The Q0 logic implementation saves a product term and maps the clock signal directly into the architecture of the ATV2500B compared to the Q1 logic.

Fitter Properties

Fitter properties allow you to control how Atmel-Synario fits your design. The default fitter property settings generally provide the best fit for most designs. However, you can modify fitter properties to help make a design fit into an Atmel CPLD or tailor the design for your system performance or power consumption requirements. Fitter properties are controlled by selecting ***Properties*** when running the ***Fit Design*** process in the Project Navigator. This generates a Properties listing. A table of useful fitter properties is shown in Figure 4. This table does not describe all the fitter properties available. These are shown in the properties listing. Some properties listed in the table such as *Pin-Preassignments* and *P-term Limit for Collapse* are available for all Atmel devices while the rest are specific to the Atmel ATF1500 device.

Summary

Atmel-Synario is a powerful design entry tool for Atmel CPLD devices. This article discussed hints that allow you to customize it to meet your design requirements and help fit your designs into Atmel CPLD devices. More information regarding these hints is available either within Atmel-Synario's on-line help system or by calling the Atmel PLD Applications Hotline at (408) 436-4333.

Figure 3. Synario-Generic and Atmel-Specific Schematic Primitive Differences

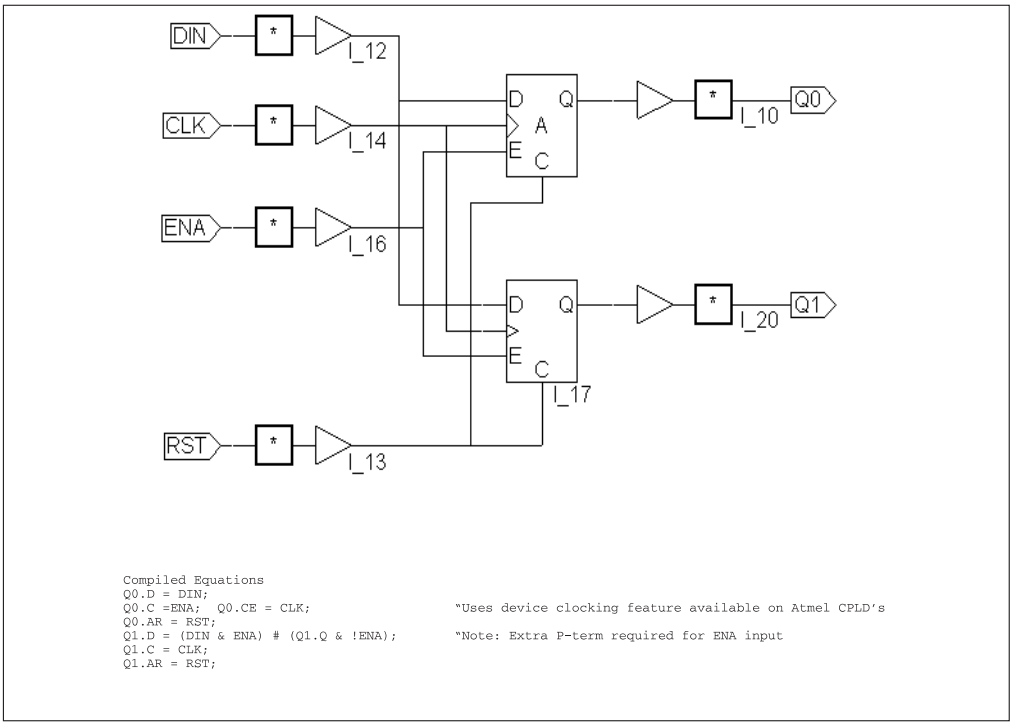

Table 1. Useful Atmel Fitter Properties

Property	Options	Description
Pin-Preassignments	*TRY(default), Keep, Ignore*	*Try*: Fit with Keep Option. If no fit, Ignore. *Keep*: Fit design with original pin/node assignments. *Ignore*: Fitter assigns all pins/nodes during fit.
P-term Limit for Collapse	*Number of P-terms*	Increase default number if design does not fit. Changing number to 20-40 may help fit some designs.
Optimization	*ENABLED(Default), Disabled*	Default setting useful for most designs. Disable if you want design to fit exactly as logic equations specify.
Soft_buffer	*Enabled, DISABLED(Default)*	Default setting useful for most designs. Enable to prevent fitter from collapsing all or specific nodes such as, combinatorial nodes with multiple fanouts or multiple flip-flop product term control signals.
Soft Buffer Node Name(s)	*Node1, Node2...*	
Cascade Logic	*ENABLED(Default), Disabled,*	Default setting useful for most designs. Disable if you don't want cascade logic to be used at all, or for only critical path outputs.
Cascade Logic Pin Name(s)	*Pin1, Pin2...*	
XOR Synthesis	*Enabled* *DISABLED(Default)*	Default setting useful for most designs. Enable if you want logic to use the hardware XOR in the ATF1500's macrocell for either all or certain pins. Especially useful for logic that uses XOR gates such as comparators, arithmetic logic.
XOR Synthesis Pin Name(s)	*Pin1, Pin2...*	
Pin-Controlled Power Down	*Enabled,* *DISABLED(Default)*	Enable of you want to use the pin-controlled power-down feature on the ATF1500.

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