ATF1500AS Product Family Conversion

Introduction

The ATF1500AS Complex Programmable Logic Device (CPLD) Product family offers high-density and high-performance devices. Atmel currently offers the ATF1500A, ATF1502AS, ATF1504AS and the ATF1508AS CPLDs. The ATF1500A is a 32 macrocell device and is offered in 44-pin PLCC/TQFP package. The ATF1502AS is a 32 macrocell ISP device and will be offered in 44-pin PLCC/TQFP package. The ATF1504AS is a 64 macrocell ISP device and is offered in 44-pin TQFP/PLCC, 68-pin PLCC, 84-pin PLCC and 100-pin TQFP/PQFP pack-ages. The ATF1508AS is a 128 macrocell ISP device and is offered in 84-pin PLCC, 100-pin TQFP/PQFP, 160-pin PQFP packages. This application note acts as a guide to use the Atmel POF2JED software utility. This utility converts a programming output file (.POF file) to the Atmel programming file (.JED) without any functionality or performance loss. It is available on the Atmel BBS and website.

BBS: 1-(408)-436-4309

Website: www.atmel.com

Target Devices

The following competitor devices can be converted over to their Atmel equivalents. The version of POF2JED software used is also listed. The information is subject to change as new devices are added. Contact Atmel PLD Applications or your local Atmel sales offices for the latest information.

PLD Hotline: (408) 436-4333

PLD e-mail: pld@atmel.com

Competitor	Atmel	POF2JED Version
7032	1500A	3.30
7032VLC44	1500ABV-J44	3.30
7032VTC44	1500ABV-A44	3.30
7032SLC44	1502AS-J44	(3.4x)[1]
7032STC44	1502AS-A44	(3.4x)[1]
7064LC44	1504AS-J44	3.30
7064TC44	1504AS-A44	3.30
7064LC68	1504AS-J68	3.30
7064LC84	1504AS-J84	3.30
7064QC100	1504AS-Q100	3.30
7064TC100	1504AS-A100	3.30
7064SLC44	1504AS-J44	3.30
7064STC44	1504AS-A44	3.30
7064SLC84	1504AS-J84	3.30
7064SQC100	1504AS-Q100	3.30
7064STC100	1504AS-A100	3.30
7128ELC84	1508AS-J84	3.30
7128LC84	1508AS-J84	3.30
7128EQC100	1508AS-Q100	3.30
7128QC100	1508AS-Q100	3.30
7128EQC160	1508AS-Q160	3.30
7128QC160	1508AS-Q160	3.30
7128SLC84	1508AS-J84	3.30
7128SQC100	1508AS-Q100	3.30
7128SQC160	1508AS-Q160	3.30
7128STC100	1508AS-A100	3.30

Note: 1. (3.4x) implies future releases.

How to Use POF2JED?

POF2JED utility is executed at the DOS prompt. The program does conversion automatically taking into account the proper device and package.

```
Command: POF2JED filename.POF
```

The output is a JEDEC (.JED) file that is used to program the Atmel CPLD. A report that shows the results of the conversion is also generated (.TXT file).

Note: A UNIX version is available. Please contact Atmel PLD Applications for more information.

To list command line options type:

POF2JED [device option]
Select one of the following device options:

-1500A
-1502AS
-1504AS
-1508AS

Standard Command Line Options

-i	Specify the input file name (.POF).
-o	Specify the output filename (.JED).
-device	Specify the target device (-1500, -1500A, -1502AS, -1504AS, -1508AS).
-PD1:	Enables the Power Down mode on pin PD1 for ATF1500AS family of devices (defaults to Disabled).
-PD2:	Enables the Power Down mode on pin PD2 for ATF1500AS family of devices (defaults to Disabled). Either PD1 or PD2 pins or both can be used to power down the part. This option can also be selected in the design source file. A logic high on these pins brings the device into the power down mode. Any time the pin is asserted, the device will switch into a standby power mode and ignore all inputs. All pin transitions are ignored until the PD pin is brought to a logic low. Note: The Translator may override this option setting if you enable this mode but the Design is using the PD pin for Design Logic.
-pinclk:	Uses pin clock wherever applicable. Global clock will be used for Product term Clock. This helps to improve performance of the design (defaults to Disabled).
-race_cover_off:	Turns off race coverage option (defaults to on). This conversion will be the same as implemented in the .POF output file. However, if turned on, it will detect any potential hazards and accordingly allocate additional resources available to correct the hazards. If the hazards cannot be corrected a warning will appear in the report file.
-secure:	Sets security bit on (defaults to off). A JEDEC file with the security bit will be generated. When this JEDEC file is programmed into the devices it will be secured. When the device is secured it cannot be read and will perform normally in the design.
-slew [fast|slow|auto]:	Sets slew rate for all outputs (7128/E: defaults to fast; 7032S/7064S/7128S: defaults to auto)
	fast	Sets output slew rate to fast. A faster slew rate provides high speed transitions and may introduce more noise transients.
	slow	Sets output slew rate to slow and thereby reduces system noise. However it does introduce a nominal delay
	auto	Follows settings from POF file. Depending on the device type the outputs would either be fast or slow.
-pin_keep:	Enables pin keeper circuits (defaults to Disabled). The pinkeeper circuits eliminate the need for external pull up resistors and eliminate their DC power consumption.

For example,

```
POF2JED filename.pof -secure -race_cover_off
```

This will secure the device and will not add race condition coverage when converting "filename.pof" to generate "filename.jed."

Advanced Command Line Options Applicable to ATF1500AS Family (1502AS/1504AS/1508AS)

-mc_power [on|off|auto]	Sets Reduced Power mode for all Macrocells (MCs)[2] (defaults to auto).	
	on	Turns on Reduced Power mode for all MCs.
	off	Turns off Reduced Power mode for all MCs.
	auto	Follows settings from POF file.
	When this feature is turned on, power consumption is reduced. All MCs draw approximately one-half the power in the reduced power mode compared to the standard power mode. *There is a speed penalty* when this option is enabled. Consult the device datasheet for details.	
-power_reset	Sets device power-up reset hysteresis. This feature allows the device to reset only when V_{CC} goes below 0.7V. This feature must be enabled if the power down mode is enabled (-PD1 and/or -PD2 option). (defaults to Disabled).	
-GCK0_ ITD	Enables ITD (Input Transition Detection circuitry) fuse on GCK0. (defaults to Disabled).	
-GCK1_ ITD	Enables ITD fuse on GCK1 (defaults to Disabled).	
-GCK2_ ITD	Enables ITD fuse on GCK2 (defaults to Disabled).	
	The ITD feature allows the user to save power by controlling whether the device will wake up on each clock edge even if no inputs are transitioning. When the feature is disabled, the devices will not wake up on each transition of the selected pin clock input. When enabled the pin clock transition will wake up the part.	
	Note: The POF2JED will automatically enable/disable this feature depending on the type of design that is being converted. If any of the GCK[0:2] pin goes to the Universal Interconnect Matrix, the ITD circuitry is enabled, overriding the default setting. This only applies to "L/Z" devices.	
-open_out [on|off|auto]	Sets all MC output types. (7064/7128/E: defaults to off; 7032S/7064S /7128S: defaults to auto).	
	on	Sets Open Collector mode. Here the outputs are of open collector type for each I/O pin. This enables the device to provide control signals that can be asserted by one of several inputs.
	off	Sets to Normal mode
	auto	Follows settings from .POF file.
-JTAG [on|off|auto]	Sets JTAG Mode. (7064/7128/E: defaults to off; 7032S/7064S 7128S: defaults to auto). When this option is turned on, the four JTAG port pins are disabled for use as I/O pins. When a JEDEC file with the JTAG bit "on" is programmed into an Atmel ISP device, the JTAG port will automatically be enabled.	
	Note: TheATF1500AS family of devices are shipped to customers in the erased state thereby enabling the JTAG port by default.	
	on	Enables JTAG mode.
	off	Disables JTAG mode. The JTAG pins are available as user I/O pins.
	auto	Follows settings from .POF file.
-TDI_PULLUP	Enables pull-up (10 KΩ) on TDI pin (7032S/7064S /7128S only). (defaults to Disabled).[1]	
-TMS_PULLUP	Enables pull-up (10 KΩ) on TMS pin (7032S/7064S /7128S only). (defaults to Disabled).[1]	

Notes: 1.   JTAG bit is enabled automatically.
           2.   MC stands for Macrocell.

A screen snapshot of a conversion will look as follows:

```
Atmel POF2JED Version 3.30 March 30, 1998
Copyright 1997 Atmel Corporation.  All Rights Reserved

7128E PLCC84 --> 1508 PLCC84

Input file                          :boolean.pof
Output file                         :boolean.jed
Conversion Report File              :boolean.txt

POF2JED processed 2 seconds
Conversion is complete!
```

Enhanced Architecture Conversion Issues Specific to ATF1500AS Family (1502AS/1504AS/1508AS)

How to reduce power consumption?

- In order to reduce power consumption, use "L/Z" devices.
- Disable the ITD on the Global Clock pins (GCK[0:2]. If any of the GCK[0:2] pin goes to the Universal Interconnect Matrix, the ITD circuitry is enabled. The ITD feature allows the user to save power by controlling whether the device will wake up on each clock edge even if no inputs are transitioning. When the feature is disabled, the devices will not wake up on each transition of the selected pin clock input thus conserving power.
- Turn on when applicable the reduced power option (mc_power). This will put all Macrocells into the reduced power mode. Note: There is a speed penalty when using this option.
- Enable Pin-Keeper circuits (-pin_keep).
- Set Slew option to slow and thereby reduce dynamic I_{CC} (-slew slow).
- Ensure that in "L/Z" designs there is a large decoupling capacitor. The "L/Z" device requires a large transient current from V_{CC} when waking-up the device from standby to active mode. This transient current can be supplied by using decoupling capacitors. A 0.22 µF capacitor is recommended for typical applications. You may also refer to the applications note, "Selecting Decoupling Capacitors for Atmel PLD's", available on our Website.

Pin Keeper Issues

- All members of the ATF1500AS Product family have active Pin Keeper circuits. Ensure that I/O or input pull-up/pulldown resistors do not contend with Pin Keeper circuits. Pin Keeper circuits have a 40 µA drive. These circuits ensure that a signal holds its previous state after the pin has been tristated.
- Problems can occur when you have 100 KΩ pullup or 30 KΩ pulldown resistors on the I/O pins. These resistors will contend with the pin keeper circuits. If a design uses pull-up on the inputs or outputs of an ATF1508AS, a 10 KΩ is recommended. For pulldown, a 5K resistor is recommended.
- POF2JED automatically disables Pin-Keeper circuits for ATF1500AS family of devices (by default).

JTAG Conversion Issues

When converting from a 7128S or any 7000 series part with JTAG capability, the POF2JED will automatically enable JTAG In-System Programming (ISP) mode of the Atmel ISP device. Refer to the .txt file generated by the POF2JED converter to determine if the JTAG port is enabled. If it is enabled, then the device can be re-programmed through ISP. Otherwise you will need to manually enable it by setting the JTAG ON option in the POF2JED converter. The translator will check if the design is using the JTAG port pins. If it is, an error will be generated and the Atmel ISP device can still be programmed once in the ISP mode. However, it will have to be re-programmed on an external programmer.

The Atmel ISP device also has an optional feature to enable the pull ups for the JTAG pins TDI and TMS (-TMS_pullup and -TDI_pullup). If these internal pullups are enabled, then no external pullups are needed for these JTAG pins.

Power ON Reset Issues

Use the **Power_Reset** feature if you are unsure about power regulation on circuit board or if the VCC/GND pins are very noisy.

In addition, when you use one of the powerdown pins (PD1 or PD2) to power down the part, the **Power_Reset** option must be turned On. This puts the device in Dual point Reset mode and ensures that the device is not reset unless the V_{CC} drops below 0.7V.

ATF1500AS

ATMEL

®

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe
Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686-677
FAX (44) 1276-686-697

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Fax-on-Demand
North America:
1-(800) 292-8635

International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

Printed on recycled paper.

0916B–04/99/xM