Designing for In-System Programmability with Atmel CPLDs

Introduction

This application note describes design methods and requirements for implementing In-System Programmability (ISP) with Atmel CPLD devices. ISP is implemented in Atmel devices through the Atmel JTAG ISP interface. The Atmel JTAG ISP interface allows you to program Atmel devices after they are mounted on your circuit Board. ISP eliminates the extra handling step required in the manufacturing process to program the device on a external programmer before placing them on your circuit board. Eliminating this step reduces greatly the possibility for damaging the delicate leads of high-pin count surface mount devices and allows you to make design changes and easy field upgrades without removing the Atmel device from the circuit board.

Atmel JTAG ISP Interface

The Atmel JTAG ISP interface is a 4-pin 5 volt interface compatible with the Joint-Test-Action Group (JTAG) standard. (IEEE Std. 1149.1a-1993) All Atmel devices are programmed, verified and erased through this interface. The JTAG interface is a serial interface consisting of the TCK, TMS, TDI and TDO pins, and a JTAG Test-Access-Port (TAP) Controller. The TCK pin is the serial data clock. Programming data is clocked by this pin. The TDI pin is the serial data input. It is used to shift programming data into the Atmel device. The TDO pin is the serial data output. It is used to shift out fuse data from the Atmel device. The TMS pin is a mode select pin. It controls the state of the JTAG TAP controller.

A JEDEC file is necessary to program any Atmel ISP device. Atmel provides a translater to convert output files from a competitor's programming format to a JEDEC file compatible with the Atmel ISP family of devices. After you have created JEDEC file(s) for each Atmel ISP device, you are ready to program them on your circuit board. Using the Atmel ISP software and download cable you can program, verify and erase any Atmel ISP device directly from your personal computer .

Note: Atmel ships all ISP devices in a bulk-erased state which enables the JTAG interface by default. Therefore, all Atmel devices are initially shipped ISP-ready and are ready to be programmed with the Atmel ISP software.

Atmel ISP devices are fully JTAG compatible and support the required Boundary-Scan Test (BST) operations specified in the JTAG standard. Atmel ISP devices can be configured to be a part of a JTAG BST chain with other JTAG devices for in-circuit testing of your system boards. With this feature you can test Atmel CPLDs along with other devices without resorting to bed-of-nails testing. The Atmel JTAG ISP interface is compatible with most Automated Test Equipment hardware on the market today.

For more information about BST or the JEDEC translator, contact Atmel PLD Applications at: **(408)436-4333**
or email us at: **pld@atmel.com**.
You can also reach us by contacting our website at: **www.atmel.com**

ATF1508AS ISP Family

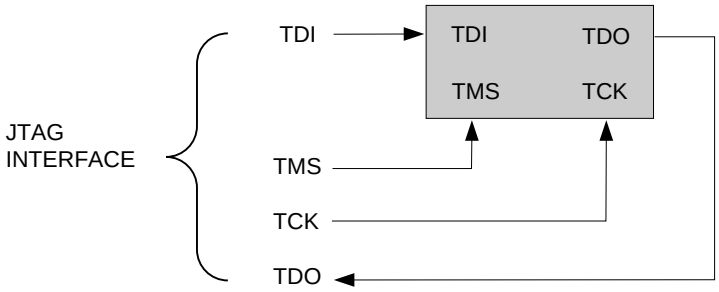
Application Note

0924A-A–9/97

Single Device Programming

The Atmel JTAG ISP interface can be configured to program a single Atmel ISP device. The JTAG configuration for a single device is shown in Figure 1. When the Atmel ISP device is configured in this way a register is present between between the TDI and TDO pins of the device. The size of this register depends on the JTAG instruction, and the data being shifted in for that instruction. The JTAG Interface pins for the Atmel ISP device must be connected to 10-pin header on your circuit board. This header mates with the Atmel ISP cable and allows the Atmel ISP software to transfer programming data from your personal computer to the Atmel ISP device. A pinout of the header is shown in Figure 4. The pinout for the JTAG pins for different Atmel ISP devices is listed in Table 2.

Figure 1. Single Device JTAG Configuration

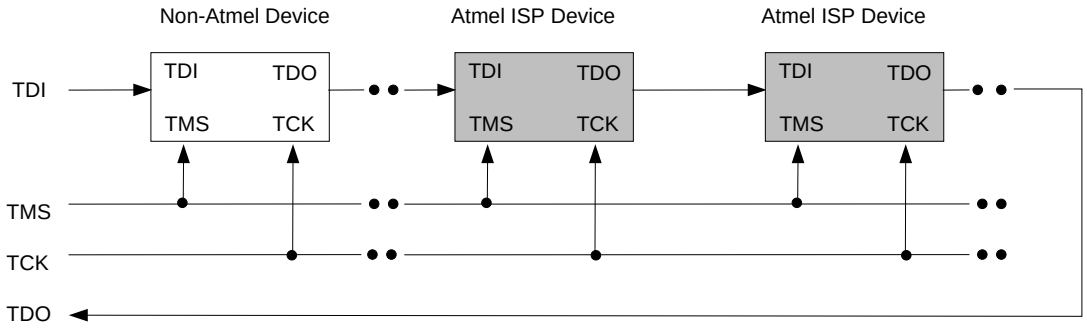


Note: You will need to reserve space on your circuit board to accomodate a 10-pin male header for the JTAG interface. The pinout for this header must match the Atmel ISP connecter pinout. The JTAG interface pins for each Atmel device must also be connected to this header.

Multiple Device Programming

Atmel ISP devices can be configured as part of a JTAG daisy chain. Once the daisy chain is configured multiple Atmel ISP devices can be programmed at the same time (Parallel ISP). Figure 2 shows the configuration for Multiple device programming.

Figure 2. Multiple Device Configuration - JTAG Chain



TDI, TMS, TCK and TDO comprise the JTAG interface. The ISP software allows you to create a JTAG daisy chain for multiple devices, including non-Atmel devices, and implement Parallel ISP for Atmel devices.

To create a JTAG daisy chain to implement Parallel ISP perform the following steps:

- Connect the the TMS and TCK pin for each device in the JTAG chain to the appropriate pins on the 10-pin header on your circuit board.

- Connect the TDI pin from the first device to the TDI pin on the 10-pin header.
- Connect the TDO pin from first device to the TDI pin for the next device. Continue this process untill all except the last one are connected.
- Connect the TDO pin from the last device to the TDO pin on the 10-pin header.

A device residing in any location in the JTAG chain can be programmed exclusive of all others. You can use the Atmel ISP software to place all other devices except the one to be programmed in the JTAG BYPASS mode. When the other devices are placed in this mode, a 1-bit flow-through register appears between the TDI and TDO pins for these devices. During a programming operation JTAG programming data passes through devices in the JTAG BYPASS mode. This allows only the device you want to program to be loaded with JEDEC fuse data. If you need more information about this feature contact Atmel PLD Applications.

Programming Considerations

While an Atmel ISP device is being programmed on your target system, the state of the outputs depend on whether the pin-keeper circuits on the device are enabled. Pin-keepers circuits are weak latches that hold input and outputs of the Atmel ISP device to their previous logic state. The logic state will be held after an output is disabled, or when a device input is externally tri-stated. Pin-keepers circuits can be enabled or disabled by specifying Atmel device fitter properties. See **Design Considerations** below for details.

Note: If you plan to use pin-keepers in your design make sure that no inputs or outputs on the Atmel ISP device are pulled-up by a 100KΩ resistor, or pulled-down by a 20KΩ resistor. If pull-up and/or pull-down resistors are necessary, then we recommend using 5 - 10KΩ resistors.

If you are re-programming the Atmel ISP device and pin-keeper circuits were enabled, then the device will hold all its outputs to their previous state while the new pattern is being re-programmed into the device. If the pin-keeper circuits have previously been disabled, then all outputs on the device will be tri-stated during re-programming.

Note: Blank devices initially shipped by Atmel with the pin-keeper circuits disabled. This means when you program an ISP device for the **first** time, all outputs will be tri-stated during programming.

If you need more information about the JTAG BYPASS mode or the device state during programming, contact Atmel PLD Applications.

Design Considerations

Performing ISP for Atmel ISP devices requires that you reserve design resources for the JTAG interface. You will need to reserve four I/O pins for the TMS, TDI, TDO and TCK pins. The pin number for these pins depend on which Atmel ISP device you are using and its package type. Refer to Table 1 for pinout information. The JTAG standard also requires that the TMS and TDI pins be pulled up externally for each device in the JTAG chain. *Atmel ISP devices have an internal pull-up feature for these pins which, when enabled, saves the need for an external pull-up resistor*. Once you have reserved logic resources for the JTAG interface you can program, verify and erase any Atmel ISP device using the Atmel ISP software.

Note: Even though you must reserve certain I/O pins in your design for the JTAG interface, you can still implement buried logic functions in the macrocells associated with these pins.

Atmel ships all ISP devices in a bulk-erased state which enables the JTAG interface by default. Therefore, all Atmel devices are initially shipped ISP-ready and are ready to be programmed with the Atmel ISP software.

To use ISP to program Atmel Devices you must enable the JTAG interface. An optional but recommended practice is to also enable the TMS and TDI internal pullups. Enabling the JTAG interface requires choosing specific Atmel device types and enabling certain property settings on the Atmel device fitter before compiling your design. This procedure is outlined below for Synario and WinCUPL™. If you need to enable Atmel fitter properties for other software platforms, please contact Atmel PLD Applications.

JTAG Interface with Synario™

To enable the JTAG interface with Atmel-Synario and Multi-vendor Synario software from Data-I/O, you need to select an Atmel ISP device type first. You can change fitter property settings to enable the TDI and TMS internal pullups or the Pin-Keeper circuits.

If you use an Atmel ISP device type for a design the uses the JTAG interface pins, Atmel-Synario will generate an error.

- *Double*-Click on the **Device Icon** in the Sources section of the **Project Navigator**. The Choose Device Dialog Box will open
- Click *once* on **Atmel PLDs**. Click on the Down arrow to scroll through the device list.
- Click *once* to select the appropriate Atmel ISP device type for your design. Refer to Table 1 for a list of Atmel ISP device types to choose from.

Note: Multi-vendor Synario users must install the Atmel PLD Device Kit first, before they can can select Atmel PLD devices.

- Click **OK** to close the Choose Device Dialog Box. If the Confirm Change Dialog Box appears, click **Yes** to close it.
- In the Processes section of the **Project Navigator**, click *once* on **Fit Design**.
- Click on the **Properties** Icon.
- Scroll down through the Properties List. You can enable the TMS and TDI pullups by double clicking on the **JTAG TMS Pullup Option** and **JTAG TDI Pullup Options** properties respectively.

Note: Selecting an Atmel ISP device type automatically enables the JTAG ISP-Mode property. Selecting a non-ISP device type disables it.

- Close the **Properties..** dialog box
- *Double-click* to run the **Fit Design** Process. If the design fits, the fitter will generate a JEDEC file, which, when programmed into the device, will keep the JTAG interface enabled and (optionally) enable the internal TMS and TDI pullups and Pin-Keeper circuits.

JTAG Interface with WinCUPL

To enable the JTAG interface for Atmel-WinCUPL and CUPL Total-Designer™ software from Logical Devices, you need to select an Atmel ISP device type first. You can then change fitter property settings to enable the TDI and TMS internal pullups, or other options.

If you use an Atmel ISP device type for a design that uses the JTAG interface pins, WinCUPL will generate an error.

- Click *once* on **Options..** from the WinCUPL main menu**,** then click *once* on **Select Device**. This will open the Select Device Dialog Box.
- Choose the appropriate Atmel ISP device. Refer to Table 1 for a device type listing for Atmel-WinCUPL.

Note: An alternate method is to choose an appropriate Atmel ISP device type from Table 1 and include it the header section of your PLD source file.

- Click **OK** to close the Select Device Dialog Box.
- Click *once* on **File..** from the WinCUPL main menu**,** then click *once* on **Open**. Select your PLD source file from the appropriate working directory.
- Click **OK** to open the PLD souce file
- (*Optional)* Add the following statements before the equations section in your CUPL PLD source file

```
  Property Atmel {TDI_pullup = ON};
/* Optional,Enables TDI pullup */
  Property Atmel {TMS_pullup = ON};
/* Optional,Enables TMS pullup */
Property Atmel {Pin_Keep = ON};
/* Optional,Enables Pin = Keeper circuits */
```

Note: Selecting and Atmel ISP device type will automatically enable the JTAG interface by default when Atmel-WinCUPL runs the Atmel device fitter.

- Click *once* on **File** from the WinCUPL main menu, then click *once* on **Save**. This will save any change you made to the source file.
- Click *once* on **Run..** from the WinCUPL main menu**,** then Click *once* on **Device Specific Compile**.
- WinCUPL will compile the design and spawn the Atmel device fitter. If the design fits, a JEDEC file is automatically created. When the JEDEC file is programmed into the device, the JTAG interface and the internal TMS and TDI pullups will remain enabled.

If you have designs which prevent you from reserving resources for the JTAG interface, or you do not wish to use ISP, you must select an Atmel non-ISP Device type. See Table 1 for a listing. You can then re-program the device using an external device programmer.

Table 1 shows a list of Atmel ISP and non-ISP device type-for Synario and WinCUPL. This information is subject to change as new devices are added. Contact Atmel PLD Application for updated information.

Table 1. Atmel-Synario, Atmel WinCUPL ISP Device Types

Atmel Device	Synario ISP Device Type	Synario non-ISP Device Type	WinCUPL ISP Device Type	WinCUPL non-ISP Device Type
ATF1508AS 68-pin PLCC	ATF1508AS - ISP PLCC68	ATF1508AS PLCC68	F1508ISPPLCC68	F1508PLCC68
ATF1508AS 84-pin PLCC	ATF1508AS - ISP PLCC84	ATF1508AS PLCC84	F1508ISPPLCC84	F1508PLCC84
ATF1508AS 100-pin QFP	ATF1508AS - ISP PQFP100	ATF1508AS PQFP100	F1508ISPQFP100	F1508QFP100
ATF1508AS 100-pin VQFP	ATF1508AS - ISP VQFP100	ATF1508AS VQFP100	F1508ISPVQFP100	F1508VQFP100
ATF1508AS 160-pin QFP	ATF1508AS - ISP PQFP160	ATF1508AS PQFP160	F1508ISPQFP160	F1508QFP160

Atmel ISP Software

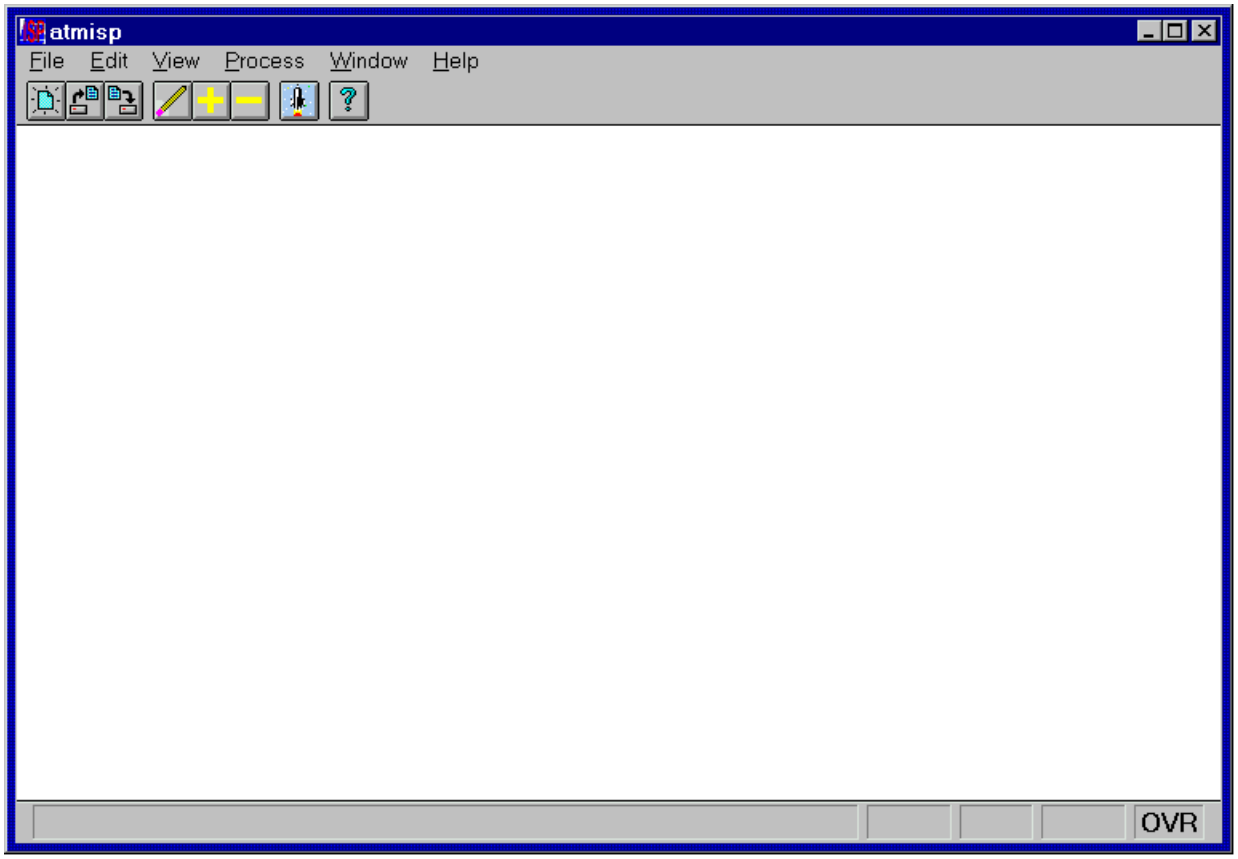
The Atmel ISP Software is the primary means for implementing ISP for Atmel devices. It can be used either from your personal computer to implement ISP or to generate a SVF output file (Serial Vector Format) for use with your ATE system. The ISP software is a windows driven program that runs on Win 3.x, Win95, and WinNT platforms. If you plan to use the Atmel ISP software to implement ISP from your personal computer you will need the Atmel ISP cable. Otherwise, it is not required.

The first step to using the software requires entering information about all the devices in your JTAG chain. For instance, where they reside in the chain, their JTAG instruction register lengths etc. All non-Atmel devices must be configured in the JTAG BYPASS mode. An Atmel device can be configured in the JTAG BYPASS mode if you do not wish to program it. After this information is entered, the software will prompt you to link the JEDEC files for each Atmel ISP device you want to program. You are now ready to program the devices. The ISP software will implement Parallel ISP if more than one Atmel device is be programmed. Figure 3 below shows the ISP software main menu.

Note: The Atmel ISP software will warn you if you attempt to program a design that uses the JTAG interface pins for logic functions.

More information on the Atmel ISP software is available by contacting Atmel PLD Applications. To order the Atmel ISP software refer to the Atmel ISP Software datasheet or contact your local Atmel Sales Representative.

Figure 3. Atmel ISP Software Main Menu



Atmel ISP Hardware

Atmel ISP hardware consists of the Atmel ISP Cable, the Atmel ISP Demo Board, Atmel PC Adapter and Atmel ISP Daughter Boards. The ISP cable is required to implement ISP from your personal computer for Atmel devices. The demo board is optional, but useful for prototyping your designs before using them in your target system. The Atmel ISP Daughter boards are used with Atmel Demo Board so you can program devices in different package types.

Note: To order any of the above hardware refer to the Atmel ISP Hardware datasheet or contact your local Atmel Sales Representative.

Atmel ISP Cable

Figure 4 shows the ISP cable and the location of pin 1. The Female header is not polarized. The 25-pin Male connector plugs into the parallel port of your personal computer. The 10-pin Female Header plugs into a 10-pin Male Header on your circuit board.

Figure 4. Atmel ISP Cable

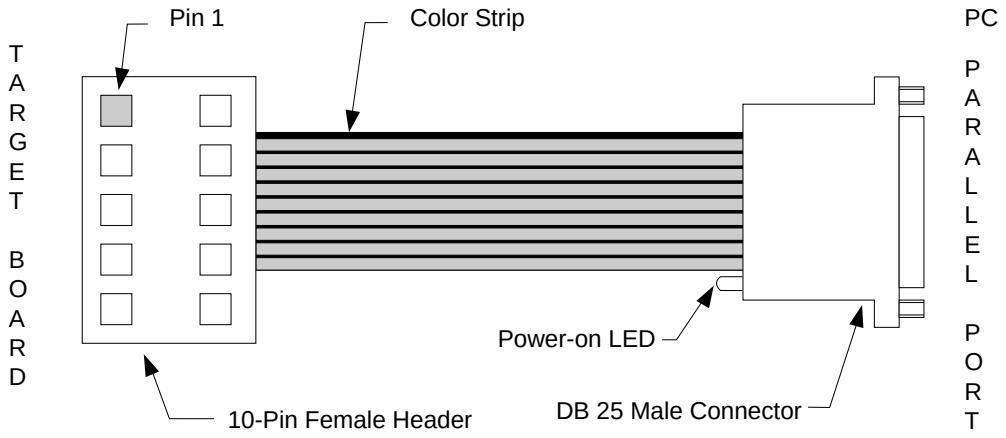


Figure 5 shows the pinout for the 10-pin Female header on the Atmel ISP cable. The pinout on the 10-pin Male Header on your circuit board *must* match this pinout.

Note: Your circuit board must supply VCC and GND to the 10-pin Male header on your circuit board.

Figure 6 shows the dimensions for the 10-pin male header that is mounted on your circuit board.

Figure 5. Atmel ISP Cable 10-pin Female Header Pinout

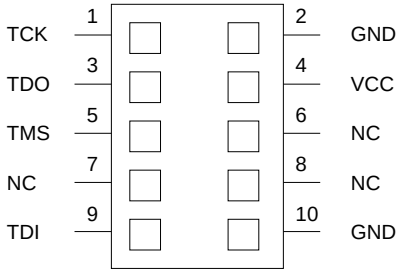
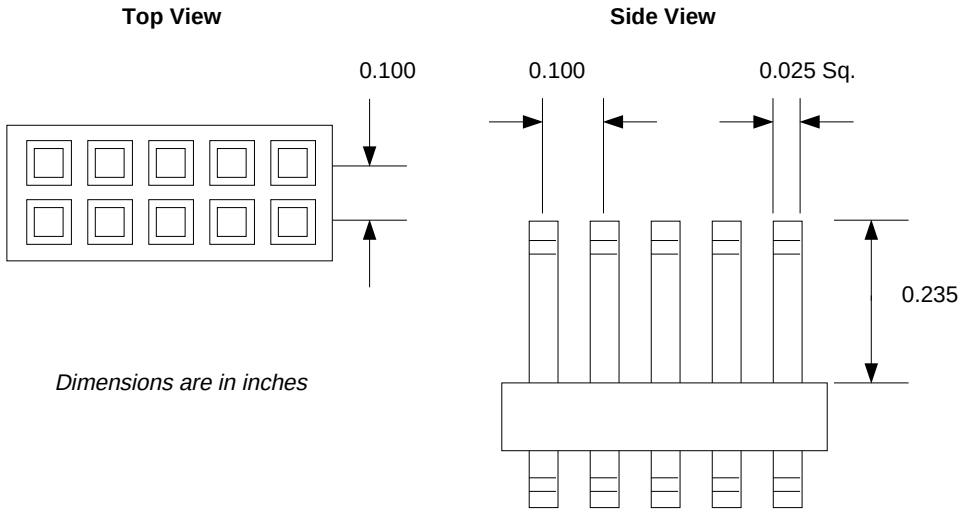


Figure 6. 10-pin Male Header Dimensions



Atmel ISP/Demo Board

Another method to implement ISP on Atmel devices is to use the Atmel ISP demo board. With the demo board you can program an Atmel ISP device in the demo board socket, remove it and insert it into your target system. The demo board requires a 9V AC/DC adapter for power.

The Demo Board connects to your personal computer in two ways. You can use a 25-pin Parallel port cable, or the Atmel ISP cable via the 10-pin male header on the Demo Board. There are two sockets that may be used for programming. One socket is a fixed 84-pin PLCC socket. The other socket can accomodate an adaptor board that can be used to program the other package types. Atmel supplies an adaptor board for each package type. The Demo Board has a prototying area, switches and LED's you can use to test additional logic not contained in the Atmel ISP device. Demo boards can be connected together via the 25-pin male connector from one board to the 25-pin female connector on the other board.

Note: Make sure to use the Atmel DC adapter to power the demo board.

For more information on the Atmel ISP Demo Board refer to the "Atmel ISP Demo Board" application note.

Atmel ISP Device Pinouts

Table 2 shows the JTAG pinout information for Atmel ISP devices currently available. This information is subject to change as new devices are added Contact the Atmel PLD Applications or contact the local Atmel sales representative for updated information

Table 2. Atmel ISP Device JTAG Pinout

	ATF1508AS Package Types				
JTAG Pin #	**68-pin PLCC**	**84-pin PLCC**	**100-pin PQFP**	**100-pin VQFP**	**160-pin PQFP**
TDI	12	14	6	4	9
TDO	57	71	75	73	112
TMS	19	23	17	15	22
TCK	50	62	64	62	99

Figure 7. Atmel ISP Demo Board