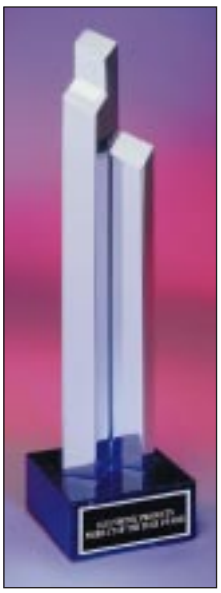
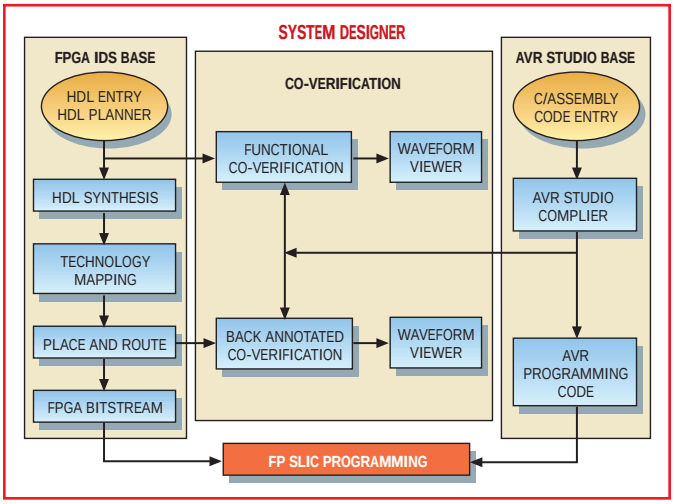
24th Annual Product of the Year Awards



From the thousands of products introduced in 1999, the editors of *Electronic Products* have chosen the most outstanding. The selections are based on significant advances in technology or its application, a decided innovation in design, or a substantial gain in price-performance. As usual, picking winners was made difficult by the many impressive products announced during the year. Here is a product by Atmel chosen as a 1999 award winner.

AT94Kxx field-programmable system-level ICs

FPGA/µP enables single-chip systems with co-verification of hardware and code



The AT94 microprocessor/FPGA allows code and logic development to proceed hand in hand.

The AT94Kxx family of field-programmable system-level ICs (FPSLICs) makes possible, for the first time, single-chip systems for small projects that don't justify the investment of an ASIC. At launch, the devices were backed by a complete EDA tool suite that includes co-verification of the processor icode and the FPGA HDL description.

The devices include the company's AVR 8-bit processor core (see *Electronic Products*, May 1998, p. 104), along with up to 40,000 gates of the AT40K FPGA family. Other common microcontroller peripherals such as UART, SPI, timer/counters, and a hardware multiplier are also integrated along with 32 Kbytes of program SRAM.

The family also features a facility for partial reconfiguration of the FPGA while the system is running. Several configurations could be stored in ROM, and substituted as necessary. For example, a cell-phone could change from WCDMA to GSM as it moved from one country to another.

System Designer, the tool suite for the family, includes co-verification of the FPGA hardware and the AVR code from the beginning (see *diagram*). The suite includes an instruction-set simulator for the AVR and a HDL FPGA design simulator that work together before any actual hardware is involved.

The System Designer EDA toolset supports co-verification of firmware and HDL, allowing a design to be completely tested in simulation before any silicon prototype is needed. A C-like macro language can be used to supply the debug environment with system macros for host file I/O simulation, reset, startup, shutdown, loops, if statements, and return statements. Interrupt simulation can launch specific interrupts periodically or at a specific cycle count.

The software allows what-if comparisons of different hardware/software partitions, predicting the performance and power consumption of each possibility. More than 50 pushbutton macro generators produce hard or soft parameterizable cores for the FPGA section. The user can specify a multiplier (for example, as "8 x 8" or "12 x 2") and need not know any HDL.

System Designer runs on Windows 95/98/NT. The AT94K FPSLIC family has three members, with 40,000, 20,000, and 10,000 FPGA gates. (AT94, from $19.90 ea/20,000—samples available now; System Designer annual subscription, $495—available now.)

Atmel, San Jose, CA
Hotline 800-29-ATMEL
literature@atmel.com