Date: November 5, 1999

ATMEL-CUPL/WinCUPL Bug List -- PLD Applications

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The following is a list of bugs which have been fixed in the ATMEL-CUPL 4.7a and earlier releases. WINCUPL V4.7b bugs to be be fixed are also included. If you notice any bugs not included in this list please contact Atmel PLD Applications.

Note: All bug files are located in the /Regress Subdirectory catagorized by package type.

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Bug #1
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ATV2500B bug:
Symtoms: simulation failed.

Work-around: Use the State diagram equations in the .PLD file.

5-1-95: Bug fixed with CUPL.DL (Atmel-CUPL 4.5c)
CUPL.DL 343,583 04-28-95 11:26a
== (See Bug #5)

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Bug #2
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ATV2500B Bug:

Symptoms: Cupl general incorrect equations using the Clock enable (.ce) product term even though JEDEC file only use .CK suffix. Equations are generated incorrect in .DOC file with compiling source file with state machine syntax.

Work-around: None

10-5-95 This bug is fixed on ATMEL-CUPL V4.5c

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Bug #3
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4-11-95
F18V8Z problem: Cannot set pin 18 to I/O mode.

To check this bug, compile with -f option and check fuse for pin 18. They should be XX.

4-11-95: This bug is fixed with Atmel-CUPL version 4.5c

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Bug #4
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ATV2500B bug:
Symtoms: CE simulation failed. The .CE equations and

configurations are generated properly (JEDEC fuse OK) but CSIM failed. JEDSIM would pass with the vectors (JEDEC vectors have to be modified because CSIM overrides with the simulation vectors).

Work-around: Do not simulate.

7-22-95 This bug is fixed with Atmel-CUPL version 4.5c.

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Bug #5

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ATF1500 Bug: (6-23-95)

Symtoms: CUPL assign node numbers to PLA file to undefined pinnodes in design when it should allow the fitter to assign them.

Workaround: Use the PINNODE instead of the NODE statement. NODE statement will eventually be removed from CUPL.

7-19-95 This bug is fixed in V4.5c of ATMEL CUPL.

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Bug #6

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(7-11-95)
Symtoms: CUPL produces incorrect PLA file for equation:
         out = !(!a & !b). PLA equation is out = !a & !b.
         when it should be: out = a # b.

Workaround: Write the equation as !out = !a # !b.
It will reduce correctly on the PLA file.

10-5-95 Fixed ATMEL-CUPL V4.5c

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Bug #7

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ATV2500 Bug

Symtoms: CUPL generates incorrect values of S1 and S5 bits for macrocell configured for a combinatorial output, and two Buried registed nodes Q1 and Q2. PT's for Q1 are inadvertantly combined with the output logic PT's.

Workaround: None at present. Needs CUPLC fix.

9-15-95 FIXED ATMEL CUPL V4.5c

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Bug #8

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ATV750B Bug: (8-29-95)

Symtoms: When more resources are used than available in the part CUPL gives no errors and compiles file. Same file on ATV750 generates "Output Mutually Excluded <   > (output name(s)" Error and terminates. Which is the correct response

Workaround: None

9-15-95 Fixed. ATMEL CUPL V4.5c

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Bug #9
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MCUPL Bug: (9-5-95)

Symtoms: MCUPL device menu doesn't include 'G22V10 and f1500 and
f1500t device types in listing.

Workaround: None.

9-15-95 Fixed. ATMEL CUPL V4.5c

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Bug #10
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ATV2500B Bug: (9-19-95)

Symtoms: Configuration bit S5 set incorrectly to "1" instead
of "0" for Combinatorial output, Buried Q1 node, Buried
Combinatorial node.

Workaround: None

9-27-95 Fixed ATMEL CUPL V4.5c

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Bug #15
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ATV2500B Bug: (10-10-95)

Symptoms: When using $REPEAT statement with State Machine Syntax
and % (modulus operator) CUPL generates incorrect equations.
Correct equations are generated for the ATV2500 device, however.

11-2-95 Fixed ATMEL CUPL V4.5c

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*********Bugs above this line have been fixed (11-2-95)********
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Bug #11
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ATF1500 Bug: (6-14-95)
Symtoms: This is general bug with applies to all devices since
simulation for CUPL's virtual device simulator. This bug
is a problem with the simulator reading the .ABS file which
generates incorrect result for registered outputs.
The same test vectors when run on programmer will pass.

Workaround: None at present
Fixed Atmel-CUPL V4.7a

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Bug #12
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ATF1500 Bug:
Symtoms: CUPL produces simulation error when there are no pin
or node assignments in the PLD file. VSIM should be able
to simulate the equations without assignments. This bug
is specific for F1500.

Workaround: Assign pin and node assignments to all pins and
nodes in source file.
Fixed Atmel-CUPL V4.7a

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Bug #13
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ATV750/B and ATV2500/B Bug: (9-5-95)

Symtoms: Buried latch representation of combinatorial output
feature available in the device not supported by CUPL.
.DFB extension compiles okay in V4.4c, generates error on V4.5b.
Device feature should be supported by using .DFB suffix option.

Workaround: For up to 4 PT's use PINNODE with same logic as
combinatorial output.
Fixed Atmel-CUPL V4.7a

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Bug #14
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ATV750B Bug: (9-19-95)

Symtoms: Using "De-morganize" option in CUPL result in equation
that are mapped in CUPLC as being inverted. (i.e S2 bit is set
incorrectly)

Workaround: Don't use the options, or try minimization option
instead to reduce product term count.
Or write logic directly in De-morganized form.
De-morganize option only works with virtual devices.

1-3-96 Fixed CUPL V4.6a. Contact PLD Application for more
information
Fixed Atmel-CUPL V4.7a

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Bug #16
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ATV2500B Bug: (10-11-95)

Symptoms: When macrocell configured as a combinatorial output plus
a Q2 registered node using T type flip-flops, S5 bit is bieng set
to a "0" instead using D type flips-flops instead of a "1".

Workaround: None
1-19-96 Fixed Atmel-CUPL V4.7a

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Bug #17
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WSIM Bug: (1-2-96)

Symptoms: WSIM will not open a *.si or *.abs file. Gives
"Invalid Libary Access Key" error. For Atmel-CUPL 4.5b.

Workaround: None
Fixed Atmel-CUPL V4.7a

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Bug # 18
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ATV2500B Bug: (1-9-96)

Symptoms: CUPL comfigures Q2 registered node as T flip-flops when using the NODE keyword. When PINNODE keyword and node number is used these nodes are configured correctly as D flip-flops.

Workaround: Define all nodes used in the design with the PINNODE keyword and node number. Do not use the NODE keyword.

2-21-96 Fixed Atmel-CUPL V4.7a

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*** Bugs above this line fixed on Atmel-CUPL V4.7a*************
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Bug # 19
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ATF1500 Bug: (2-21-96)
Atmel-CUPL V4.7a
Symptoms: CSIM generates errors with simulating an ATF1500 design with no pin or node number assigned in the source (.pld) file.

Workaround: Assign pin and node number for the design in the source file

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Bug # 20
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MCUPL Bug: 6-21-96
Symptom: Cannot access the examples directory in MCUPL for Atmel-CUPL V4.7a.

Workaround: Copy the MCUPL.CFG file from the Atmel BBS into you CUPL executables directory. If you directory path is different than the default path you need the modify the wdpath setting in this file.

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Bug # 21
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MCUPL Bug: 7-26-96
Atmel-CUPL V4.7a
Symptom: No p22v10 information in <Device Information> section Atmel-CUPL V4.7a

Workaround: Download new devhelp.txt from Atmel BBS an copy to your CUPL executables directory

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Bug # 22
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MCUPL Bug: 8-26-96
Atmel-CUPL V4.7a
Symptom: MCUPL running under Win95, ezedit with not display under the MCUPL <Edit Design File> section.

Workaround: Run CUPL for the DOS prompt. Use the DOS editor, or any other editor to modify the input file. Make sure path to ezedit is specified in MCUPL.CFG file.

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Bug # 23
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MCUPL,CUPL Bug: 8-28-96
Atmel-CUPL V4.7a
Symptom: Using g16v8 or g20v8 device type in Atmel-CUPL V4.7a give CUPLB error "g16v8s or g20v8s" not is library. Autoselect is selecting the wrong device type.

Workaround: Select the g16v8a or g20v8a device type.

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Bug # 24
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Examples: 11-6-96
Atmel-CUPL V4.7a

Symptom: The gates.pld example has an error on the nand equation. equation written as nand = !(!a & !b) instead of !(a & b). File fails simulation.

Workaround: Fix the PLD source file and re-simulate. Updated Atmel-CUPL ZIP file dated 11-6-96 is on BBS.

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Bug # 25
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ATV2500B Bug: 11-1-96
Atmel-CUPL V4.7a
Symptom: CUPL configures macrocell S0-S3 bits to illegal (1000) configurations for I/O pins used as an input with Q1 and Q2 buried registered nodes.

Workaround: None

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Bugs above this line fixed with Atmel-WINCUPL V4.7b******
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Bug # 26
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VSIMA Bug: 8-29-96, ATF1500
Atmel-CUPL V4.7a,WINCUPL V4.7b
Symptom: Logic with a registered output used a clock to another register (i.e. ripple counter logic) does not simulute correctly. Register clock output is ignored by VSIM.

Workaround: Use a PINNODE to buffer output that clocks second register. Define clock equation for second register to equal buffered output.

```
For example:
Original Equation                    New Equation
reg2.ck = reg1;                      PINNODE = temp;
reg1 is a registered output          temp = reg1;
                                     reg2.ck = temp;

*****************************************************************
Bug # 27
*****************************************************************
WINCUPL V4.7b Bug: 12-2-96
Symptom: WINCUPL is not able to open some large text files for viewing.
Reports "File to Read" error.

Workaround: Open the DOS Prompt in WINCUPL and use the DOS editor to
view the file.

*****************************************************************
Bug # 28
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WCSIM Bug: 12-2-96
WINCUPL V4.7b

Symptom: WINCUPL generates a General Protection Fault when trying to run
WCSIM of a file that failed simulation.

Workaround: None

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Bug # 29
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CSIM Bug: 12-6-96
WINCUPL V4.7b

Symptom: Designs using gated sychronous clock option on ATV2500B fail
to simulate.

Workaround: Gated synchronous clock need to be defined using .CK instead
of .CE term. Define .CK product term to be Pin1 & <clock equation>. If you
do not intend to simulate your design this workaround is not necessary.

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Bug # 30
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CUPL Bug:  12-20-96
WINCUPL V4.7b

Symptom: CUPL is compiling equations such as:
D0.AR = RST # ![X0..X1]; incorrectly. Is reduced to D0.AR = RST # !X0;
extra term is being dropped.

Workaround: Defined equation as D0.AR = rst # !x0 & !x1; It will compile
correctly.

*****************************************************************
Bug # 31
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WINCUPL Bug: 2-3-96
ATV2500B Bug
CUPLC.DLL/CUPLC.exe

Symptom: For a I/O pin using an input, > 4PT Q1 nodes and < 4PT Q2
```

node CUPL is reporting "excessive number of product terms" when implementing the logic into the macrocell. Logic should fit if registered mode is selected.

Workaround: None

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Bug # 32

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FIT1500 Bug: 6-16-97 (FIT1500 V2.32)

Symtom: Fitter failed to fit design.
Problem:

```
EQ = (1);     becomes
EQ = A # !A;  after Espresso.
```

Logically, both equations are valid. But the second equation will use 2 product terms.. which may cause the fitter failed to fit the design

Workaround:

Run FIT1500 from the DOS command:

```
FIT1500 filename.TT2
```

E.g.

```
FIT1500 test.TT2
```

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Bug # 33

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WINCUPL Bug: 6-23-97
ATV2500B Bug
CUPLC.DLL/CUPLC.EXE

Symptom: For a I/O pin used as an input, and pinnode equations for both Q1 and Q2 nodes CUPL defaults to configuring the macrocell as combinatorial with two 4PT registered nodes.
Configuring the macrocell as registered with an 8PT Q1 and 4PT Q2 node is a more efficient configuration, since it allows and extra 4 PT's to be allocated to the Q1 node.

Workaround: As an example, define equations as follows:

INSTEAD OF THIS:

```
Pin <number> = INPUT_VARIABLE;

Pinnode <number> = Q1_node;
Pinnode <number> = Q2_node;

INPUT_VARIABLE.oe = 'b'0;

Q1_node = <Logic Expression> ;
Q2_node = <Logic Expression> ;

out1 = Q1_node # Q2_node;
out2 = Q2_node & INPUT_VARIABLE;
```

DO THIS:

```
Pin <number> = INPUT_VARIABLE;
```

```
Pinnode <number> = Q2_node;

INPUT_VARIABLE.oe = 'b'0;

INPUT_VARIABLE.d = <Q1_node Logic expression> ; /* Q1 node logic equation */
Q2_node = <Logic Expression> ;

out1 = INPUT_VARIABLE # Q2_node;
out2 = Q2_node & INPUT_VARIABLE.IO; /* Input Pin feedback */

This will configure the macrocell correctly.

*****************************************************************
Bug # 34
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WINCUPL (V4.8a) Bug: 11-05-97

Symptom: Download the WinCUPL ZIP file from BBS or website and install
directly from the harddisk overwrites the readme.txt file with one of
zero size.

Workaround: Unzip WinCUPL ZIP files. Unzip disk1,disk2.zip on 1.44MB
floppy disks and install.

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Bug # 35
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WINCUPL (V4.8a) Bug: 11-05-97
CSIMA Bug:

Symptom: Select the "display results" options under "Simulator Options"
to view a successful simulation as a waveform generates an error,
"Could not find program wcsim"

Workaround: Make sure the WINCUPL executables directory in the DOS path
specified in the AUTOEXEC.bat file on your PC.

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Bug # 36
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WINCUPL (4.8a) Bug: 12-24-97
FIND1500/FIND1508 Bug:

Symptom: WinCUPL generates "Fatal Fitter Error During Processing" when compiling
1500 and/or 1508 file.

Workaround: This error can occur if the fitter in unable to fit your design.
First check to see if you have a <filename>.fit file in your project directory.
Read it (if it exists) to find out why the design didn't fit. If this file doesn't
exist then you can manually run the fitter. Follow the steps below to do
this:

Copy fitter executable in the same directory as the project
sub-directory. Re-Compile the design.

OR

1) Open the  COMPILE OPTIONS.. submenu under the OUTPUT FILE menu.
2) Select PLA file, De-select JEDEC file output
3) Re-compile design in the Main menu
   The fitter will generate an output file with the (<filename>.tt2) extension.
```

4) Open the DOS Prompt in the UTILITIES menu.
5) Copy the (*.tt2) into the WinCUPL executables directory
6) Type fit1500 <filename[.tt2]> Press <return>

OR fit1508 <filename[.tt2]> Press <return> If attempting to use the 1508.

7) The fitter will attempt to fit your design. All the output files generated by the fitter will reside in the WinCUPL executables directory.

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Bug # 37

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WINCUPL (4.8a) Bug: 12-29-97
FIND1500 Bug:

Symptom: WinCUPL unable to open DOS PROMPT to spawn ATF1500 fitter. Either automatically or from the DOS PROMPT select in the UTILITIES menu for WINNT 4.0 system. Works okay in Win95 and WinNT3.x

Workaround: Use Win95 or WinNT3.x.

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Bug # 38

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WinCUPL (4.8a) Bug: 2-18-98
CUPLX Bug:

Symptom: Using the Register_Select(output_name) = 2 Keyword to convert an RS or JK-type FF to T-type flip flop generates the wrong equations.

For example:

output_name.s = Set;
output_name.r = Reset
output_name.ck = clock;

Compiled equations for T-type FF (DOC file) are:

output_name.t = !output_name & Set;

Reset term missing from equation. Should be:

output_name.t = Set & !output_name # Reset & output_name;

Workaround: Define the T-type logic manually.

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Bug # 39

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WinCUPL (4.8a) Bug: 2-20-98
CUPLX Bug:

Symptom: Using the Register_Select(output_name) = 1 Keyword to convert an synchronous RS equations to D-type flip flop results in incorrect equations. Converting JK equations to D works however.

Workaround: Use JK equations instead. This behaviour should be functionally equivalent to the synchronous RS equations.

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Bug # 40

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WinCUPL (4.8a) Bug: 2-23-98
CSIM Bug:

Symptom: For ATF1500AS family of device CUPL simulator does not simulate
active low output correctly. Reports the same results as active high output
Works OK on ATV family of devices.

For example,

pin !a; pin b; pin !c;

b = a; c = a;

Simulation:

Order !a, b, !c;
Vector:
0 L L
1 H H

Instead of:

Vector:
0 L H
1 H L

Workaround: specify c to be active high: pin = c; c = !a,

Simulation:

Order !a,b,c; Same vectors as before. This should report the correct simulation results.

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Bug # 41
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WinCUPL (4.8a) Bug: 9-18-98
CSIM Bug:

Cupl Simulator ignores vector values if there are errors in the order statement such
as a missing ',' on one of the signals. Could report a correct simulation when the
vectors are incorrect.

Workaround: Check syntax of Simulation Input file, make sure it's correct. Use example
files for referenence and the correct syntax.

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Bug # 42
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WinCUPL (4.8a) Bug: 5-19-99

Cannot print from within the WINCUPL program.

Workaround:
Copy th file into another Editor such as Notepad and then Print

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Bug # 43
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WinCUPL (4.8a) Simulator Bug: 7/28/99

Adding .io extension to ORDER statement for a Field Variable in *.SI file even through supported on *.PLD file cause GPF fault when attempting to run simulator. This bug could be generalized to any output extension available in CUPL.

For example,

```
        Order:Rset,!Ale,Aux,!Rd,!Wd,%2,DatBus.io,
        %2,AdrLat,%2,InpBuf,%2,OutLat;
```

Creates GPF fault.

Workaround:

```
        Order:Rset,!Ale,Aux,!Rd,!Wd,%2,DatBus,
        %2,AdrLat,%2,InpBuf,%2,OutLat;
```

Is OKAY. Where DatBus, AdrLat, InpBuf, OutLat are FIELD variable specified in the *.pld source file.

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Bug #44

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WinCUPL (V4.8a) Simulator Bug: 7/29/99

When running the simulator with an old *.so file open. WinCUPL should prompt the user to overwrite it after a new simulation is completed. This will prevent the user from having to re-open the file after every simulation to view the updated results.

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Bug #45

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Wincupl5.126 Compiler/FInd1500 Bug: 8/31/99

When trying to load a file from A:\, specifically targetting the 1500a device, the file compiles OK and then the find1500 window opens and comes up with a message:
[007xl] could not change to specified directory. could notopen PDS file for copying.
Seems like the find1500 program is unable to find the fit1500 program ?

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Bug #46

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Wincupl5.126 Install Bug on network drive: 8/31/99

I installed this on the F:\common (network drive);
After Installing : I clicked on Finish and then the System hangsup;
I could open WINCUPL program, however it was missing several device type.

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Bug #47

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Wincupl5.126

The file fails to compile for f1508isptqfp100 device type. problem is with a valid I/O pin number 45 not being recognized as a valid I/O.

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Bug #48

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Wincupl5.126

After starting WinCUPL, following message is shown on screen:
Runtime error 5.Invalid procedure call or argument.

Similar problem occurs on WINNT4.0 This happens with European version of WINDOWS
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Bug #49
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EDITOR Bugs/Features Desired in WINCUPL:-
- In the Editor the command, CUT.COPY does not work (CtrlC, CtrlX) (?)
  Paste from Windows Clipboard is OK, Cut into clipboard fails, Delete is OK
- Search.replace.all does ONE only, Search.replace.OK does ALL. (backwards)
- Search.replace suffers recursion fail, with effective lockout,
  if Result String is Superset of Find String
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Bug #50
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SIMULATOR [WINSIM] :-
a) generates messages :-
"[0033sa] Please note: jedec vectors cannot be created with undefined
pin numbers.in0" when auto-run from within CUPL, but does appear to actually
append the JED vectors (!)

b) General edit, often causes Runtime rrror 5 error/terminate WinSim.

c) BUS display does not seem to be correct, Help example shows expected
HEX, run does not.
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Bug #51
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The project navigator does not update the Files list if a given .PLD file is
recompiled by choosing a different device type

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