

CL-SH8665

Preliminary Product Bulletin

FEATURES

Microcontroller

ARM7TDMI 32-bit RISC processor

- High-performance RISC core ideal for integration into disk drive electronics solutions
- Excellent MIPS/die size and MIPS/watt with high code density and an open architecture

DSP-assist logic

- Rounding, scaling, and saturation operation in hardware

Internal memory

- 4 Kbytes of instruction/data SRAM
- 16 Kbytes of instruction ROM (mask-programmable)

External memory

 — 512 Kbytes of addressable memory with up to two programmable chip selects for flash/ROM/SRAM

Peripherals

- Interrupt controller
- Timers
- UART
- General-purpose I/O
 JTAG boundary scan

(cont.)

Integrated ATA Drive Electronics

OVERVIEW

The CL-SH8665 is a high-performance, low-cost, integrated microcontroller, ATA disk controller, and read channel. The CL-SH8665, flash memory, EDO DRAM buffer memory, preamplifier, and power drivers comprise a complete drive electronics solution for ATA disk drives.

The ARM7TDMI 32-bit RISC processor core delivers high performance in a small core size with low power consumption. Combining the ARM core with the DSP-assist logic provides enough bandwidth to

(cont.)





FEATURES (cont.)

ATA Disk Controller (CL-SH7656)

- Ultra DMA support (33.3 Mbytes/sec.)
- Direct buffer access by CPU
- Buffer bandwidth
 - 64 Mbytes/sec. with EDO DRAM and 40-MHz SYSCLK
- 8-bit NRZ disk data rate 260 Mbits/sec. maximum
- Advanced ECC capabilities

Read Channel

- User data rate from 47 to 245 Mbits/sec.
- Digitally controlled VGA (variable gain amplifier)
- Ten-tap adaptive digital FIR (finite impulse response) equalization filter

- Fourth-order analog LPF (low-pass filter)
- 6-bit flash ADC (analog-to-digital converter)
- Rate 16/17 d=0 RLL encoder/decoder
- Enhanced PR4 partial response sequence detector
- Thermal asperity detection and correction capability for MR heads

General

- Customer-defined control logic
- On-chip oscillator and frequency synthesizer
- Power management
 - Three system power modes (Run, Idle, and Sleep), plus clock disabling of idle subsystems
- 3.3-volt, 0.35-micron design

OVERVIEW (cont.)

manage servo and spindle control, as well as disk controller and other drive functions.

The Thumb[™] technology from ARM[™] allows 16-bit instructions to be executed within the 32-bit processor core, reducing the firmware code size with no penalty in performance. For critical functions, such as servo processing or interrupt handling, 32-bit instructions can be employed. A high-speed 16-bit external bus is used for instruction fetch from flash memory. Data memory can be accessed through the internal SRAM or by using a portion of the buffer memory with direct processor access through the disk controller.

The hard disk controller logic (CL-SH7656 core) offers full hardware support of the ID-less architecture, including automatic sector pulse generation, logical sector mapping and on-track defect management. Buffer bandwidth using EDO DRAM of up to 64 Mbytes/sec. can sustain host data rates of 33.3 Mbytes/sec. in Ultra DMA mode 2 and disk data rates up to 260 Mbits/sec. (for the controller). The advanced ECC logic provides five-byte error correction and can correct a single-burst error of 113 bits or a double-burst error of 49 bits on-the-fly. In addition, higher ECC correction and erasure pointer support.

The read channel logic (CL-SH3360 core) is a sampled amplitude digital read/write channel that provides a highly flexible, state-of-the-art, synchronous read path for high-density magnetic disk drives. In addition, this block has a programmable architecture and calibration feature that allows the channel parameters to be tuned to characteristics of each drive, head, and zone. High disk data rates — up to 245 Mbits/sec. (for the channel) — and erasure pointers are supported.

As shown in the system block diagram on page 1, the CL-SH8665, external flash memory, external buffer memory, a preamplifier, and the power drivers comprise the bulk of the drive electronics required for an ATA disk drive.

An on-chip oscillator and frequency synthesizer provide all clock frequencies required by the processor, peripheral, and disk controller subsystems. Sophisticated power management can be configured for three system power modes, plus automatic clock disabling of idle subsystems delivers maximum power savings.

The CL-SH8665 is designed in a 3.3-volt, 0.35micron process with 5-volt-tolerant I/Os. The device is available in a 208-pin package.





BUFFER MEMORY









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