CLEAR LOGIC

CL81500A

Laser-Configured ASIC Family

Key Features

- Laser-Configured ASIC (LASIC™) technology offers the ultimate combination of performance, flexibility, and low cost
- Functionally, architecturally, and electrically compatible with industry-standard FLEX® 8000A™ series FPGAs
- High Density
  - 16,000 Usable gates
  - 1,500 Flip-flops
  - 298 Maximum user I/O pins
- Laser fuse technology provides very fast, dense interconnect routing
- Optional Instant-On configuration eliminates the need for an external configuration EPROM
- Fabricated using 0.5 micron CMOS process
- Very low current consumption (active and standby)
- 3.3 volt or 5.0 volt operation
- Alpha particle immune

CL8000 Product Family Overview

Parameter	CL8282A CL8282AV	CL8452A	CL8636A	CL8820A	CL81188A	CL81500A
Available Gates	5,000	8,000	12,000	16,000	24,000	32,000
Useable Gates	2,500	4,000	6,000	8,000	12,000	16,000
Flip-flops	282	452	636	820	1,188	1,500
Logic Elements	208	336	504	672	1,008	1,296
Max user I/O pins	78	120	136	152	184	298
Packages	84 pin PLCC 100 pin TQFP	84 pin PLCC 100 pin TQFP 160 pin PQFP	84 pin PLCC 160 pin PQFP 208 pin PQFP	144 pin TQFP 160 pin PQFP 208 pin PQFP 225 pin BGA	208 pin PQFP 240 pin PQFP	240 pin PQFP 304 pin PQFP

Description

The Clear Logic CL8000 Laser-Configured ASIC (LASIC™) family offers the ultimate combination of performance, flexibility, and cost. This family is a system level second source to Altera Flex® 8000™ products. For designs not requiring in-system reprogrammability, design verification can be performed using the programmable Altera devices, and Clear Logic LASICs can be used for low cost, high volume production.

Clear Logic's innovative laser ASIC technology eliminates NRE costs, test vector development, ordering minimums and long lead times. No re-simulation or re-layout is required, as the device is engineered using a cell-based, PLD-like architecture. Clear Logic's TestCell™ technology ensures complete test coverage through the use of specialized testing modes which are transparent to the user.

The Clear Logic CL8000 Laser-Configured ASIC family is based upon a large array of logic elements. Each logic element contains a configurable look up table for combinatorial functions and a register for sequential operations. A group of eight logic elements forms a block. Laser-configured metal fuses implement logical functions and control signal routing

Laser configuration provides reduced cost and enhanced performance. These inherent performance benefits include extremely consistent propagation delays, reduced power consumption, and improved immunity to noise and upset events.

Configuration

Clear Logic's CL8000 LASIC family is compatible with all six configuration modes defined for the Flex 8000 product family. These configuration modes include the following:

- Active Serial
- Active Parallel Up
- Active Parallel Down
- Passive Parallel Synchronous
- Passive Parallel Asynchronous
- Passive Serial

The CL8000 is already configured when it is shipped, and can be configured to bypass the FLEX 8000 configuration modes.

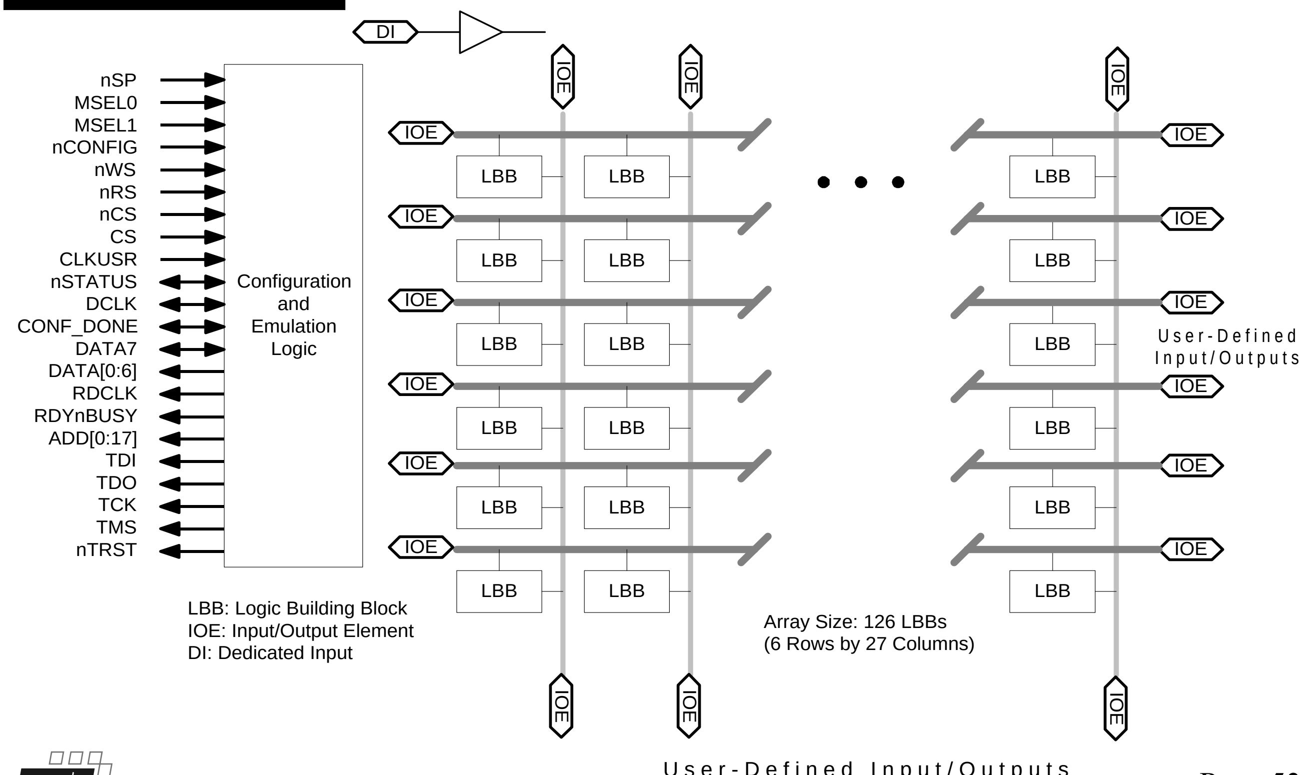
This "Instant-On" configuration mode eliminates the need for external EPROMs or microcode. In the Instant-On mode, the CL8000 device begins Initialization immediately upon a low-to-high transition on the nCONFIG pin.

Additional Information

For further information on designing with the CL8000 LASIC family, please consult the following documents:

- *CL8K01: CL8000 Packaging Guide*. This document provides specifications and drawings for packages used by the CL8000 family.
- *CL8K02: CL8000 and System Configuration*. This document contains a detailed discussion of all aspects of configuring CL8000-based systems.
- *CL8K03: CL8000 Technology White Paper*. This document outlines the technologies employed by the CL8000 LASIC family.
- *CL8K04: Requesting a CL8000 First Article*. This document provides instructions on how to submit a bitstream file for generation of first articles.
- *CL8K05: Calculating CL8000 Power Consumption*. This document provides guidelines for calculating power consumption based on design characteristics.

Block Diagram



Pin Configuration

Pin Name	240 pin PQFP	304 pin PQFP
nSP	237	304
MSEL0	19	26
MSEL1	38	51
nSTATUS	142	178
nCONFIG	120	152
DCLK	183	230
CONF_DONE	161	204
nWS	134	167
nRS	138	171
RDCLK	159	202
nCS	167	212
CS	170	215
RDYnBUSY	147	183
CLKUSR	156	199
ADD17	56	73
ADD16	54	71
ADD15	52	69
ADD14	45	60
ADD13	43	58
ADD12	41	56
ADD11	34	47
ADD10	32	45
ADD9	30	43
ADD8	27	34
ADD7	25	32
ADD6	23	30
ADD5	16	20
ADD4	14	18
ADD3	12	16
ADD2	5	8
ADD1	3	6
ADD0	1	4
DATA7	199	254
DATA6	197	252
DATA5	196	250
DATA4	194	248
DATA3	193	246
DATA2	190	243
DATA1	189	241
DATA0	187	239
TDI	63	80
TDO	117	149
TCLK	116	148
TMS	64	81
nTRST	115	145
Dedicated Inputs	8, 49, 131, 172	12, 64, 164, 217
VCCINT	18, 40, 60, 62, 91, 114, 129, 151, 173, 209, 236	24, 54, 77, 144, 79, 115, 162, 191, 218, 266, 301
VCCIO	17, 39, 61, 78, 94, 108, 130, 152, 174, 191, 205, 221, 235	22, 53, 78, 99, 119, 137, 163, 193, 220, 244, 262, 282, 300
GND	6, 7, 28, 29, 50, 51, 71, 85, 92, 101, 118, 119, 140, 141, 162, 163, 184, 185, 186, 198, 208, 214, 228	9, 11, 36, 38, 65, 67, 90, 108, 116, 128, 150, 151, 175, 177, 206, 208, 231, 232, 237, 253, 265, 273, 291
NC (No Connect)	-	10, 21, 23, 25, 35, 37, 39, 40, 41, 42, 52, 55, 66, 68, 146, 147, 161, 173, 174, 176, 187, 188, 189, 190, 192, 194, 195, 205, 207, 219, 221, 233, 234, 235, 236, 302, 303
Total user I/O pins	177	204

DC Electrical Specifications

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		-2.0	7.0	V
V_I	DC input voltage[1]		-2.0	7.0	V
I_{OUT}	DC output current, per pin		-25	25	mA
T_{STG}	Storage temperature	No bias	-65	150	°C
T_{AMB}	Ambient temperature	Under bias	-65	135	°C
T_J	Junction temperature	Under bias		135	°C

Recommended Operating Conditions[2]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage, internal logic and input buffers Commercial Grade Devices Industrial Grade Devices		 4.75 4.50	 5.25 5.50	V
V_{CCIO}	DC input voltage 5.0 volt commercial 5.0 volt industrial 3.3 volt operation		 4.75 4.50 3.00	 5.25 5.50 3.60	V
V_I	Input voltage		0	V_{CCINT}	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Operating temperature Commercial temperature range Industrial temperature range		 0 -40	 70 85	°C
t_R	Input signal rise time			40	ns
t_F	Input signal fall time			40	ns
t_{RVCC}	V_{CC} rise time			100	ms

DC Electrical Characteristics (over the operating range)

Symbol	Parameter	Conditions	Min	Typ[3]	Max	Unit
V_{IH}	Input HIGH Voltage		2.0		$V_{CCINT} + 0.3$	V
V_{IL}	Input LOW Voltage		-0.3		0.8	V
V_{OH}	Output HIGH Voltage	$I_{OH} = -4.0$ mA, $V_{CCIO} = V_{CCIO[Min]}$	2.4			V
V_{OL}	Output LOW Voltage	$I_{OL} = 12.0$ mA, $V_{CCIO} = V_{CCIO[Min]}$			0.45	V
I_{IN}	Input Leakage Current	$V_I = V_{CC}$ or GND	-10		10	μA
I_{OZ}	Output Leakage Current	$V_I = V_{CC}$ or GND	-40		40	μA
I_{CC0}	Standby Current	V_I = GND, no load		0.5	10	mA

Capacitance[4]

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

AC Electrical Specifications

I/O Element Timing Parameters[5]

Symbol	Parameter	Conditions	speed: -2 Min	speed: -2 Max	speed: -3 Min	speed: -3 Max	speed: -4 Min	speed: -4 Max	Unit
t_{IOD}	IOE register data delay			0.7		0.8		0.9	ns
t_{IOC}	IOE register control signal delay			1.7		1.8		1.9	ns
t_{IOE}	Output enable delay			1.7		1.8		1.9	ns
t_{IOCO}	IOE register clock to output delay			1.0		1.0		1.0	ns
t_{IOCOMB}	IOE combinatorial delay			0.3		0.2		0.1	ns
t_{IOSU}	IOE register setup time before clock		1.4		1.6		1.8		ns
t_{IOH}	IOE register hold time after clock		0.0		0.0		0.0		ns
t_{IOCLR}	IOE register clear delay			1.2		1.2		1.2	ns
t_{IN}	Input pad and buffer delay			1.5		1.6		1.7	ns
t_{OD1}	Output buffer and pad delay	slow slew rate = off, V_{CCIO} = 5.0v, C_L = 35 pF		1.1		1.4		1.7	ns
t_{OD2}	Output buffer and pad delay	slow slew rate = off, V_{CCIO} = 3.3v, C_L = 35 pF		1.6		1.9		2.2	ns
t_{OD3}	Output buffer and pad delay	slow slew rate = on, C_L = 35 pF, V_{CCIO} = 3.3v or 5.0v		4.6		4.9		5.2	ns
t_{ZX}	Output buffer disable delay	C_L = 5 pF		1.4		1.6		1.8	ns
t_{ZX1}	Output buffer disable delay	slow slew rate = off, V_{CCIO} = 5.0v, C_L = 35 pF		1.4		1.6		1.8	ns
t_{ZX2}	Output buffer disable delay	slow slew rate = off, V_{CCIO} = 3.3v, C_L = 35 pF		1.9		2.1		2.3	ns
t_{ZX3}	Output buffer disable delay	slow slew rate = on, C_L = 35 pF, V_{CCIO} = 3.3v or 5.0v		4.9		5.1		5.3	ns

External Timing Parameters[4]

Symbol	Parameter	Conditions	speed: -2 Min	speed: -2 Max	speed: -3 Min	speed: -3 Max	speed: -4 Min	speed: -4 Max	Unit
t_{DRR}	Register to register delay via four LEs, three row interconnects, and four local interconnects			16		20		25	ns
t_{ODH}	Output data hold time after clock		1.0		1.0		1.0		ns

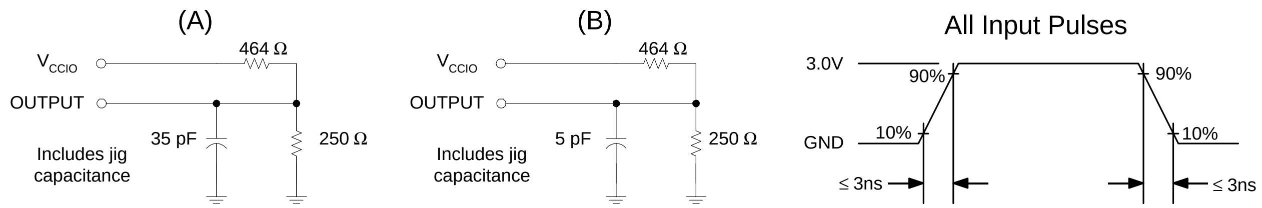
Logic Element Timing Parameters[5]

Symbol	Parameter	Conditions	speed: -2 Min	speed: -2 Max	speed: -3 Min	speed: -3 Max	speed: -4 Min	speed: -4 Max	Unit
t_{LUT}	Look up table delay for data-in			2.0		2.5		3.2	ns
t_{CLUT}	Look up table delay for carry-in			0.0		0.0		0.0	ns
t_{RLUT}	Look up table delay for LE register feedback			0.9		1.1		1.5	ns
t_{GATE}	Cascade gate delay			0.0		0.0		0.0	ns
t_{CASC}	Cascade chain routing delay			0.6		0.7		0.9	ns
t_{CICO}	Carry-in to carry-out delay			0.4		0.5		0.6	ns
t_{CGEN}	Data-in to carry-out delay			0.4		0.5		0.7	ns
t_{CGENR}	LE register feedback to carry-out delay			0.9		1.1		1.5	ns
t_C	LE register control signal delay			1.6		2.0		2.5	ns
t_{CH}	Clock high time		1.7		1.7		2.7		ns
t_{CL}	Clock low time		1.7		1.7		2.7		ns
t_{CO}	LE register clock-to-output delay			0.4		0.5		0.6	ns
t_{COMB}	Combinatorial delay			0.4		0.5		0.6	ns
t_{SU}	LE register setup time before clock		0.8		1.1		1.2		ns
t_H	LE register hold time after clock		0.9		1.1		1.5		ns
t_{PRE}	LE register preset delay			0.6		0.7		0.8	ns
t_{CLR}	LE register clear delay			0.6		0.7		0.8	ns

Interconnect Timing Parameters[5]

Symbol	Parameter	Conditions	speed: -2 Min	speed: -2 Max	speed: -3 Min	speed: -3 Max	speed: -4 Min	speed: -4 Max	Unit
$t_{LABCASC}$	Cascade delay between LEs in different LABs			0.3		0.3		0.4	ns
$t_{LABCARRY}$	Carry delay between LEs in different LABs			0.3		0.3		0.4	ns
t_{LOCAL}	LAB local interconnect delay			0.5		0.6		0.8	ns
t_{ROW}	Row interconnect routing delay			6.2		6.2		6.2	ns
t_{COL}	Column interconnect routing delay			3.0		3.0		3.0	ns
t_{DIN_C}	Dedicated input to LE control delay			5.0		5.0		5.5	ns
t_{DIN_D}	Dedicated input to LE data delay			8.2		8.2		8.7	ns
t_{DIN_IO}	Dedicated input to IOE control delay			5.0		5.0		5.5	ns

AC Test Conditions



Notes to Tables

1. During transitions, inputs may undershoot to -2.0v for periods shorter than 20ns. Otherwise, minimum DC input voltage is 0.3v.

2. The following devices do not have V_{CCIO} pins: CL8282A, CL8452A. For these devices, all references to V_{CCIO} should be changed to V_{CCINT}

3. Typical values are at V_{CC} of 5.0 volts and ambient temperature of 25 °C.

4. Guaranteed but not tested. Characterized initially, and after any design changes which may affect these parameters.

5. Internal timing delays are based on characterization, and cannot be explicitly tested. Internal timing parameters should be used for performance estimation only.

Ordering Information

Part Number	Temperature Range	Package Type	Speed	Altera Equivalent
CL81500AQC240-4	Commercial	240-pin Plastic QFP	-4 (slowest)	EPF81500AQC240-4
CL81500AQC240-3			-3	EPF81500AQC240-3
CL81500AQC240-2			-2 (fastest)	EPF81500AQC240-2
CL81500AQC304-4		304-pin Plastic QFP	-4 (slowest)	EPF81500AQC304-4
CL81500AQC304-3			-3	EPF81500AQC304-3
CL81500AQC304-2			-2 (fastest)	EPF81500AQC304-2
CL81500AQI240-3	Industrial	208-pin Plastic QFP	-3	EPF81500AQI240-3