



CL8282AV

Laser-Configured ASIC Family

Key Features

- ◆ Laser-Configured ASIC (LASIC™) technology offers the ultimate combination of performance, flexibility, and low cost
- ◆ Functionally, architecturally, and electrically compatible with industry-standard FLEX® 8000A™ series FPGAs
- ◆ High Density
 - 2,500 Usable gates
 - 282 Flip-flops
 - 78 Maximum user I/O pins
- ◆ Laser fuse technology provides very fast, dense interconnect routing
- ◆ Optional Instant-On configuration eliminates the need for an external configuration EPROM
- ◆ Fabricated using 0.5 micron CMOS process
- ◆ Available in five volt version (CL8282A)
- ◆ Very low current consumption (active and standby)
- ◆ Alpha particle immune

CL8000 Product Family Overview

Parameter	CL8282A CL8282AV	CL8452A	CL8636A	CL8820A	CL81188A	CL81500A
Available Gates	5,000	8,000	12,000	16,000	24,000	32,000
Useable Gates	2,500	4,000	6,000	8,000	12,000	16,000
Flip-flops	282	452	636	820	1,188	1,500
Logic Elements	208	336	504	672	1,008	1,296
Max user I/O pins	78	120	136	152	184	298
Packages	84 pin PLCC 100 pin TQFP	84 pin PLCC 100 pin TQFP 160 pin PQFP	84 pin PLCC 160 pin PQFP 208 pin PQFP	144 pin TQFP 160 pin PQFP 208 pin PQFP 225 pin BGA	208 pin PQFP 240 pin PQFP	240 pin PQFP 304 pin PQFP

Description

The Clear Logic CL8000 Laser-Configured ASIC (LASIC™) family offers the ultimate combination of performance, flexibility, and cost. This family is a system level second source to Altera Flex® 8000™ products. For designs not requiring in-system reprogrammability, design verification can be performed using the programmable Altera devices, and Clear Logic LASICs can be used for low cost, high volume production.

Clear Logic's innovative laser ASIC technology eliminates NRE costs, test vector development, ordering minimums and long lead times. No re-simulation or re-layout is required, as the device is engineered using a cell-based, PLD-like architecture. Clear Logic's TestCell™ technology ensures complete test coverage through the use of specialized testing modes which are transparent to the user.

The Clear Logic CL8000 Laser-Configured ASIC family is based upon a large array of logic elements. Each logic element contains a configurable look up table for combinatorial functions and a register for sequential operations. A group of eight logic elements forms a block. Laser-configured metal fuses implement logical functions and control signal routing

Laser configuration provides reduced cost and enhanced performance. These inherent performance benefits include extremely consistent propagation delays, reduced power consumption, and improved immunity to noise and upset events.

Configuration

Clear Logic's CL8000 LASIC family is compatible with all six configuration modes defined for the Flex 8000 product family. These configuration modes include the following:

- ◆ Active Serial
- ◆ Active Parallel Up
- ◆ Active Parallel Down
- ◆ Passive Parallel Synchronous
- ◆ Passive Parallel Asynchronous
- ◆ Passive Serial

The CL8000 is already configured when it is shipped, and can be configured to bypass the FLEX 8000 configuration modes.



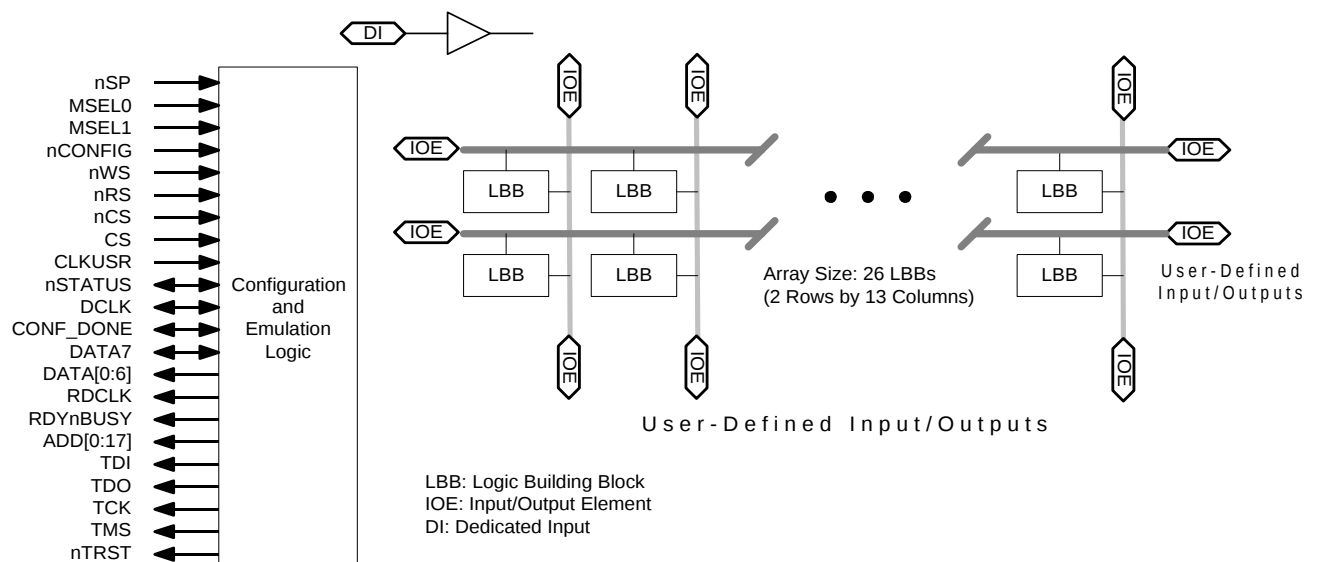
This “Instant-On” configuration mode eliminates the need for external EPROMs or microcode. In the Instant-On mode, the CL8000 device begins Initialization immediately upon a low-to-high transition on the nCONFIG pin.

Additional Information

For further information on designing with the CL8000 LASIC family, please refer to the following documents:

- ◆ *CL8K01: CL8000 Packaging Guide.* This document provides specifications and drawings for packages used by the CL8000 family.
- ◆ *CL8K02: CL8000 and System Configuration.* This document contains a detailed discussion of all aspects of configuring CL8000-based systems.
- ◆ *CL8K03: CL8000 Technology White Paper.* This document outlines the technologies employed by the CL8000 LASIC family.
- ◆ *CL8K04: Requesting a CL8000 First Article.* This document provides instructions on how to submit a bitstream file for generation of first articles.
- ◆ *CL8K05: Calculating CL8000 Power Consumption.* This document provides guidelines for calculating power consumption based on design characteristics.

Block Diagram



Pin Configuration

Pin Name	84 pin PLCC	100 pin TQFP
nSP	75	75
MSEL0	74	74
MSEL1	53	51
nSTATUS	32	24
nCONFIG	33	25
DCLK	10	100
CONF_DONE	11	1
nWS	30	22
nRS	48	42
RDCLK	49	45
nCS	29	21
CS	28	19
RDYnBUSY	77	77
CLKUSR	50	47
ADD17	51	49
ADD16	36	28
ADD15	56	55
ADD14	57	57
ADD13	58	58
ADD12	60	59
ADD11	61	60
ADD10	62	61
ADD9	63	62
ADD8	64	64
ADD7	65	65
ADD6	66	66
ADD5	67	67
ADD4	69	68
ADD3	70	69
ADD2	71	71
ADD1	76	76
ADD0	78	78
DATA7	3	90
DATA6	4	91
DATA5	6	92
DATA4	7	95
DATA3	8	97
DATA2	9	99
DATA1	13	4
DATA0	14	5
TDI	55	54
TDO	27	18
TCLK	72	72
TMS	20	11
nTRST	52	50
Dedicated Inputs	12, 31, 54, 73	3, 23, 53, 73
VCCINT	17, 38, 59, 80	6, 20, 37, 56, 70, 87
GND	5, 26, 47, 68	2, 13, 30, 44, 52, 63, 80, 94
NC (No Connect)	-	-
Total user I/O pins	64	74



DC Electrical Specifications

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		-2.0	7.0	V
V_I	DC input voltage ^[1]		-2.0	7.0	V
I_{OUT}	DC output current, per pin		-25	25	mA
T_{STG}	Storage temperature	No bias	-65	150	°C
T_{AMB}	Ambient temperature	Under bias	-65	135	°C
T_J	Junction temperature	Under bias		135	°C

Recommended Operating Conditions^[2]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage		3.0	3.6	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature		0	70	°C
t_R	Input signal rise time			40	ns
t_F	Input signal fall time			40	ns

DC Electrical Characteristics (over the operating range)

Symbol	Parameter	Conditions	Min	Typ ^[3]	Max	Unit
V_{IH}	Input HIGH Voltage		2.0		$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage		-0.3		0.8	V
V_{OH}	Output HIGH Voltage	$I_{OH} = 0.1 \text{ mA}$	$V_{CC} - 0.2$			V
V_{OL}	Output LOW Voltage	$I_{OL} = 4.0 \text{ mA}$			0.45	V
I_{IN}	Input Leakage Current	$V_I = V_{CC}$ or GND	-10		10	μA
I_{OZ}	Output Leakage Current	$V_I = V_{CC}$ or GND	-40		40	μA
I_{CC0}	Standby Current	$V_I = \text{GND}$, no load		0.3	10	mA



Capacitance^[4]

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0\text{ V}$, $f = 1.0\text{ MHz}$		10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{ V}$, $f = 1.0\text{ MHz}$		10	pF

AC Electrical Specifications**I/O Element Timing Parameters^[5]**

Symbol	Parameter	Conditions	speed: -2		speed: -3		speed: -4		Unit
			Min	Max	Min	Max	Min	Max	
t_{IOD}	IOE register data delay			0.7		0.8		2.2	ns
t_{IOC}	IOE register control signal delay			1.7		1.8		2.0	ns
t_{IOE}	Output enable delay			1.7		1.8		2.0	ns
t_{IOCO}	IOE register clock to output delay			1.0		1.0		2.0	ns
t_{IOCOMB}	IOE combinatorial delay			0.3		0.2		0.0	ns
t_{IOSU}	IOE register setup time before clock		1.4		1.6		2.8		ns
t_{IOH}	IOE register hold time after clock		0.0		0.0		0.2		ns
t_{IOCLR}	IOE register clear delay			1.2		1.2		2.3	ns
t_{IN}	Input pad and buffer delay			1.5		1.6		3.4	ns
t_{OD2}	Output buffer and pad delay	slow slew rate = off, $V_{CCIO} = 3.3\text{V}$, $C_L = 35\text{ pF}$		-		1.9		4.1	ns
t_{OD3}	Output buffer and pad delay	slow slew rate = on, $C_L = 35\text{ pF}$, $V_{CCIO} = 3.3\text{V}$		4.6		4.9		7.1	ns
t_{ZX}	Output buffer disable delay	$C_L = 5\text{ pF}$		1.4		1.6		4.3	ns
t_{ZX2}	Output buffer disable delay	slow slew rate = off, $V_{CCIO} = 3.3\text{V}$, $C_L = 35\text{ pF}$		-		2.1		4.3	ns
t_{ZX3}	Output buffer disable delay	slow slew rate = on, $C_L = 35\text{ pF}$, $V_{CCIO} = 3.3\text{V}$		4.9		5.1		8.3	ns

External Timing Parameters^[4]

Symbol	Parameter	Conditions	speed: -2		speed: -3		speed: -4		Unit
			Min	Max	Min	Max	Min	Max	
t_{DRR}	Register to register delay via four LEs, three row interconnects, and four local interconnects			16		20		50	ns
t_{ODH}	Output data hold time after clock		1.0		1.0		1.0		ns



Logic Element Timing Parameters^[5]

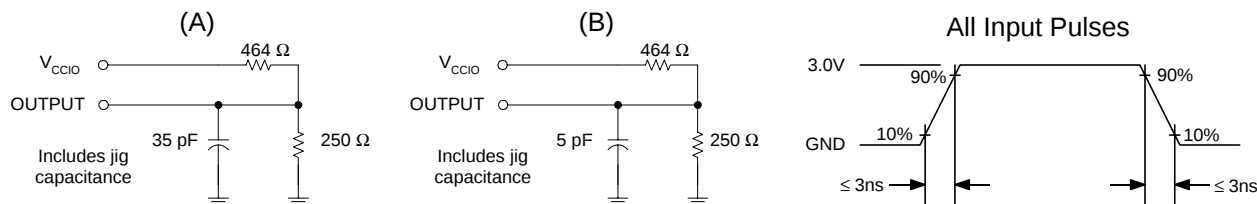
			speed: -2		speed: -3		speed: -4		Unit
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	
t_{LUT}	Look up table delay for data-in		2.0		2.5		7.3		ns
t_{CLUT}	Look up table delay for carry-in		0.0		0.0		1.4		ns
t_{RLUT}	Look up table delay for LE register feedback		0.9		1.1		5.1		ns
t_{GATE}	Cascade gate delay		0.0		0.0		0.0		ns
t_{CASC}	Cascade chain routing delay		0.6		0.7		2.8		ns
t_{CICO}	Carry-in to carry-out delay		0.4		0.5		1.5		ns
t_{CGEN}	Data-in to carry-out delay		0.4		0.5		2.2		ns
t_{CGENR}	LE register feedback to carry-out delay		0.9		1.1		3.7		ns
t_c	LE register control signal delay		1.6		2.0		4.7		ns
t_{CH}	Clock high time		1.7		1.7		6.0		ns
t_{CL}	Clock low time		1.7		1.7		6.0		ns
t_{CO}	LE register clock-to-output delay		0.4		0.5		0.9		ns
t_{COMB}	Combinatorial delay		0.4		0.5		0.9		ns
t_{SU}	LE register setup time before clock		0.8		1.1		2.4		ns
t_H	LE register hold time after clock		0.9		1.1		4.6		ns
t_{PRE}	LE register preset delay		0.6		0.7		1.3		ns
t_{CLR}	LE register clear delay		0.6		0.7		1.3		ns

Interconnect Timing Parameters^[5]

			speed: -2		speed: -3		speed: -4		Unit
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$	Cascade delay between LEs in different LABs		0.3		0.3		1.3		ns
$t_{LABCARRY}$	Carry delay between LEs in different LABs		0.3		0.3		0.8		ns
t_{LOCAL}	LAB local interconnect delay		0.5		0.6		1.5		ns
t_{ROW}	Row interconnect routing delay		4.2		4.2		6.3		ns
t_{COL}	Column interconnect routing delay		2.5		2.5		3.8		ns
t_{DIN_C}	Dedicated input to LE control delay		5.0		5.0		8.0		ns
t_{DIN_D}	Dedicated input to LE data delay		7.2		7.2		10.8		ns
t_{DIN_IO}	Dedicated input to IOE control delay		5.0		5.0		9.0		ns



AC Test Conditions



Notes to Tables

1. During transitions, inputs may undershoot to -2.0v for periods shorter than 20ns. Otherwise, minimum DC input voltage is 0.3v.
2. The following devices do not have V_{CCIO} pins: CL8282A, CL8452A. For these devices, all references to V_{CCIO} should be changed to V_{CCINT} .
3. Typical values are at V_{CC} of 3.3 volts and ambient temperature of 25 °C.
4. Guaranteed but not tested. Characterized initially, and after any design changes which may affect these parameters.
5. Internal timing delays are based on characterization, and cannot be explicitly tested. Internal timing parameters should be used for performance estimation only.

Ordering Information

Part Number	Temperature Range	Package Type	Speed	Altera Equivalent
CL8282AVLC84-4	Commercial	84-pin PLCC	-4 (slowest)	
CL8282AVLC84-3			-3	
CL8282AVLC84-2			-2 (fastest)	
CL8282AVTC100-4		100-pin Plastic TQFP	-4 (slowest)	EPF8282ATC100-4
CL8282AVTC100-3			-3	
CL8282AVTC100-2			-2 (fastest)	

