CLEAR LOGIC

# CL8636A

**Laser-Configured ASIC Family**

## Key Features

- Laser-Configured ASIC (LASIC™) technology offers the ultimate combination of performance, flexibility, and low cost
- Functionally, architecturally, and electrically compatible with industry-standard FLEX® 8000A™ series FPGAs
- High Density
  - 6,000 Usable gates
  - 636 Flip-flops
  - 136 Maximum user I/O pins
- Laser fuse technology provides very fast, dense interconnect routing
- Optional Instant-On configuration eliminates the need for an external configuration EPROM
- Fabricated using 0.5 micron CMOS process
- Very low current consumption (active and standby)
- 3.3 volt or 5.0 volt operation
- Alpha particle immune

### CL8000 Product Family Overview

| Parameter | CL8282A<br>CL8282AV | CL8452A | CL8636A | CL8820A | CL81188A | CL81500A |
|---|---|---|---|---|---|---|
| Available Gates | 5,000 | 8,000 | 12,000 | 16,000 | 24,000 | 32,000 |
| Useable Gates | 2,500 | 4,000 | 6,000 | 8,000 | 12,000 | 16,000 |
| Flip-flops | 282 | 452 | 636 | 820 | 1,188 | 1,500 |
| Logic Elements | 208 | 336 | 504 | 672 | 1,008 | 1,296 |
| Max user I/O pins | 78 | 120 | 136 | 152 | 184 | 298 |
| Packages | 84 pin PLCC<br>100 pin TQFP | 84 pin PLCC<br>100 pin TQFP<br>160 pin PQFP | 84 pin PLCC<br>160 pin PQFP<br>208 pin PQFP | 144 pin TQFP<br>160 pin PQFP<br>208 pin PQFP<br>225 pin BGA | 208 pin PQFP<br>240 pin PQFP | 240 pin PQFP<br>304 pin PQFP |

## Description

The Clear Logic CL8000 Laser-Configured ASIC (LASIC™) family offers the ultimate combination of performance, flexibility, and cost. This family is a system level second source to Altera Flex® 8000™ products. For designs not requiring in-system reprogrammability, design verification can be performed using the programmable Altera devices, and Clear Logic LASICs can be used for low cost, high volume production.

Clear Logic's innovative laser ASIC technology eliminates NRE costs, test vector development, ordering minimums and long lead times. No re-simulation or re-layout is required, as the device is engineered using a cell-based, PLD-like architecture. Clear Logic's TestCell™ technology ensures complete test coverage through the use of specialized testing modes which are transparent to the user.

The Clear Logic CL8000 Laser-Configured ASIC family is based upon a large array of logic elements. Each logic element contains a configurable look up table for combinatorial functions and a register for sequential operations. A group of eight logic elements forms a block. Laser-configured metal fuses implement logical functions and control signal routing

Laser configuration provides reduced cost and performance benefits. These inherent performance benefits include extremely consistent propagation delays, reduced power consumption, and improved immunity to noise and upset events.

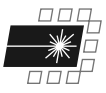
## Configuration

Clear Logic's CL8000 LASIC family is compatible with all six configuration modes defined for the Flex 8000 product family. These configuration modes include the following:

- Active Serial
- Active Parallel Up
- Active Parallel Down
- Passive Parallel Synchronous
- Passive Parallel Asynchronous
- Passive Serial

The CL8000 is already configured when it is shipped, and can be configured to bypass the FLEX 8000 configuration modes.





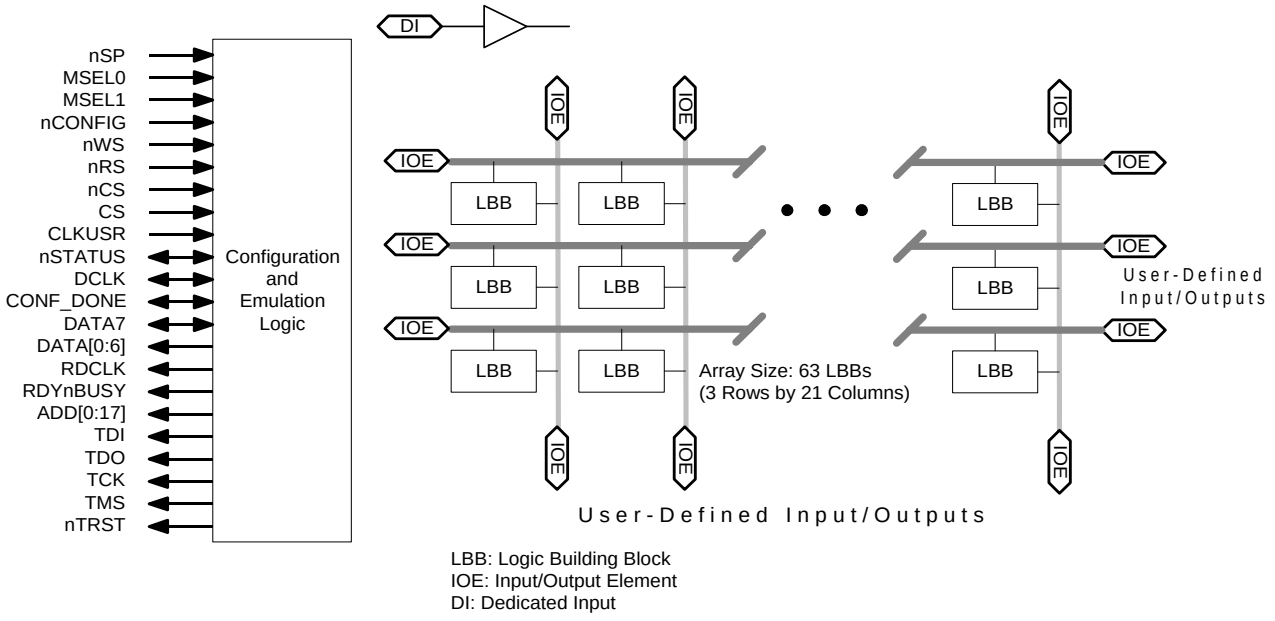
This "Instant-On" configuration mode eliminates the need for external EPROMs or microcode. In the Instant-On mode, the CL8000 device begins Initialization immediately upon a low-to-high transition on the nCONFIG pin.

## Additional Information

For further information on designing with the CL8000 LASIC family, please consult the following documents:

- *CL8K01: CL8000 Packaging Guide*. This document provides specifications and drawings for packages used by the CL8000 family.
- *CL8K02: CL8000 and System Configuration*. This document contains a detailed discussion of all aspects of configuring CL8000-based systems.
- *CL8K03: CL8000 Technology White Paper*. This document outlines the technologies employed by the CL8000 LASIC family.
- *CL8K04: Requesting a CL8000 First Article*. This document provides instructions on how to submit a bitstream file for generation of first articles.
- *CL8K05: Calculating CL8000 Power Consumption*. This document provides guidelines for calculating power consumption based on design characteristics.

## Block Diagram




LBB: Logic Building Block
IOE: Input/Output Element
DI: Dedicated Input

# Pin Configuration

| Pin Name | 84 pin PLCC | 160 pin PQFP | 208 pin PQFP |
|---|---|---|---|
| nSP | 75 | 1 | 207 |
| MSEL0 | 74 | 3 | 4 |
| MSEL1 | 53 | 38 | 49 |
| nSTATUS | 32 | 83 | 108 |
| nCONFIG | 33 | 81 | 103 |
| DCLK | 10 | 120 | 158 |
| CONF_DONE | 11 | 118 | 153 |
| nWS | 30 | 89 | 114 |
| nRS | 48 | 50 | 66 |
| RDCLK | 49 | 48 | 64 |
| nCS | 29 | 91 | 116 |
| CS | 28 | 93 | 118 |
| RDYnBUSY | 77 | 155 | 201 |
| CLKUSR | 50 | 44 | 59 |
| ADD17 | 51 | 43 | 57 |
| ADD16 | 55 | 33 | 43 |
| ADD15 | 56 | 31 | 41 |
| ADD14 | 57 | 29 | 39 |
| ADD13 | 58 | 27 | 37 |
| ADD12 | 60 | 24 | 31 |
| ADD11 | 61 | 23 | 30 |
| ADD10 | 62 | 22 | 29 |
| ADD9 | 63 | 21 | 28 |
| ADD8 | 64 | 20 | 24 |
| ADD7 | 65 | 19 | 23 |
| ADD6 | 66 | 18 | 22 |
| ADD5 | 67 | 17 | 21 |
| ADD4 | 69 | 13 | 14 |
| ADD3 | 70 | 11 | 12 |
| ADD2 | 71 | 9 | 10 |
| ADD1 | 72 | 7 | 8 |
| ADD0 | 76 | 157 | 203 |
| DATA7 | 2 | 137 | 178 |
| DATA6 | 4 | 132 | 172 |
| DATA5 | 6 | 129 | 169 |
| DATA4 | 7 | 127 | 165 |
| DATA3 | 8 | 124 | 162 |
| DATA2 | 9 | 122 | 160 |
| DATA1 | 13 | 115 | 149 |
| DATA0 | 14 | 113 | 147 |
| TDI | 45 | 55 | 72 |
| TDO | 27 | 95 | 120 |
| TCLK | 44 | 57 | 74 |
| TMS | 43 | 59 | 76 |
| nTRST | 52 | 40 | 54 |
| Dedicated Inputs | 12, 31, 54, 73 | 6, 35, 87, 116 | 7, 45, 112, 150 |
| VCCINT | 17, 38, 59, 80 | 4, 5, 26, 85, 106 | 5, 6, 33, 110, 137 |
| VCCIO | - | 25, 41, 60, 70, 80, 107, 121, 140, 149, 160 | 32, 55, 78, 91, 102, 138, 159, 182, 193, 206 |
| GND | 5, 26, 47, 68 | 15, 16, 36, 37, 45, 51, 75, 84, 86, 96, 97, 117, 126, 131, 154 | 19, 20, 46, 47, 60, 67, 96, 109, 111, 124, 125, 151, 164, 171, 200 |
| NC (No Connect) | | 2, 39, 82, 119 | 1, 2, 3, 16, 17, 18, 25, 26, 27, 34, 35, 36, 50, 51, 52, 53, 104, 105, 106, 107, 121, 122, 123, 130, 131, 132, 139, 140, 141, 154, 155, 156, 157, 208 |
| Total user I/O pins | 64 | 114 | 132 |

# DC Electrical Specifications

## Absolute Maximum Ratings

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | -2.0 | 7.0 | V |
| $V_I$ | DC input voltage[1] | | -2.0 | 7.0 | V |
| $I_{OUT}$ | DC output current, per pin | | -25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | -65 | 150 | °C |
| $T_{AMB}$ | Ambient temperature | Under bias | -65 | 135 | °C |
| $T_J$ | Junction temperature | Under bias | | 135 | °C |

## Recommended Operating Conditions[2]

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage, internal logic and input buffers<br>Commercial Grade Devices<br>Industrial Grade Devices | | <br>4.75<br>4.50 | <br>5.25<br>5.50 | V |
| $V_{CCIO}$ | DC input voltage<br>5.0 volt commercial<br>5.0 volt industrial<br>3.3 volt operation | | <br>4.75<br>4.50<br>3.00 | <br>5.25<br>5.50<br>3.60 | V |
| $V_I$ | Input voltage | | 0 | $V_{CCINT}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Operating temperature<br>Commercial temperature range<br>Industrial temperature range | | <br>0<br>-40 | <br>70<br>85 | °C |
| $t_R$ | Input signal rise time | | | 40 | ns |
| $t_F$ | Input signal fall time | | | 40 | ns |
| $t_{RVCC}$ | $V_{CC}$ rise time | | | 100 | ms |

## DC Electrical Characteristics (over the operating range)

| Symbol | Parameter | Conditions | Min | Typ[3] | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | $V_{CCINT}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage | | -0.3 | | 0.8 | V |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = -4.0 mA, $V_{CCIO}$ = $V_{CCIO[Min]}$ | 2.4 | | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 12.0 mA, $V_{CCIO}$ = $V_{CCIO[Min]}$ | | | 0.45 | V |
| $I_{IN}$ | Input Leakage Current | $V_I$ = $V_{CC}$ or GND | -10 | | 10 | µA |
| $I_{OZ}$ | Output Leakage Current | $V_I$ = $V_{CC}$ or GND | -40 | | 40 | µA |
| $I_{CC0}$ | Standby Current | $V_I$ = GND, no load | | 0.5 | 10 | mA |

### Capacitance[4]

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 10 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 10 | pF |

## AC Electrical Specifications

### I/O Element Timing Parameters[5]

| | | | speed: -2 | | speed: -3 | | speed: -4 | | |
|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{IOD}$ | IOE register data delay | | | 0.7 | | 0.8 | | 0.9 | ns |
| $t_{IOC}$ | IOE register control signal delay | | | 1.7 | | 1.8 | | 1.9 | ns |
| $t_{IOE}$ | Output enable delay | | | 1.7 | | 1.8 | | 1.9 | ns |
| $t_{IOCO}$ | IOE register clock to output delay | | | 1.0 | | 1.0 | | 1.0 | ns |
| $t_{IOCOMB}$ | IOE combinatorial delay | | | 0.3 | | 0.2 | | 0.1 | ns |
| $t_{IOSU}$ | IOE register setup time before clock | | 1.4 | | 1.6 | | 1.8 | | ns |
| $t_{IOH}$ | IOE register hold time after clock | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{IOCLR}$ | IOE register clear delay | | | 1.2 | | 1.2 | | 1.2 | ns |
| $t_{IN}$ | Input pad and buffer delay | | | 1.5 | | 1.6 | | 1.7 | ns |
| $t_{OD1}$ | Output buffer and pad delay | slow slew rate = off, $V_{CCIO}$ = 5.0v, $C_L$ = 35 pF | | 1.1 | | 1.4 | | 1.7 | ns |
| $t_{OD2}$ | Output buffer and pad delay | slow slew rate = off, $V_{CCIO}$ = 3.3v, $C_L$ = 35 pF | | 1.6 | | 1.9 | | 2.2 | ns |
| $t_{OD3}$ | Output buffer and pad delay | slow slew rate = on, $C_L$ = 35 pF, $V_{CCIO}$ = 3.3v or 5.0v | | 4.6 | | 4.9 | | 5.2 | ns |
| $t_{ZX}$ | Output buffer disable delay | $C_L$ = 5 pF | | 1.4 | | 1.6 | | 1.8 | ns |
| $t_{ZX1}$ | Output buffer disable delay | slow slew rate = off, $V_{CCIO}$ = 5.0v, $C_L$ = 35 pF | | 1.4 | | 1.6 | | 1.8 | ns |
| $t_{ZX2}$ | Output buffer disable delay | slow slew rate = off, $V_{CCIO}$ = 3.3v, $C_L$ = 35 pF | | 1.6 | | 2.1 | | 2.3 | ns |
| $t_{ZX3}$ | Output buffer disable delay | slow slew rate = on, $C_L$ = 35 pF, $V_{CCIO}$ = 3.3v or 5.0v | | 4.9 | | 5.1 | | 5.3 | ns |

### External Timing Parameters[4]

| | | | speed: -2 | | speed: -3 | | speed: -4 | | |
|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{DRR}$ | Register to register delay via four LEs, three row interconnects, and four local interconnects | | | 16 | | 20 | | 25 | ns |
| $t_{ODH}$ | Output data hold time after clock | | 1.0 | | 1.0 | | 1.0 | | ns |

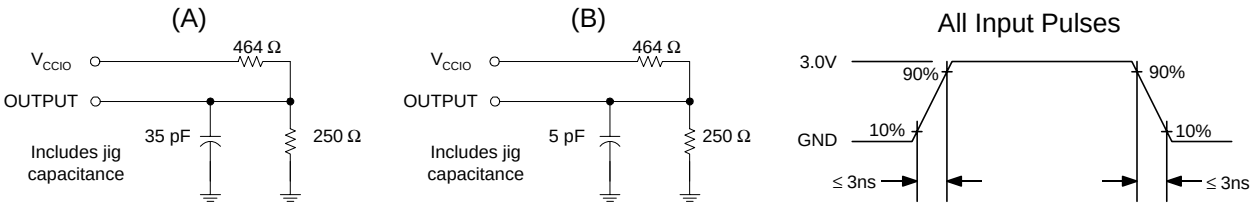
## Logic Element Timing Parameters[5]

| Symbol | Parameter | Conditions | speed: -2 Min | speed: -2 Max | speed: -3 Min | speed: -3 Max | speed: -4 Min | speed: -4 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{LUT}$ | Look up table delay for data-in | | | 2.0 | | 2.3 | | 3.0 | ns |
| $t_{CLUT}$ | Look up table delay for carry-in | | | 0.0 | | 0.2 | | 0.1 | ns |
| $t_{RLUT}$ | Look up table delay for LE register feedback | | | 0.9 | | 1.6 | | 1.6 | ns |
| $t_{GATE}$ | Cascade gate delay | | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{CASC}$ | Cascade chain routing delay | | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{CICO}$ | Carry-in to carry-out delay | | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{CGEN}$ | Data-in to carry-out delay | | | 0.4 | | 0.9 | | 0.8 | ns |
| $t_{CGENR}$ | LE register feedback to carry-out delay | | | 0.9 | | 1.4 | | 1.5 | ns |
| $t_{C}$ | LE register control signal delay | | | 1.6 | | 1.8 | | 2.4 | ns |
| $t_{CH}$ | Clock high time | | 1.7 | | 1.7 | | 2.7 | | ns |
| $t_{CL}$ | Clock low time | | 1.7 | | 1.7 | | 2.7 | | ns |
| $t_{CO}$ | LE register clock-to-output delay | | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{SU}$ | LE register setup time before clock | | 0.8 | | 1.0 | | 1.1 | | ns |
| $t_{H}$ | LE register hold time after clock | | 0.9 | | 1.1 | | 1.4 | | ns |
| $t_{PRE}$ | LE register preset delay | | | 0.6 | | 0.7 | | 0.8 | ns |
| $t_{CLR}$ | LE register clear delay | | | 0.6 | | 0.7 | | 0.8 | ns |

## Interconnect Timing Parameters[5]

| Symbol | Parameter | Conditions | speed: -2 Min | speed: -2 Max | speed: -3 Min | speed: -3 Max | speed: -4 Min | speed: -4 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{LABCASC}$ | Cascade delay between LEs in different LABs | | | 0.3 | | 0.4 | | 0.4 | ns |
| $t_{LABCARRY}$ | Carry delay between LEs in different LABs | | | 0.3 | | 0.4 | | 0.4 | ns |
| $t_{LOCAL}$ | LAB local interconnect delay | | | 0.5 | | 0.5 | | 0.7 | ns |
| $t_{ROW}$ | Row interconnect routing delay | | | 5.0 | | 5.0 | | 5.0 | ns |
| $t_{COL}$ | Column interconnect routing delay | | | 3.0 | | 3.0 | | 3.0 | ns |
| $t_{DIN\_C}$ | Dedicated input to LE control delay | | | 5.0 | | 5.0 | | 5.5 | ns |
| $t_{DIN\_D}$ | Dedicated input to LE data delay | | | 7.0 | | 7.0 | | 7.5 | ns |
| $t_{DIN\_IO}$ | Dedicated input to IOE control delay | | | 5.0 | | 5.0 | | 5.5 | ns |

## AC Test Conditions




## Notes to Tables

1. During transitions, inputs may undershoot to -2.0v for periods shorter than 20ns. Otherwise, minimum DC input voltage is 0.3v.

2. The following devices do not have $V_{CCIO}$ pins: CL8282A, CL8452A. For these devices, all references to $V_{CCIO}$ should be changed to $V_{CCINT}$

3. Typical values are at $V_{CC}$ of 5.0 volts and ambient temperature of 25 °C.

4. Guaranteed but not tested. Characterized initially, and after any design changes which may affect these parameters.

5. Internal timing delays are based on characterization, and cannot be explicitly tested. Internal timing parameters should be used for performance estimation only.

## Ordering Information

| Part Number | Temperature Range | Package Type | Speed | Altera Equivalent |
|---|---|---|---|---|
| CL8636ALC84-4 | Commercial | 84-pin PLCC | -4 (slowest) | EPF8636ALC84-4 |
| CL8636ALC84-3 | | | -3 (fastest) | EPF8636ALC84-3 |
| CL8636AQC160-4 | | 160-pin Plastic QFP | -4 (slowest) | EPF8636AQC160-4 |
| CL8636AQC160-3 | | | -3 (fastest) | EPF8636AQC160-3 |
| CL8636AQC208-4 | | 208-pin Plastic QFP | -4 (slowest) | EPF8636AQC208-4 |
| CL8636AQC208-3 | | | -3 | EPF8636AQC208-3 |
| CL8636AQC208-2 | | | -2 (fastest) | EPF8636AQC208-2 |
| CL8636ALI84-4 | Industrial | 84-pin PLCC | -4 | EPF8636ALI84-4 |