CLEAR LOGIC

Introducing The Clear Logic CL7000 LPLD™* Families

*Laser-Processed Logic Device

www.clear-logic.com

CLEAR LOGIC

Who Is Clear Logic?

- Founded In May, 1996
  - Privately Funded
  - Integrated Device Technology is Major Investor
  - Wafer Foundry: IDT Salinas, CA
  - Assembly Partners: Amkor and ASAT
- Focus: Production Alternatives to Altera
  - Low Cost and Easy to Use

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Programmable Logic

- Programmable Logic Advantages
  - Easy-To-Use, Flexible
  - Time-to-Market Benefits
- Programmable Logic Disadvantages
  - Unit Cost is High
  - High Power Consumption
  - Lack of Design Security

Originally Developed To Be Prototyping Tool Only!

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Clear Logic: Production Alternatives to Altera

- No Customer Engineering Involvement:
  - Quick, Easy Path To Lower Cost & Power
  - Bitstream Or Programming File Is All We Need
  - No Customer Design Reviews or Test Vectors
  - Factory Tested With 100% Fault Coverage
  - Eliminate Boot EPROMs - No Board Changes

CLEAR LOGIC

It’s Easy To Do Business With Us

- Two Free Samples in Two Weeks
- Standard Product Business Terms:
  - Never Any NRE Charges
  - No Minimum Order Quantities
  - Four Week Production Lead Time
  - 30 Day Cancellation Window

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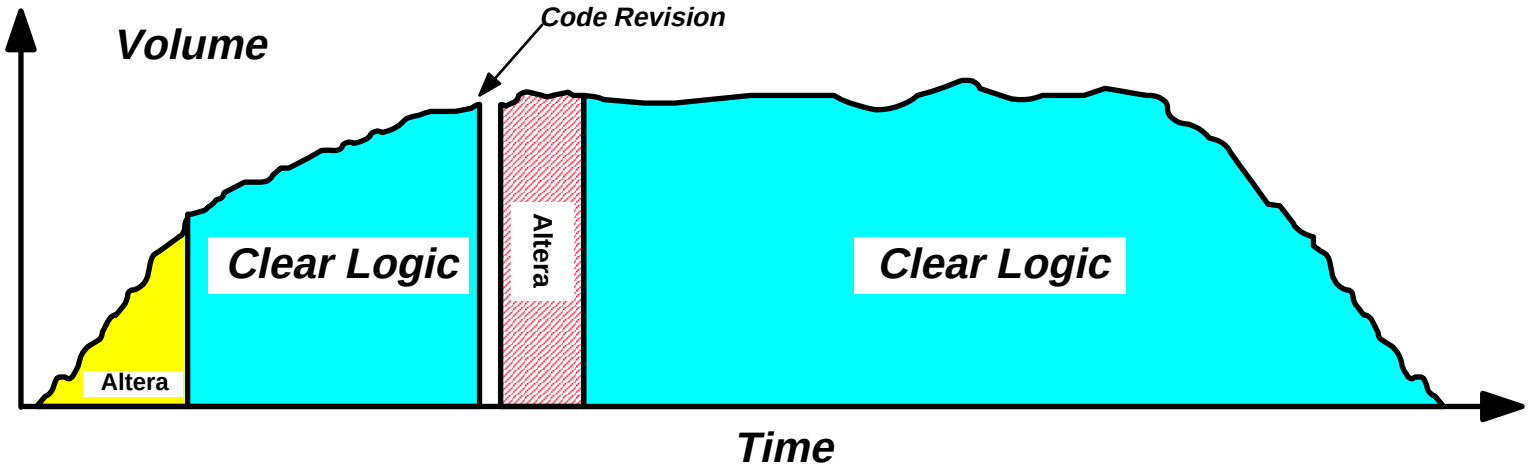
The Ultimate Production Solution

Quick & Easy	*Lower Cost & Power*	*No NRE*
No Inventory Problem	*No Order Minimums*	*Eliminate EPROMs*



"NO RISK - BIG RETURNS"

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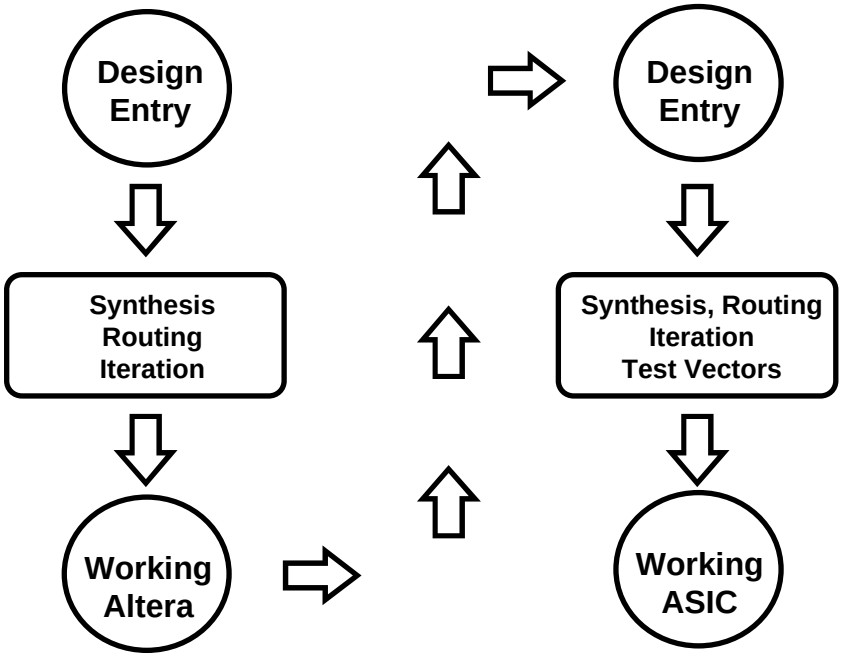
The Problem With "ASIC Conversions"



Really Two <u>Different</u> Designs….
Not A True "Conversion"!!!

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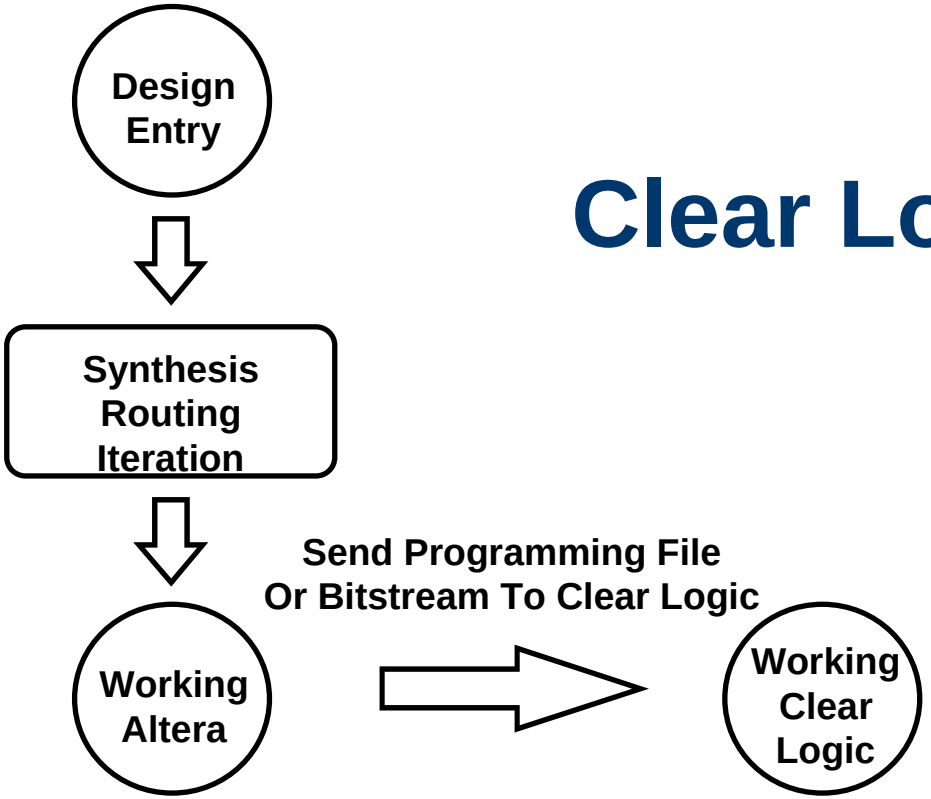

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We <u>Map</u> Your Design Directly To A Socket-Compatible Device

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Clear Logic
Product Families

NEW! CL7000 LPLD™

- Production Replacement for MAX 7000
- Sampling Q4 98

- CL8000A LASIC™
  - Production Replacement for FLEX 8000A
  - CL8000A Introduced in January, 1998

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Introducing Clear Logic LPLD

- LPLD™ Laser-Processed Logic Device
  - Functional Equivalent to Pre-Programmed CPLD
  - Replace MAX 7000, MAX 7000E, & MAX 7000S
  - Sampling CL7128E and CL7128S in Dec 98
  - 20% to 50% Lower Unit Cost

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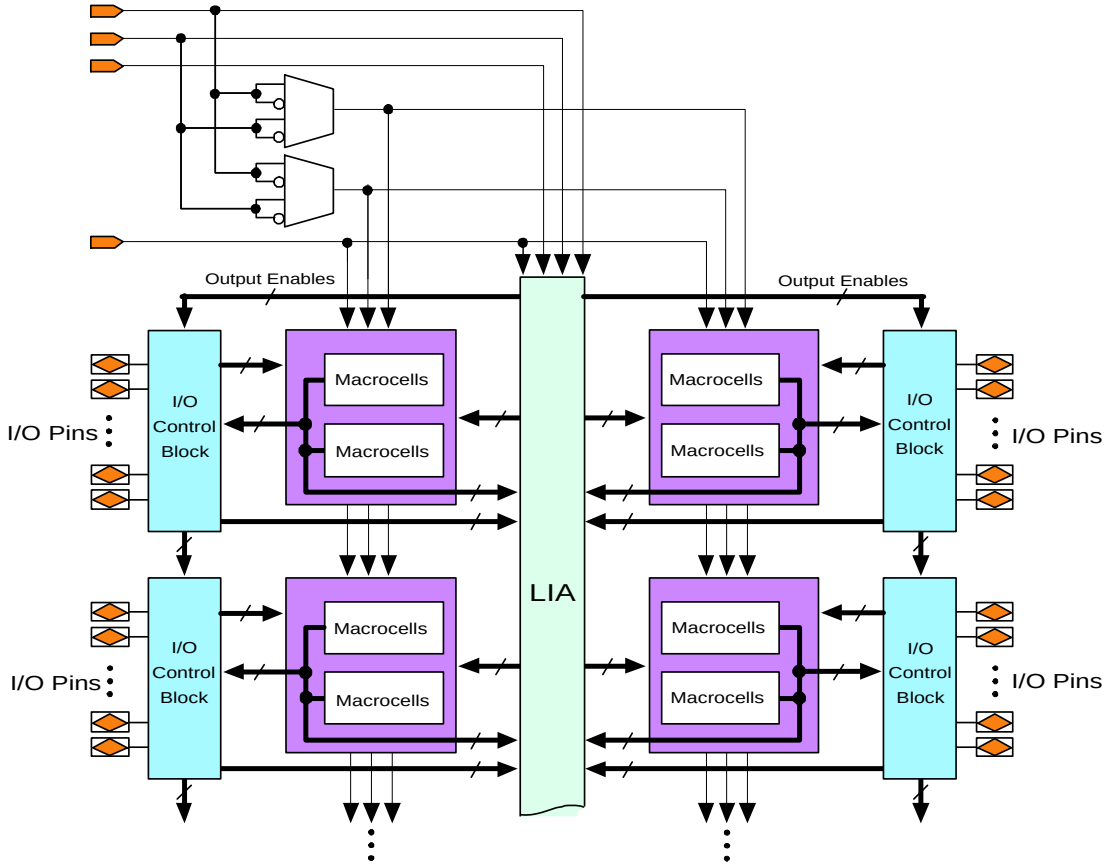
Architecture Similar To MAX 7000



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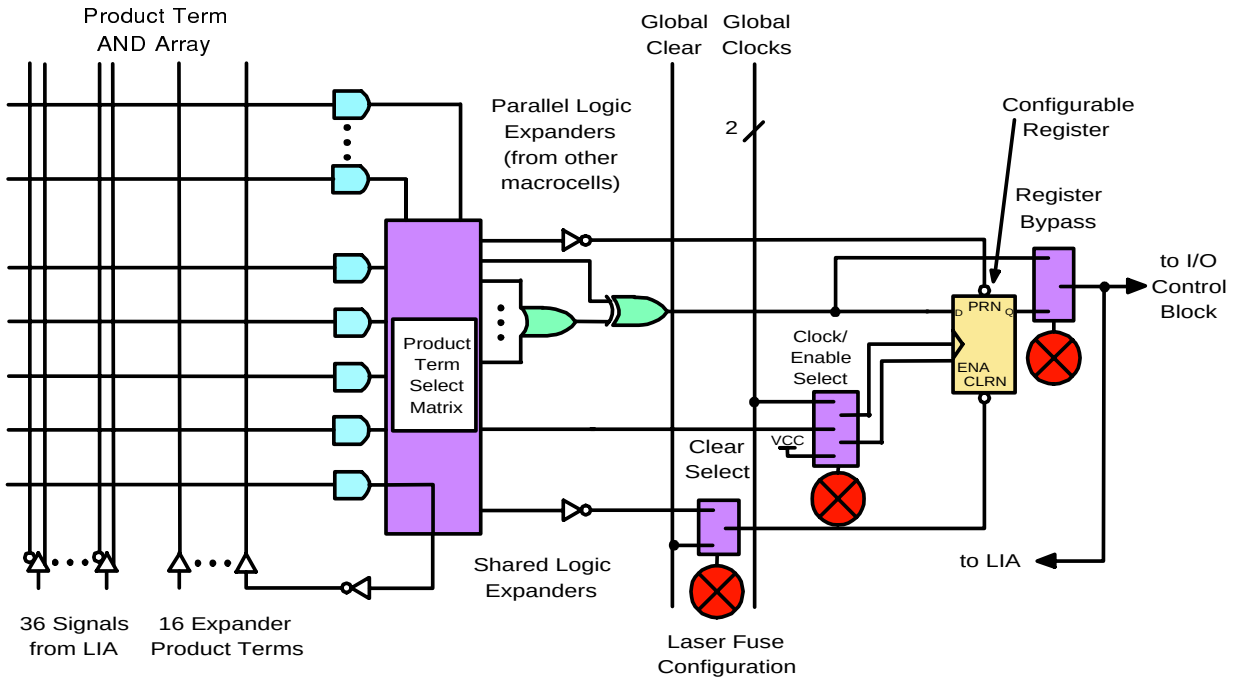
MacroCell Similar To MAX 7000



CL7000 Macrocell

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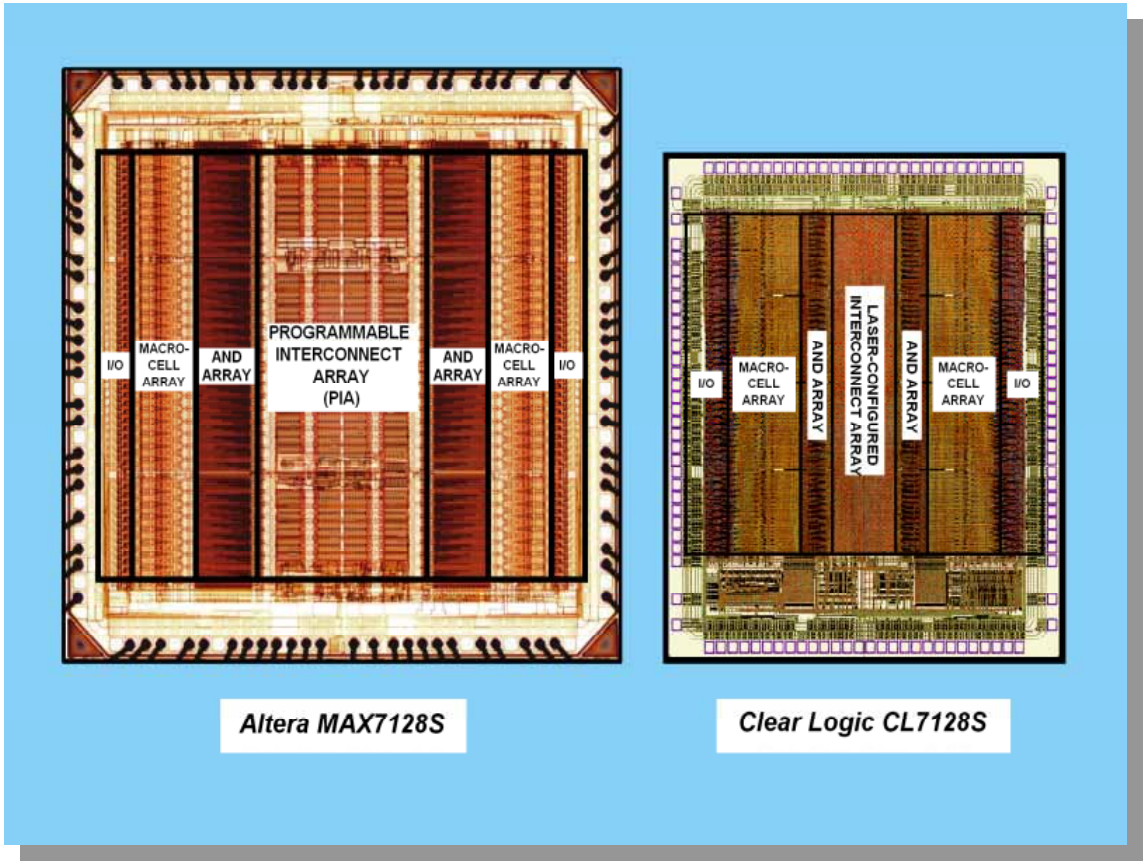
LPLD Cost Reduction



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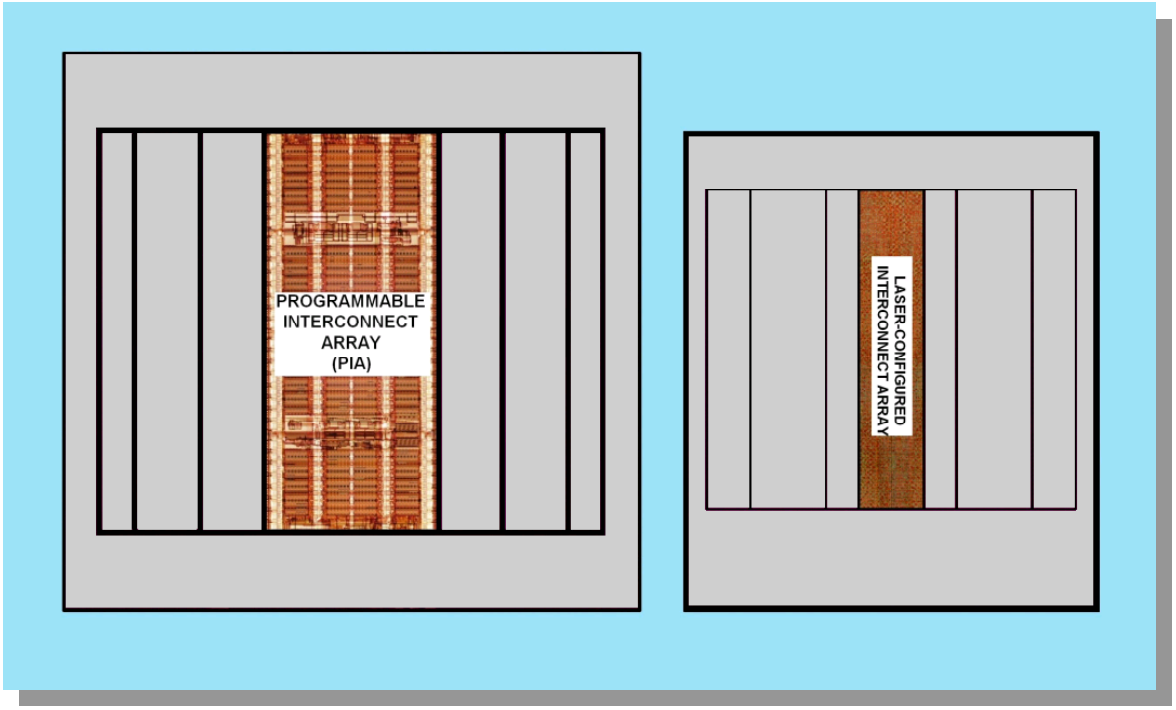
Interconnect Array



Clear Logic: 72% Less Interconnect Area!!

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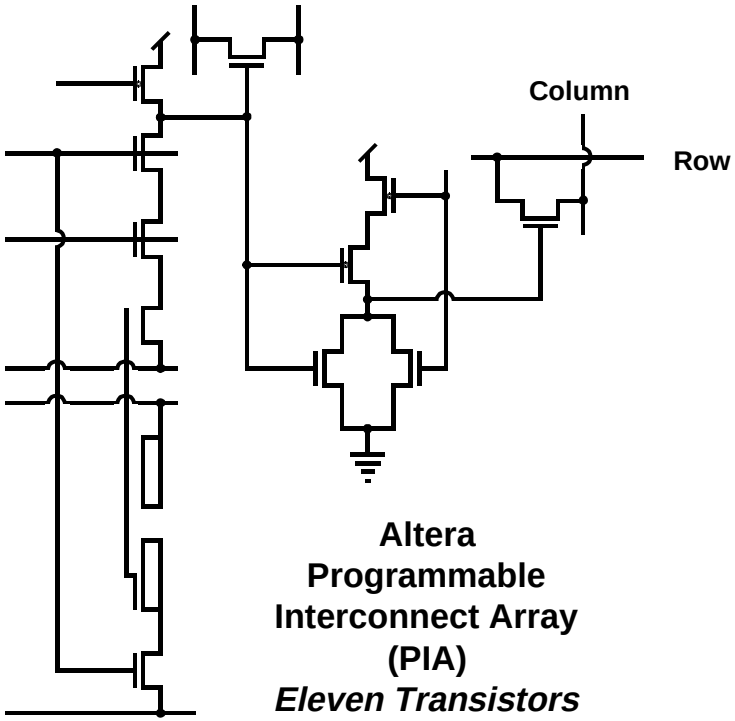
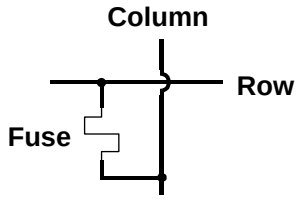
Laser-Configured Interconnect Array



Altera Programmable Interconnect Array (PIA)
Eleven Transistors



Clear Logic Laser-Configured Interconnect Array (LIA)
Zero Transistors!!

All Transistors Eliminated in the LIA!!

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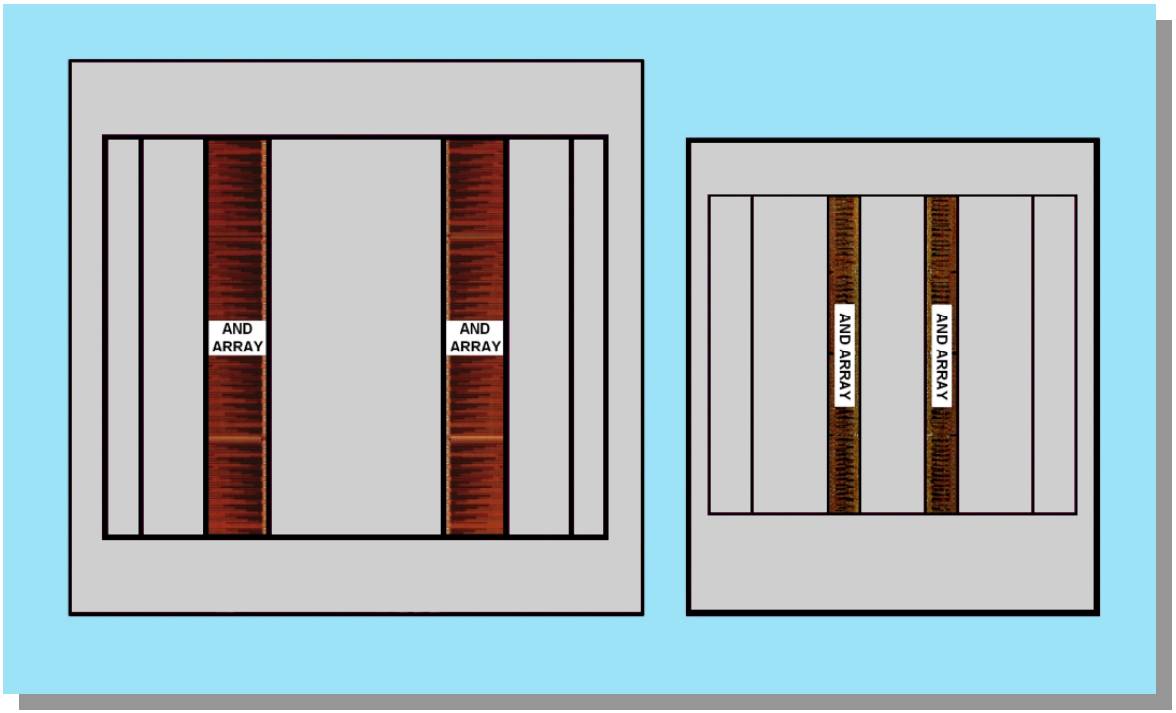
Product Term AND Array



Clear Logic: 55% Less AND Array Area!!

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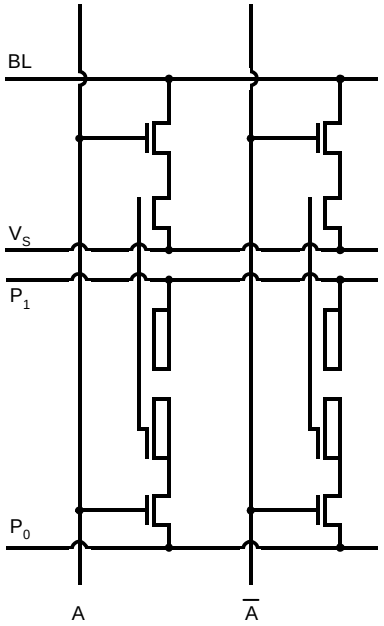
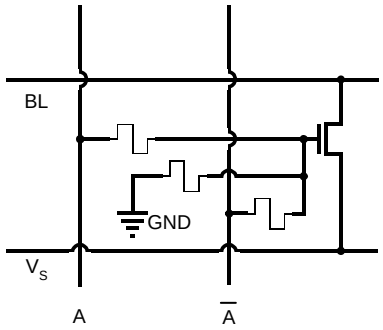
Product Term AND Array



Altera
Programmable
AND Array
Six Transistors



Clear Logic
Laser-Configured
AND Array
1 Transistor + 3 Fuses!!

80% of Transistors <u>Eliminated</u> in AND Array

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Compare to Pre-Programmed CPLDs

	CL7000 LPLD	MAX 7000 CPLD
Re-Synthesis Required	No	No
Re-Routing Required	No	No
Test Vector Generation	No	No
NRE Required	No	No
Minimum Order Quantity	No	No
100% Fault Coverage Provided	Yes	N/A
Prototype Lead Times	2 Weeks	1 Day
Hi-Volume Lead Times	4 Weeks	4 Weeks
Price	X	Up to 2X

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CL7000 LPLD™ Products

Altera	*Clear Logic*	*MacroCells*	*Speed*	*Availability*
EPM7128E/S	**CL7128E/S**	**128**	**-6**	**Jan 99**
EPM7256E/S	**CL7256E/S**	**256**	**-7**	**Feb 99**
EPM7192E/S	**CL7192E/S**	**192**	**-7**	**Mar 99**
EPM7160E	**CL7160E**	**160**	**-7**	**Apr 99**
EPM7096	**CL7096**	**96**	**-7**	**Jun 99**

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Clear Logic's Original CL8000A Family Replaces FLEX 8000A In Volume Production

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A Broad Offering of CL8000As

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Clear Logic CL8000A Update

- Shipped Over 170 Different First Article Projects
- 70% Of Customers Select “Instant-On”
- Logic/Timing Fully Compatible To FLEX 8K
- Shipping Production Since April, 1998

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CL8000A Product Family

- Converts FLEX 8000A FPGAs to LASIC™
  - Proven Functional and Timing Compatibility
  - Lower Cost and Power
  - Same “No Hassle” Benefits as LPLD

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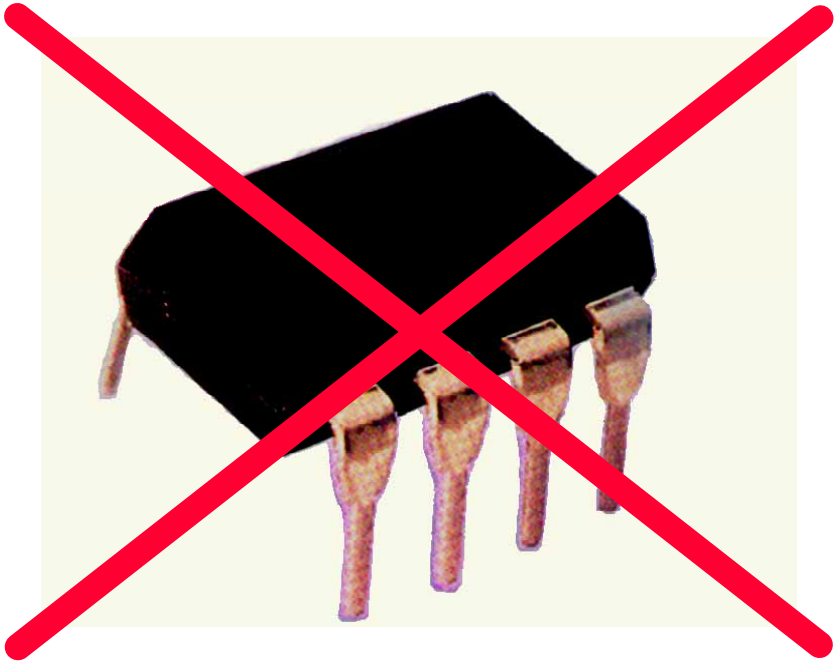
And *Additional* Savings.....



***Eliminate* Configuration EPROMs**
Without PC Board Changes

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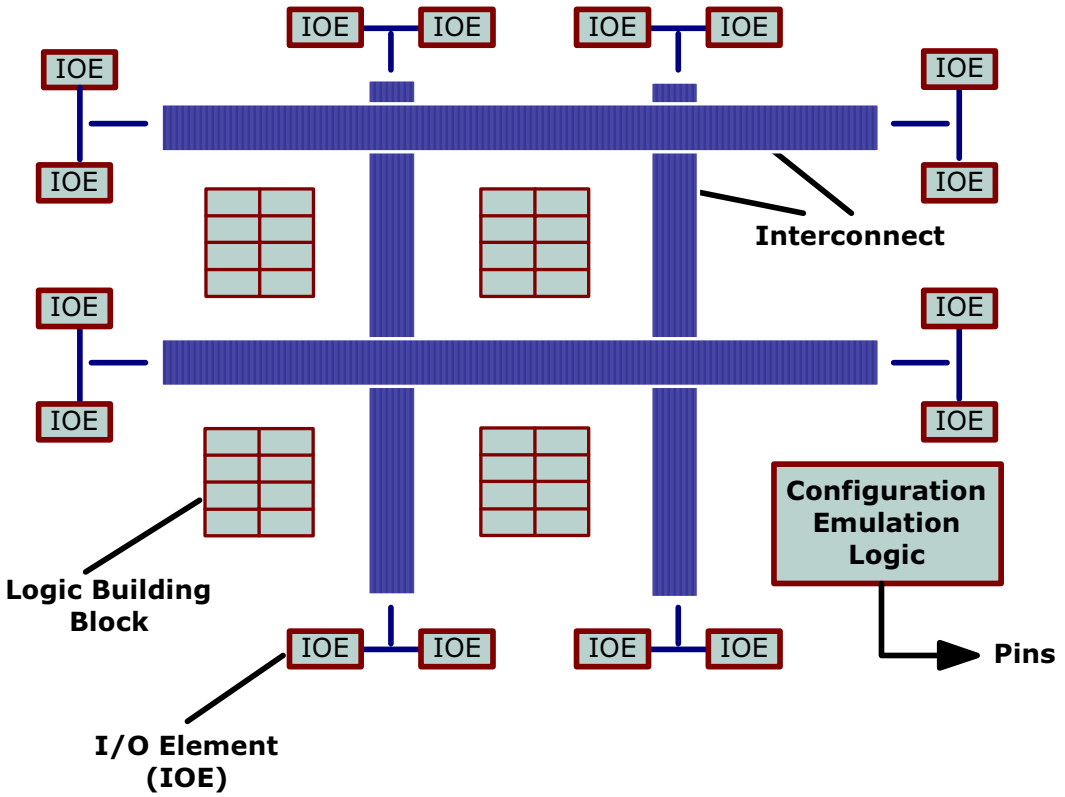
CL8000A Architecture Similar To FLEX 8K FPGA



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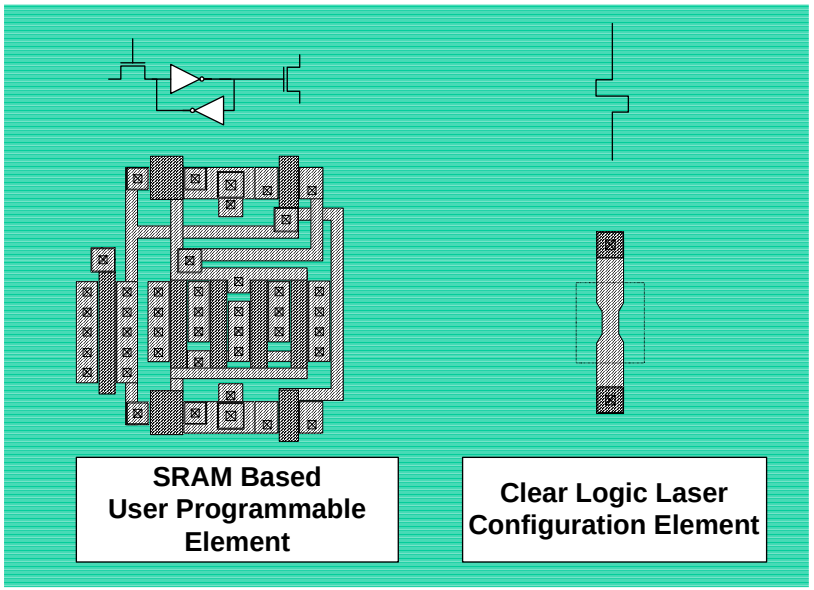
CL8000A Configuration Element

- New Architecture
  - Smaller Die Size Leads to **Lower Cost**
  - Simplified Configuration Elements



Five Times Area Improvement for Configuration Elements!

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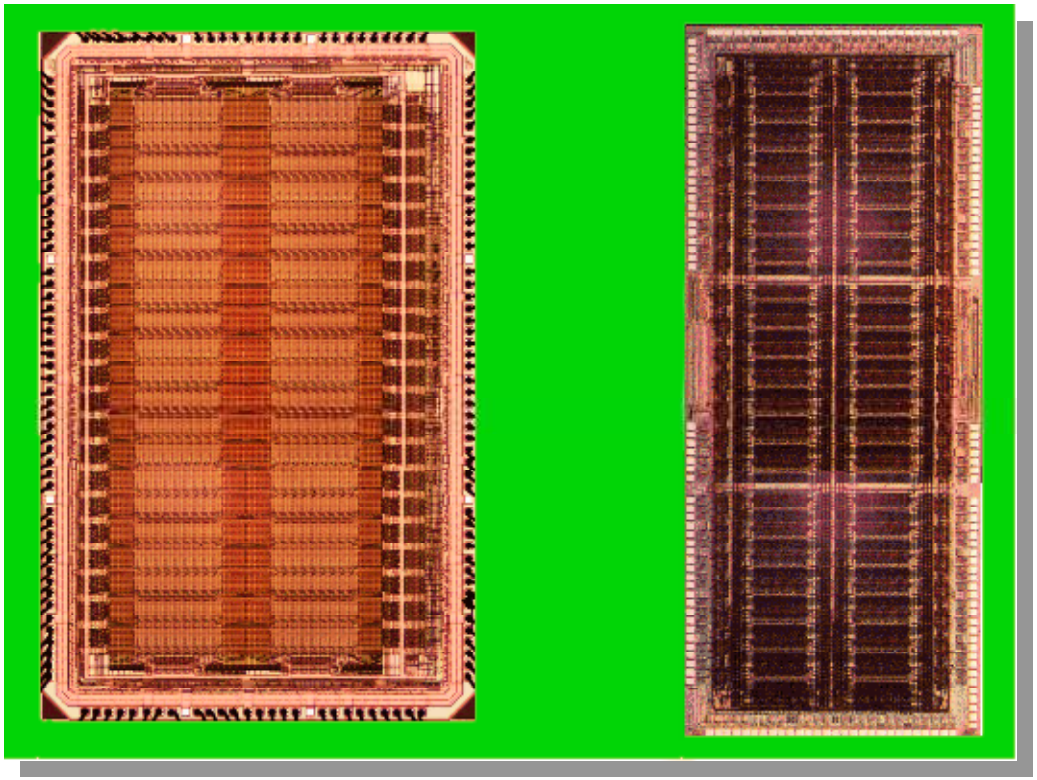
Die Size Comparison



Altera EPF8452A

Clear Logic CL8452A

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Compare CL8000A LASIC™ to ASIC

	Clear Logic	ASIC
Re-Synthesis Required	**No**	**Yes**
Re-Routing Required	**No**	**Yes**
Test Vector Generation	**No**	**Yes**
NRE Required	**No**	**Yes**
Large Minimum Order Quantity	**No**	**Yes**
100% Fault Coverage Provided	**Yes**	**No**
Prototype Lead Times	**2 Weeks**	**1 Month**
Production Lead Times	**4 Weeks**	**3 Months**

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CL8000A LASIC™ Products

Altera	*Clear Logic*	*Gates*	*Status*	*Availability*
EPF8282A	CL8282A	2,500	NEW	Nov 98
EPF8452A	CL8452A	4,000	Jan 98	Now
EPF8636A	CL8636A	6,000	June 98	Now
EPF8820A	CL8820A	8,000	NEW	Now
EPF81188A	CL81188A	12,000	NEW	Now

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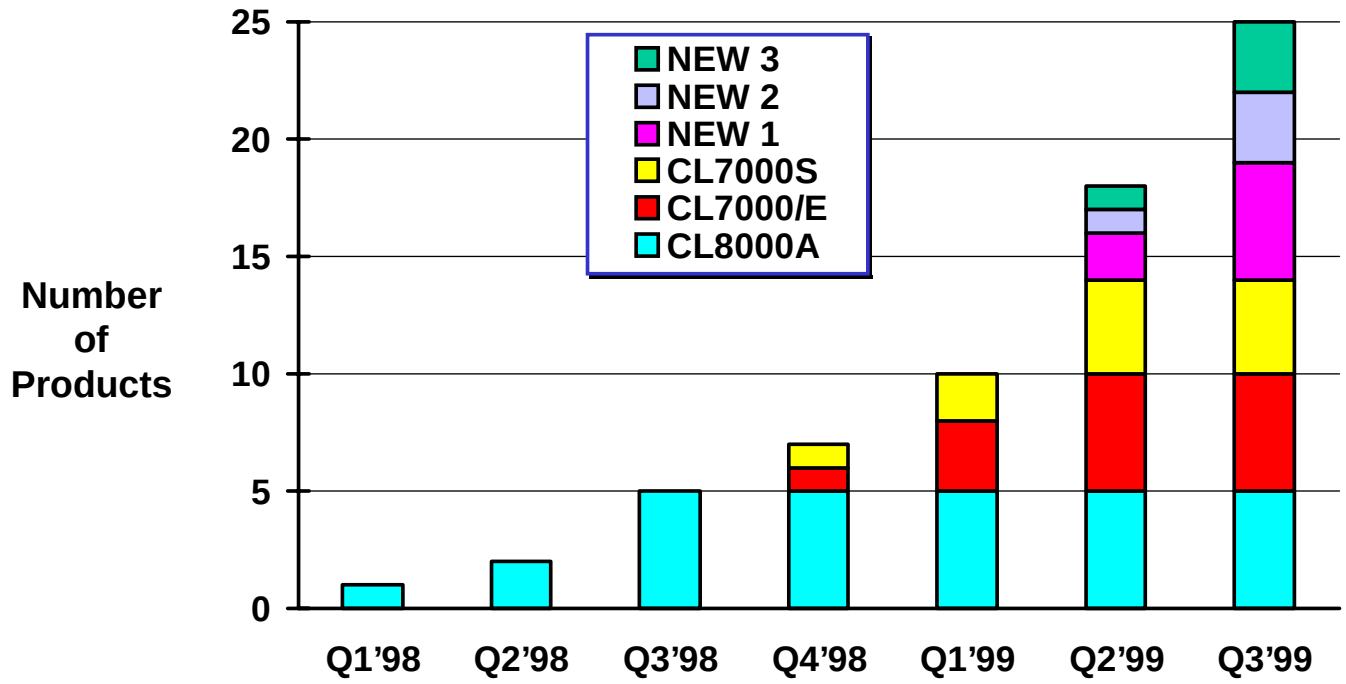
Product Family Road Map



CLEAR LOGIC

The Way We Do It

1. Chip Designed For Compatibility
2. ClearShot™ Bitstream Extraction
3. ClearFire™ Laser Configuration
4. NoFault™ Test Technology

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1. Chip Designed for Compatibility

- Altera Source Design *Maps* To Clear Logic
- No Resynthesis
- Routing & Placement From Source Device
- Timing Relationships Preserved
- I/O Matched To Source Device

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2. ClearShot

- Automated Bitstream Extraction
- Performed In Less Than One Hour
- Maps Design To Laser Fuse Map
- Passes Data To NoFault™ Testing
- No Customer Software

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3. ClearFire

- Laser Configuration Process
- Performed At Production Rates
- Proven Laser Technology

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Laser Configuration

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Laser Configuration

- No Masks = No Up-Front Cost
- Each Die Unique = No Min Order Qty
- Fewer Transistors = Lower Power
- Last Wafer Step = Short Lead Time

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4. NoFault™

- Integrated Test Generation/Process
- Built-in Chip Level Scan Test
- Automatic Test Vector Generation
- 100% Fault Coverage

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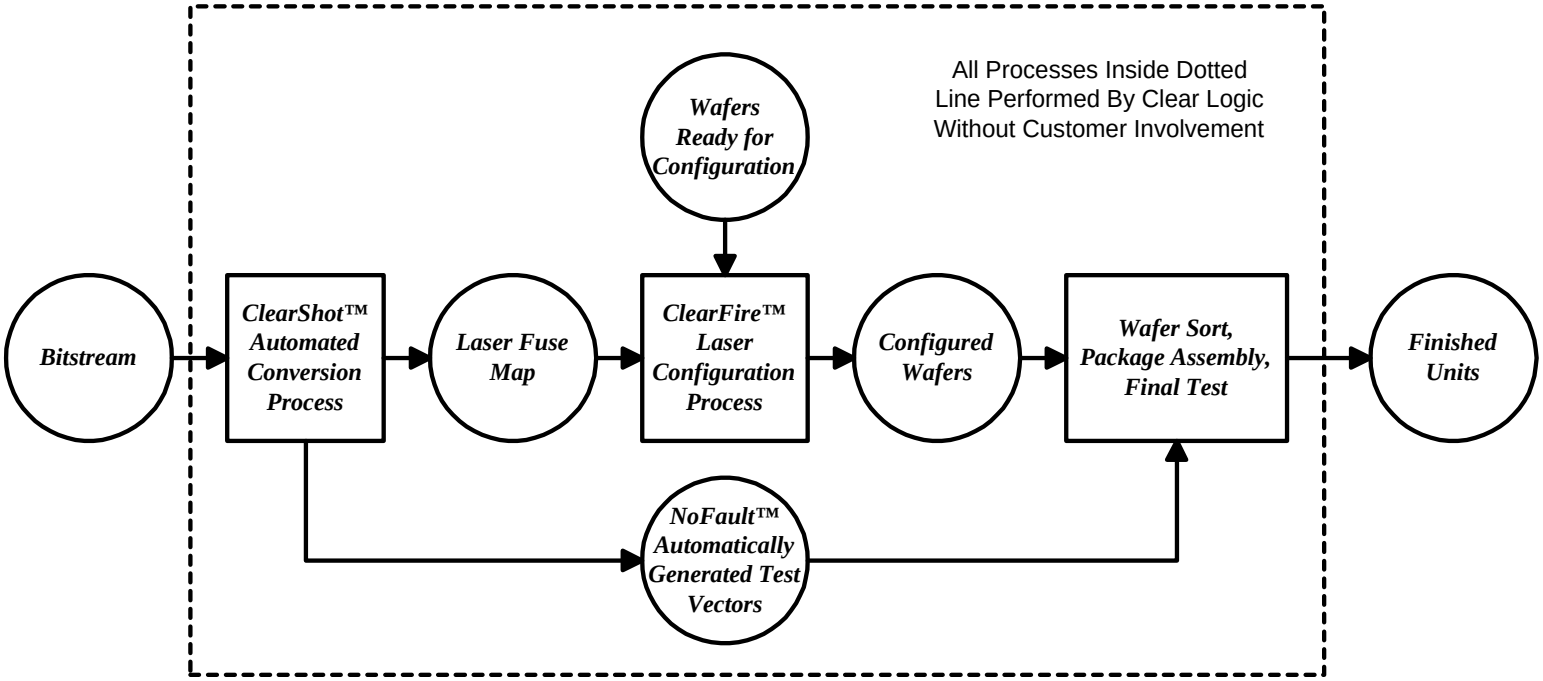
Clear Logic Process



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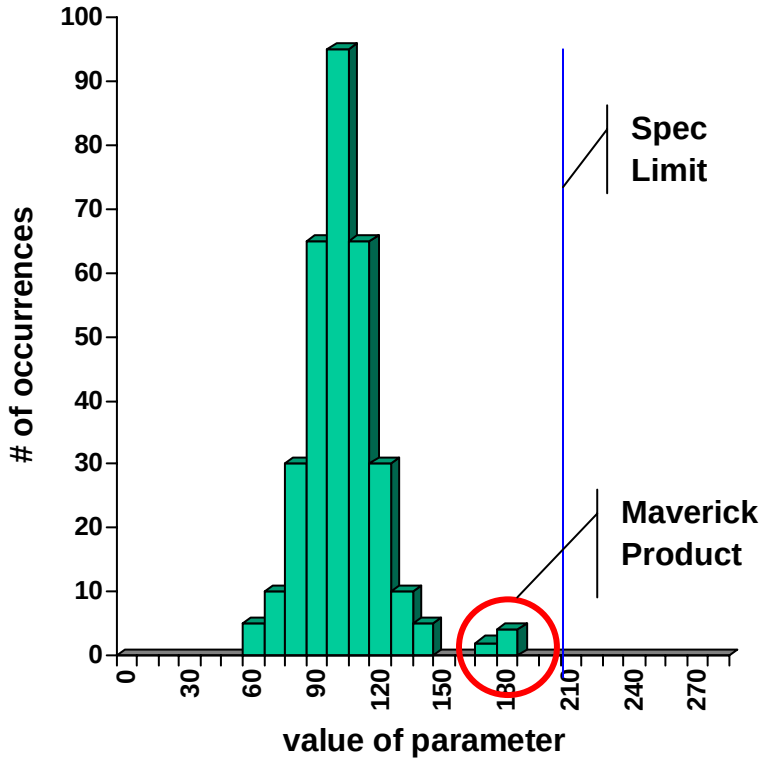
Elimination of Mavericks



- "Maverick" Philosophy Pioneered by IBM and Others
- Eliminate Products Outside Normal Distribution
- Clear Logic Program Follows Guidelines Established By JEDEC (EIA/JESD50)
- Eliminating Maverick Product Reduces Field Failure Rate

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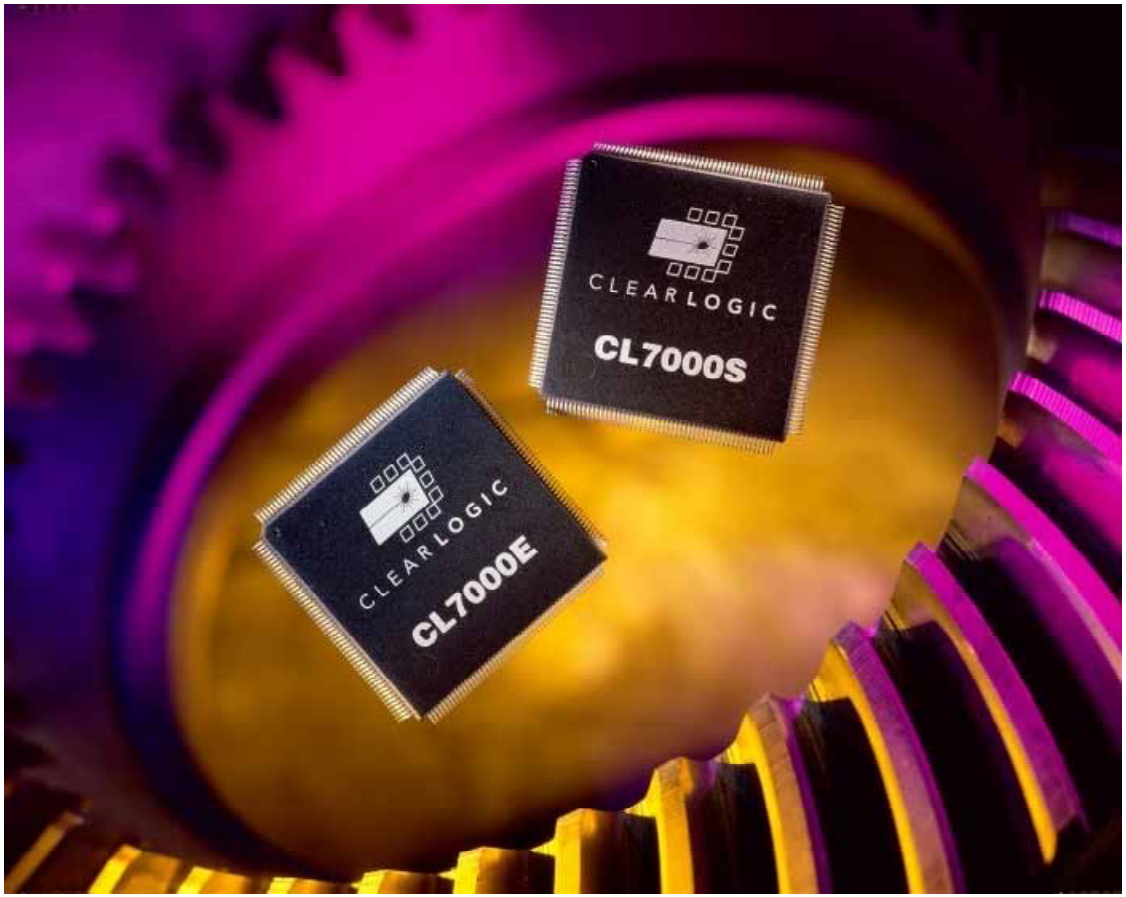
The Clear Alternative to MAX 7000



CLEAR LOGIC

Let Us Be Part of the Solution...

For Existing Programs, Provide us a copy of the .HEX or .POF File. We'll Provide First Articles for Evaluation within two Weeks, Completely free of charge.

For New Programs, Design with Clear Logic in Mind. It's the Quickest Path to a Low Cost, Alternative Solution for Volume Production.