This user guide addresses the features, setup and operation of the VersaKit development system for the evaluation and programming of Ramtron's high performance VRS51L2xxx microcontrollers.

Table of Contents

1 VersaKit-20xx Development System Overview

The VersaKit-20xx development kit is a plug and play evaluation system for the VRS51L2xxx series of high performance, highly integrated 8051 microcontrollers. The VersaKit-20xx provides a complete and comprehensive programming and development platform, with ample prototyping space and easy access to chip peripherals and I/Os.

The VersaKit-20xx development system features:

- VRS51L2070 in QFP-64 package soldered onboard (contact Ramtron for details on the VRS51L2170 in QFP-44 package)
- FM31xx MCU companion, FM25xx SPI FRAM and FM24xx I²C FRAM devices installed
- 5x2 header to connect Versa-JTAG programming/debugging interface
- 2 DB9 serial port female connectors and 1 onboard RS-232 transceiver with configuration jumper
- Tact switches for manual reset and external interrupt of the processor
- Four sets of 16 probing points around VRS51L2070 device
- 22x2 header alongside prototyping area to access QFP-44 device pins (header pin number corresponds to device pin number)
- 32x2 header alongside prototyping area to access QFP-64 device pins (header pin number corresponds to the device pin number)
- Prototyping space
- Character LCD interface header footprint
- External crystal footprint
- 8 uncommitted user LEDs
- Onboard 3.3V regulator with power-on LED
- Optional regulator footprint

1.1 The VersaKit-20xx ships complete with:

- Development board that supports the VRS51L2070
- Versa-JTAG programming/debugging interface
- DB25 Parallel Cable
- Power supply

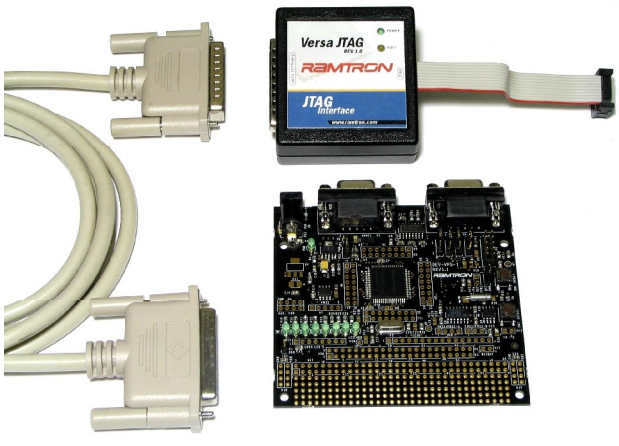


Figure 1: VersaKit-20xx complete kit

1.2 Supported Devices

The VersaKit-20xx ships with a VRS51L2070-40-Q soldered onto the development board.

VRS51L2170 Evaluation

Note that the VersaKit-20xx can also be used for evaluation of the VRS51L2170 (44-pin version of the VRS51L2070), since its peripherals are a subset of the VRS51L2070. A dedicated development board will be available for the 44-pin VRS51L2170 (part number VersaKit-21xx) in the future that is based on the VersaKit-20xx (there is a 44-pin QFP footprint underneath the installed VRS51L2070 on the VersaKit-20xx that will be used for this purpose). The user should consult the Ramtron website for availability of the VersaKit-21xx development board. In the short term, code can be developed on the VRS51L2070 and easily ported to the VRS51L2170.

Note, therefore, that for the sake of completeness, this User Guide will include a discussion of headers, etc., that are associated with the VersaKit-21xx development board.

2 Overview of the VersaKit-20xx Development Board

The figure below offers a detailed look at the VersaKit-20xx development board and its principal features, which will be addressed in this document.

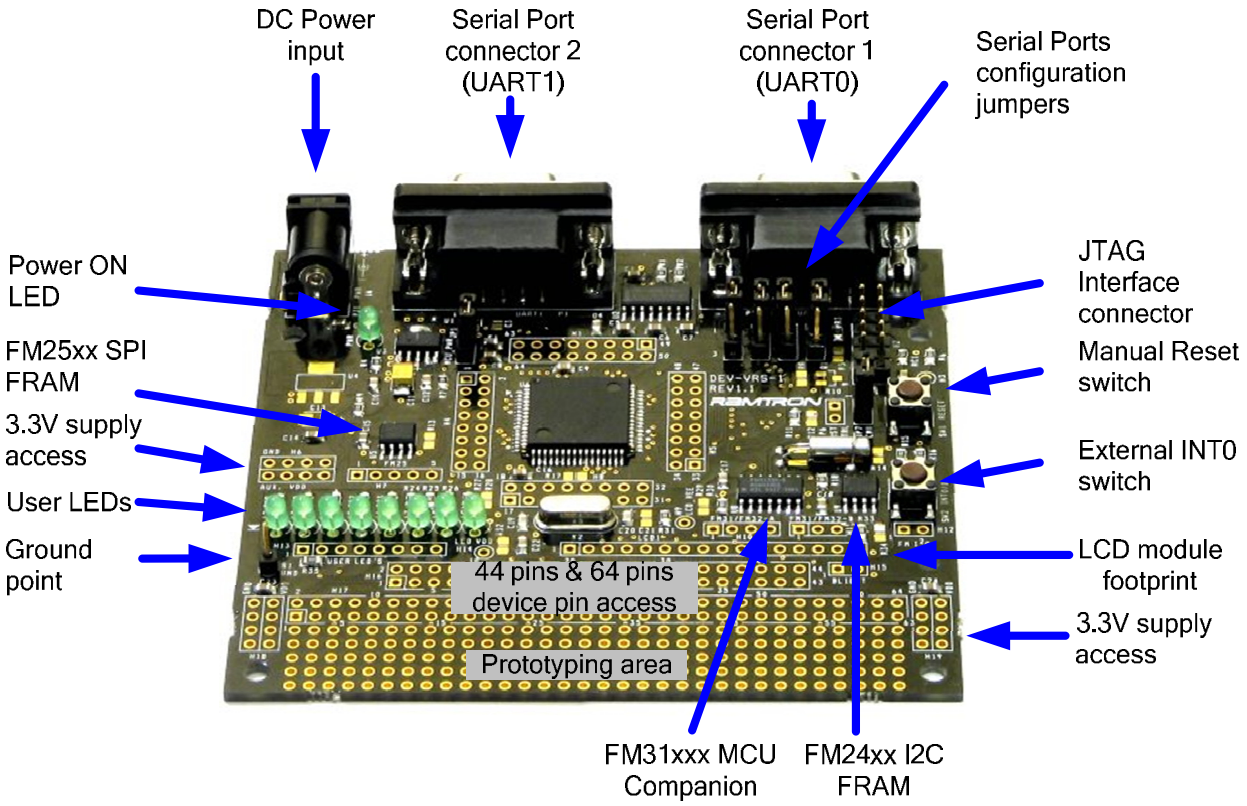


Figure 2: VersaKit-20xx Development Board

2.1 Power Supply Requirements

The VersaKit-20xx development board has the following power supply input requirements:

Voltage	6VDC to 9V
Current	200mA+
Plug Type	2.1mm Female Plug (Center positive)

The kit includes a wall-mount DC power supply adapter that complies with the above requirements. It should be plugged into Connector PJ1 (PWR).

Warning: Many commercially-available wall-mount DC power adapters exceed their output voltage rating when in low load condition. If you do not plan to use the power supply provided, please verify that the specifications on the one you choose meets the requirements above before using it with the development board.

Ensure that the input voltage supplied to the devboard PWR-IN input is always below 12 volts.

2.2 JP1 – VRS51L2070 Supply Configuration

The development board includes a 3.3V linear regulator to power the VRS51L2070 and the RS-232 transceiver. This regulator can survive polarity reversal conditions and includes a thermal shutdown feature.

To facilitate the use of the development board as a prototyping platform, we provide access to the 3.3V regulator output, as well as ground access via two 4x2 header footprints located on each side of the prototyping area. The development board also features the footprint of an auxiliary LM2937 regulator, which is powered by the DC power input and whose output is accessible on the H6 4x2 header footprint.

Heat dissipation of the regulators is done through the development board PCB. As such, the area around the regulators on the PCB may become hot when the regulators are operating. To avoid this, limit the load on the regulators to about 100mA.

Please refer to the development board schematics at the end of this document for more details about regulator configuration.

2.3 P1, P2 - RS-232 DB9 Connectors for Serial Ports

The development board includes a 2-channel RS-232 transceiver and two DB9 connectors to access the VRS51L2070's UARTs.

P1 – Provides access to VRS51L2070 UART 0
P2 – Provides access to VRS51L2070 UART 1

A set of four jumpers enables the P1 and P2 connectors to be assigned to the UARTs. A set of four headers (**JP2, JP3, JP4, JP5)** located directly below the P1 DB9 Connector configures the connection between the VRS51L2070, RS-232 transceiver and DB9 connectors P1 and P2. Several configurations are possible with different header settings, but the two configurations below are the most typical:

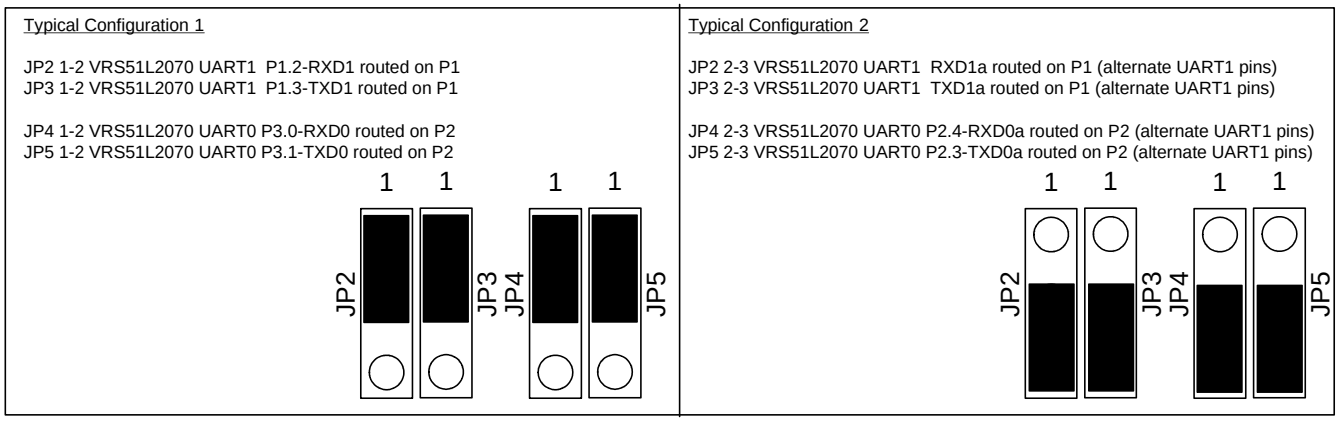


Figure 3: Typical configurations for headers and serial ports

2.4 VRS51L2070 Peripheral and I/O Access and Development Board Prototyping Area

The development board includes a set of probe points that surround the VRS51L2070. These probe points provide a direct connection to the device pins for signal probing.

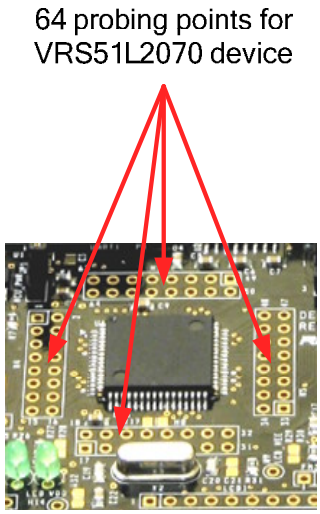


Figure 4: Probing points around the VRS51L2070-40-Q

Access to the device I/Os is also possible through two header footprints organized as follows:

The H17 header footprint provides access to the VRS51L2070 pins. Pin assignment on the H17 Header directly corresponds to the VRS51L2070 pin-out.

If the VRS51L2170 is installed on the PCB, Header H16 provides a direct connection to the 44-pin device and the H16 Header pin assignment directly corresponds to the device pin-out.

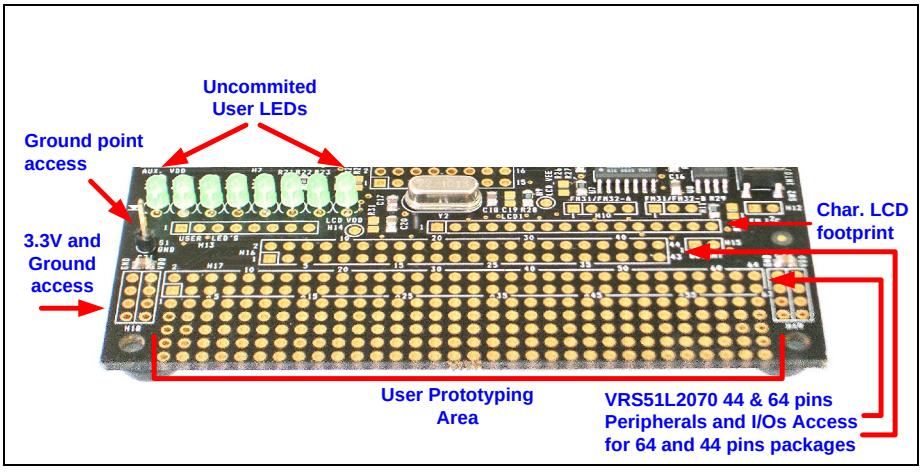


Figure 5: Prototyping area and access to VRS51L2070 I/O and peripherals pins

2.4.1 Probe headers for peripheral and I/O access around the VRS51L2070 QFP-64

The following figure shows the pin connections of the header footprints located around VRS51L2070-40-Q on the development board:

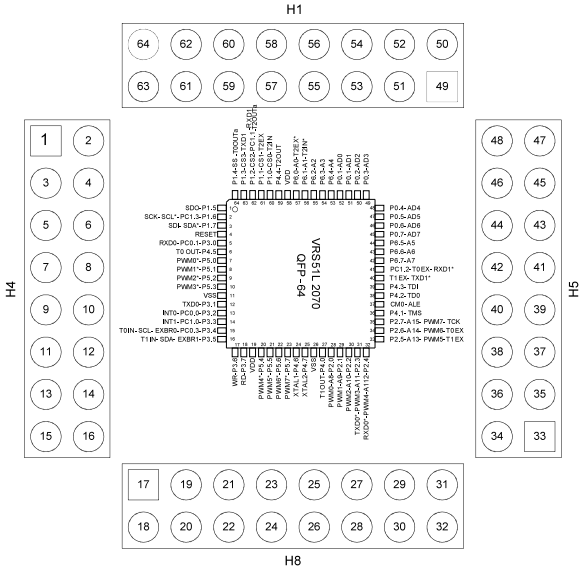


Figure 6: Probing vias around the VRS51L2070

2.4.2 Header Footprints for VRS51L2070 QFP-64 Peripherals and I/O access

To access the VRS51L2070 I/Os and peripherals, the development board provides a 64-pin header footprint near the prototyping area. This header footprint provides access to all the pins on the chip. The diagram below shows the header footprint pin-out.

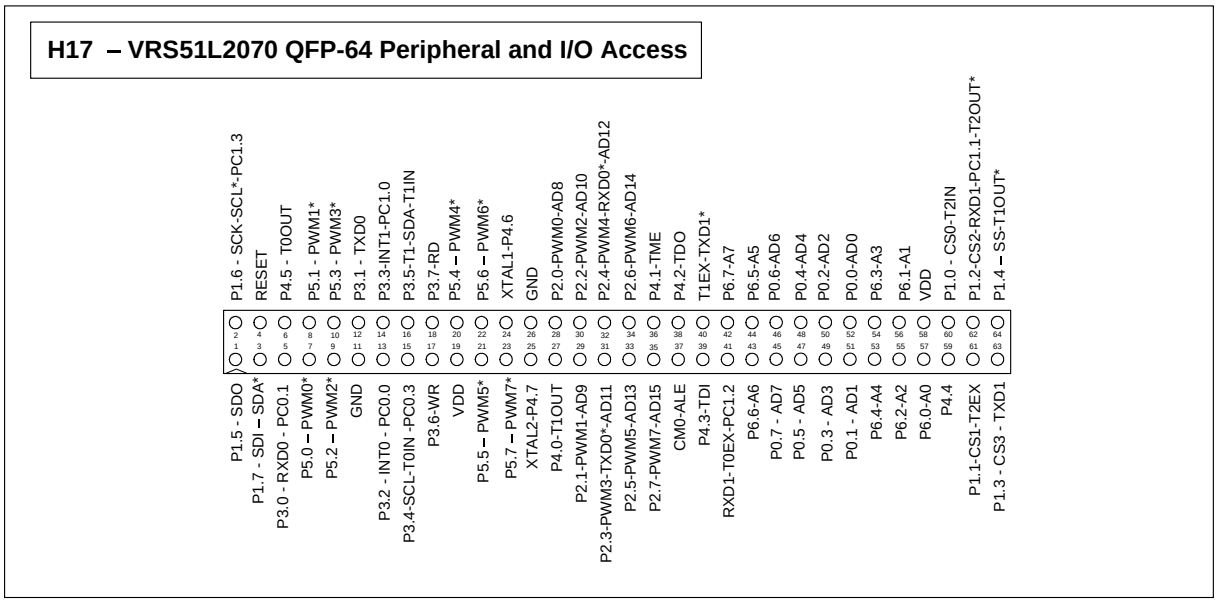


Figure 7: Pin description of H17 I/O and peripheral access

2.4.3 Probe headers for peripherals and I/O access around the VRS51L2170 QFP-44

The following figure shows the pin connections of the header footprints located around VRS51L2170 QFP-44 on the development board:

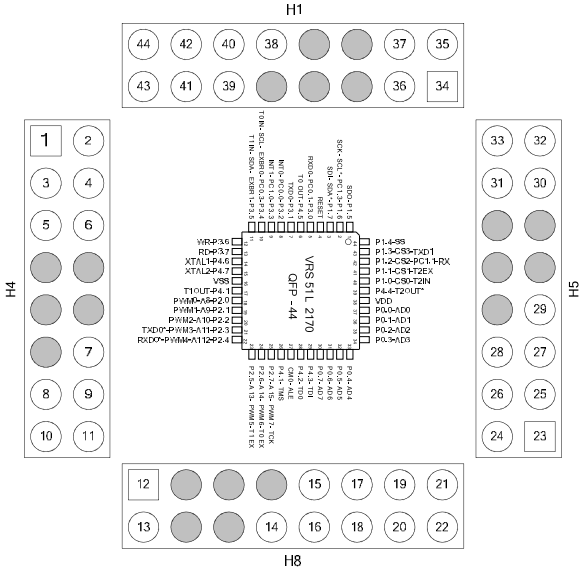


Figure 8: Probing vias around the VRS51L2170

2.4.4 Header Footprints for VRS51L2170 QFP-44 Peripheral and I/O Access

To access the VRS51L2170 QFP-44 I/Os and peripherals, the development board provides a 44-pin header footprint near the prototyping area. This header footprint provides access to all the pins on the chip. The diagram below shows the header footprints pin-out.

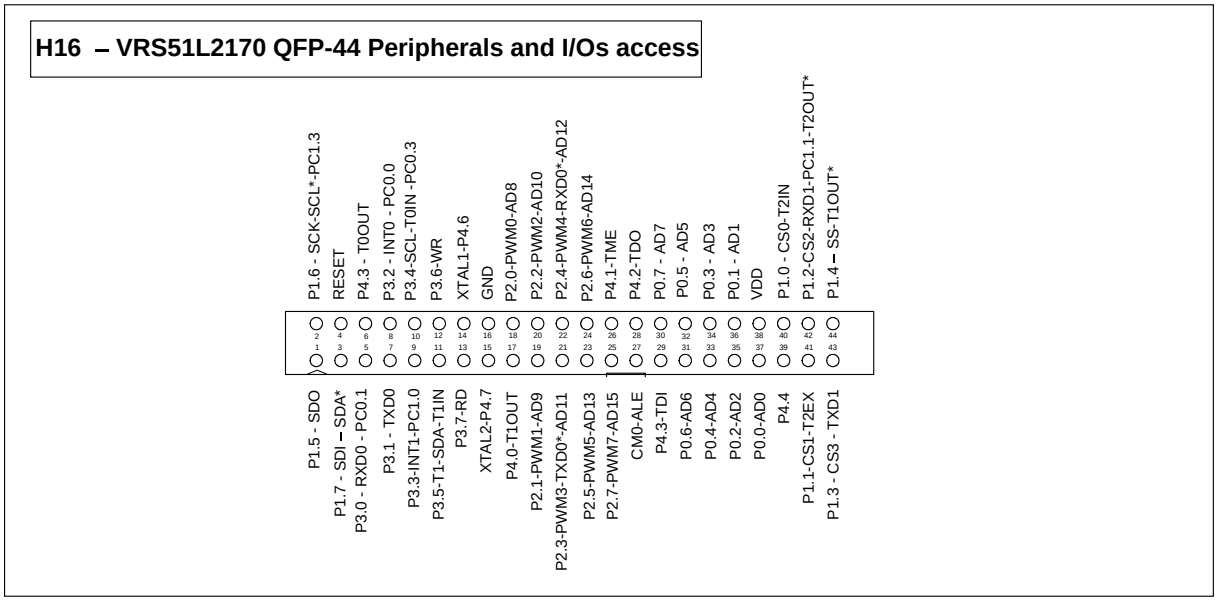


Figure 9: Pin description of H21 access to VRS51L2170 QFP-44 peripherals

Ground Points on the Development Board

The VersaKit-20xx development board provides a ground access point (S1) located above the H18 header on the right side of the PCB. This point can be used to connect measurement instruments to ground.

2.5 Tact Switches

The development board includes two tact switches:

- **SW1** – VRS51L2070 Reset Switch. This switch allows a manual reset of the VRS51L2070 device. The VRS51L2070 reset is active low.

  Note: During programming or in-circuit debugging of the VRS51L2070, do not press SW1. Doing so could disturb the synchronization between the Versa Ware JTAG software and VRS51L2070 debugger.

- **SW2** – VRS51L2070 Interrupt Switch. This switch allows users to manually send a low pulse to the device's INT0 pin. A connection can be established from the SW2 to the VRS51L2070 INT1 pin by installing a 0Ω resistor at position R28 and removing the 0Ω resistor from R27.

2.6 User LEDs

The development board includes a set of eight uncommitted, 3mm, green user LEDs. The anode of each LED is connected to the board's VCCMCU supply line through a 680R current limiting resistor, while the cathode of each LED is connected to the user LED's H13 header footprint.

2.7 Character LCD module header footprint

The development board features a header footprint (LCD1) for easy installation of a character LCD module. When installed, the character LCD module header footprint and the VRS51L2070 are configured as follows:

LCD	Connected to
LCD Data [7:4]	P0 [7:4]
LCD Data [3:0]	Not connected
LCD E	P0.2
LCD RW	P0.1
LCD RS	P0.0
LCD VEE	Accessible through H9

Most character LCD modules require a 5V supply. The LCD supply is accessed through H14. If the LCD module operates from 3.3V, a 0Ω resistor can be installed at position R31 to connect the LCD module supply and the devboard supply.

The LCD drive pin (VEE) is accessible through H9. The LCD driving voltage that must be applied on the VEE pin of the LCD module depend on the LCD type and varies among different manufacturers. Please consult the specific LCD manufacturer's module datasheet to establish the proper voltage to apply to the LCD VEE line. For your convenience, we have included an unpopulated 0805 resistor footprint between the H9 and the LCD VEE pin as well as a 0805 capacitor footprint between the LCD VEE pin and the development board ground.

The LCD module backlight pins are accessible via the H15 2x1 header footprint

2.8 Onboard FM24C64 I2C FRAM, FM25CL64 SPI FRAM and FM31256 MCU Companion

A 64KB I²C 5V FRAM device (FM24CL64) is included with the development board at position U8. The SCL and SDA lines of FM24C64 are connected to the H12 2x1 header footprint.

The development board also features a FM31256 processor companion at position U8 featuring 256KB of FRAM memory, a real-time clock, a watchdog timer, an event counter and power fail monitoring circuitry. A 32 kHz crystal required for driving the FM31256's RTC is also included on the PCB.

Two 2KΩ pull-up resistors, R15 and R16, are connected between the 3.3V supply and the SDA and SCL lines, respectively. Two header footprints are provided for accessing the FM3164 I/Os. The FM3164's I²C communications interface is connected to H12.

Finally, an FM25CL64 SPI-based FRAM is also installed on the devboard at position U5. The device communication interface I/Os are accessible through the H7 header footprint.

3 Development Kit Setup for VRS51L2070 Evaluation

3.1 VersaKit-20xx Hardware Setup

The VRS51L2070 includes a Versa-JTAG programming/debugging interface port, accessed via the 5x2 header at position H2 (JTAG). To evaluate the VRS51L2070, the VersaKit-20xx includes a parallel port based JTAG device that interfaces with Ramtron's Versa Ware JTAG Windows®-based programming/debugging software.

Figure 10: Versa-JTAG interface for programming and debugging the VRS51L2070

3.1.1 Hardware Setup and Jumper Configuration for VRS51L2070 Evaluation

To program the VRS51L2070, connect the JTAG interface to the H2 Connector and connect the parallel cable to the PC's parallel port. Then connect the power adapter to the development system power connector located at PJ1. PWR (L1) will turn ON.

Figure 11: Connecting the Versa-JTAG programming interface and the development board supply

3.2 Versa Ware JTAG Software Overview

Versa Ware JTAG is a Windows®-based software tool that provides a friendly development platform for all Ramtron microcontrollers featuring a JTAG interface (the VRS51L2xxx and future derivatives).

The Versa Ware JTAG Software is composed of two parts:

- **Versa Ware JTAG Programmer**

  The Versa Ware JTAG Programmer provides an easy-to-use interface with which to perform operations such as erase, program, read, etc., on the target device's Flash memory.

- **Versa Ware JTAG Debugger**

  The Versa Ware JTAG Debugger is a user interface that links the in-circuit debugger and the source code. All Ramtron MCUs with a JTAG interface include an integrated debugger that enables in-application debugging of the device via its JTAG interface.

3.2.1 Installing the Versa Ware JTAG Software

The Versa Ware JTAG software can be downloaded from the Ramtron web site at www.ramtron.com. After downloading the software, launch it by double-clicking the following icon:

Versa_Ware_JTAG_20_SETUP.exe

This will initiate the Versa Ware JTAG setup program (see below):

Figure 12: Versa Ware JTAG setup screen

Follow the instructions to complete the Versa Ware JTAG installation.

3.2.2 Running the Versa Ware JTAG Programmer

Once the software is installed, it can be run directly from the setup program, or by clicking on the Versa Ware JTAG shortcut created during the installation process.

Upon startup, the software will attempt connecting to the Versa-JTAG interface.

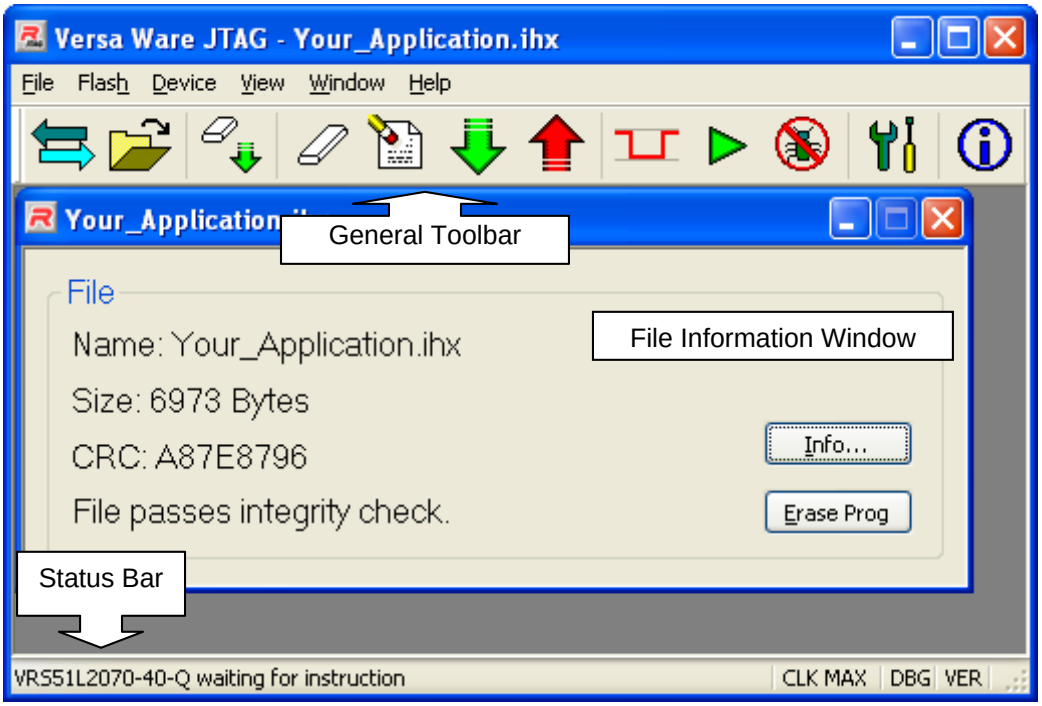


Figure 13: Versa Ware JTAG setup screen

Most of the functions provided by the Versa Ware JTAG software are accessible through the action toolbar.

To download a HEX file into the VRS51L2070, follow the instructions:

1. Make sure that the Versa-JTAG interface is properly installed in the H2 header and the power supply is connected to the development board.
2. Click on the Synchronize button. The status bar should show: “VRS51L2070-40-Q waiting for instruction”.
3. Click on Open to select the HEX file to be programmed into the VRS51L2070.
4. Click on Erase then Program to erase and program the Flash. By default, after this process is complete, the program will start.

The Synchronize button can also be used to halt execution of the VRS51L2070 program and put the device into program mode. The Run button restarts program execution.

Via the Options button, the user can configure the programming option, set the Flash security options, and activate the in-circuit debugger.

3.2.3 Running the Versa Ware JTAG Debugger

Once the program is loaded into the VRS51L2070 Flash memory and the debugger is enabled, activate the debugger by clicking on the Debugger button.

The following window shows the in-circuit debugger in action when the source code IRAM, SFR page 0, and watch lists windows are open and the program is at a breakpoint.

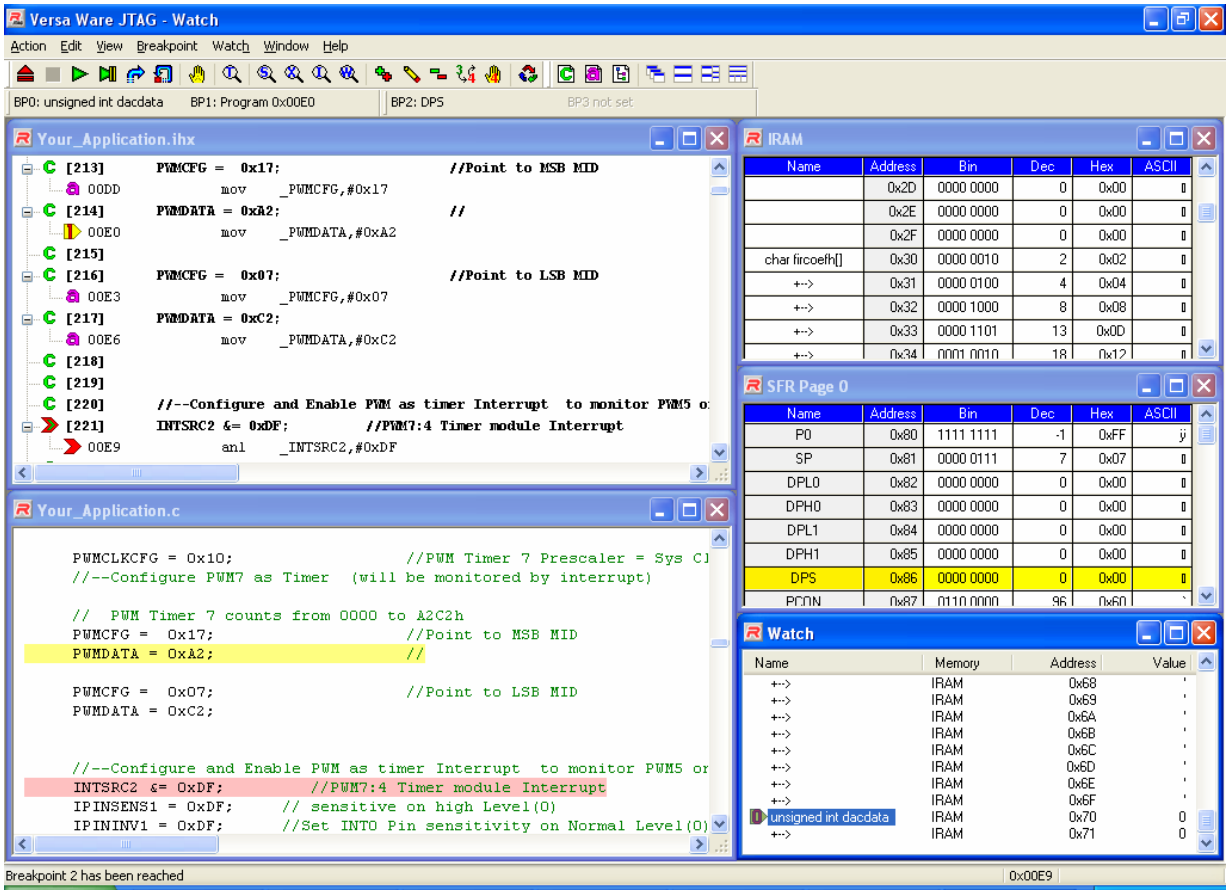


Figure 144: Versa Ware JTAG debugger window

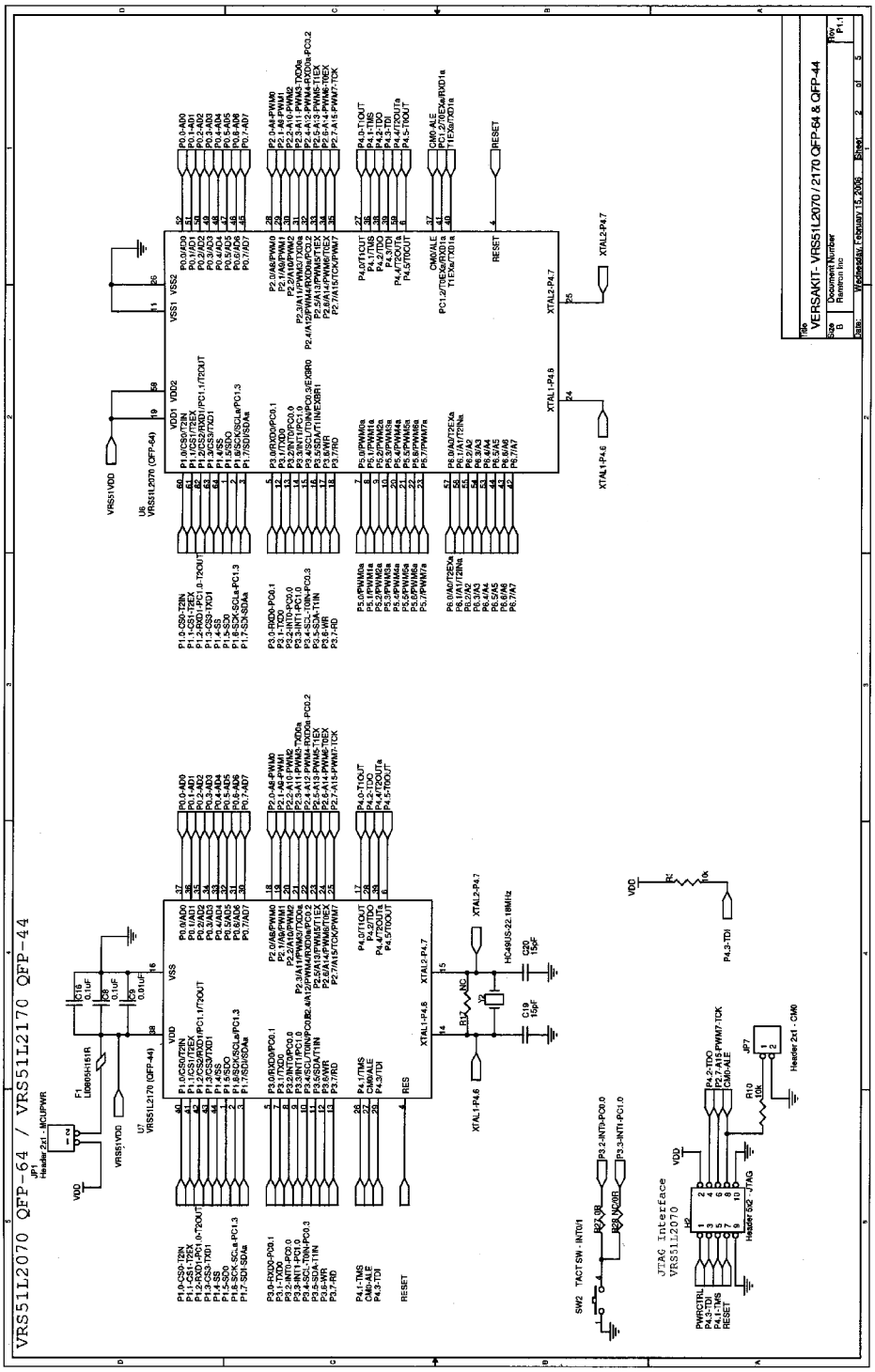
The following table summarizes the Versa Ware JTAG Debugger commands. Please consult the Versa Ware JTAG Software User Guide for a detailed description of software features.

Command	Toolbar	Toolbar button	Menu	Keyboard Shortcut
Run	Debugger		Action	F7
Step	Debugger		Action	F6
Halt	Debugger		Action	Ctrl + Backspace
Restart	Debugger		Action	
Jump	Debugger		Action	
Stop Debugging	Debugger		Action	
Copy			Edit	Ctrl + C
Find			Edit	Ctrl + F
Find next			Edit	F3
Go to			Edit	
Refresh	Debugger		View	Ctrl + R
View SFR	Debugger		View	Ctrl + Shift/Alt + S
View IRAM	Debugger		View	Ctrl + Shift/Alt + I
View XRAM	Debugger		View	Ctrl + Shift/Alt + X
View Program Trace	Debugger		View	Ctrl + Shift + T
View Watch	Debugger		View	Ctrl + Shift + W
View C files	View		View	
View Assembler files	View		View	
View Address Tree	View		View	Ctrl + Shift + S
View Toolbars			View	
View Options			View	Ctrl + Shift + V
Toggle Breakpoint 0			Breakpoint	Ctrl + B
Toggle Breakpoint 1 - 5			Breakpoint	Ctrl + F1 to Ctrl + F5
Breakpoint Settings	Debugger		Breakpoint	Ctrl + Shift + B
Add Watch	Debugger		Watch	
Edit Watch	Debugger		Watch	
Force Watch	Debugger		Watch	
Remove Watch	Debugger		Watch	
Break on Value	Debugger		Watch	
Disable Value Breakpoint			Watch	
Cascade	View		Window	
Tile	View		Window	
60:40 Horizontal	View		Window	
75:25 Vertical	View		Window	
About			Help	
Erase then Program	Program		Flash	F5
Erase Page	Program		Flash	
Read Flash	Program		Flash	

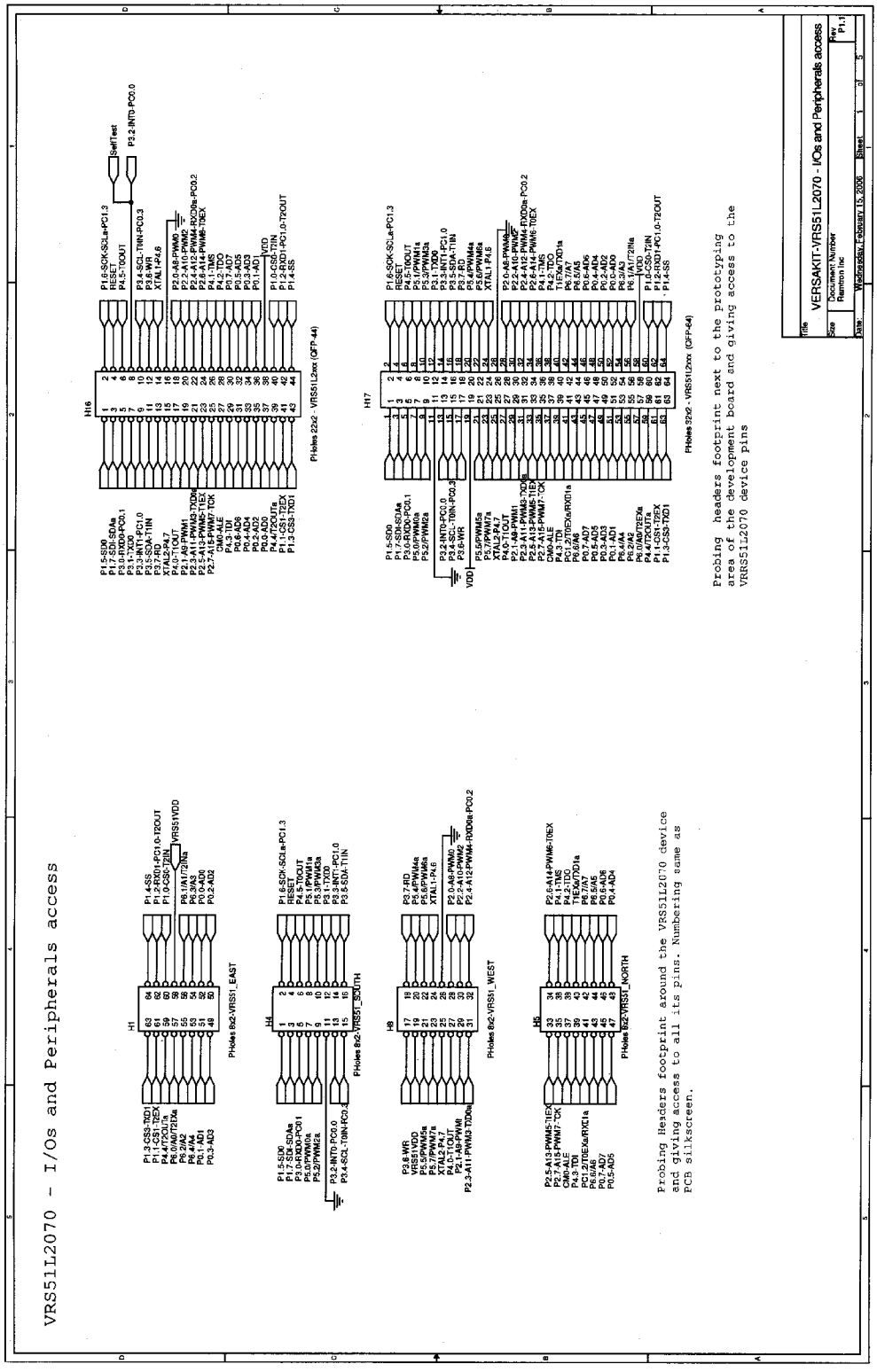
Table 1: Debugger command set

4 VersaKit-20xx Development Board Schematics

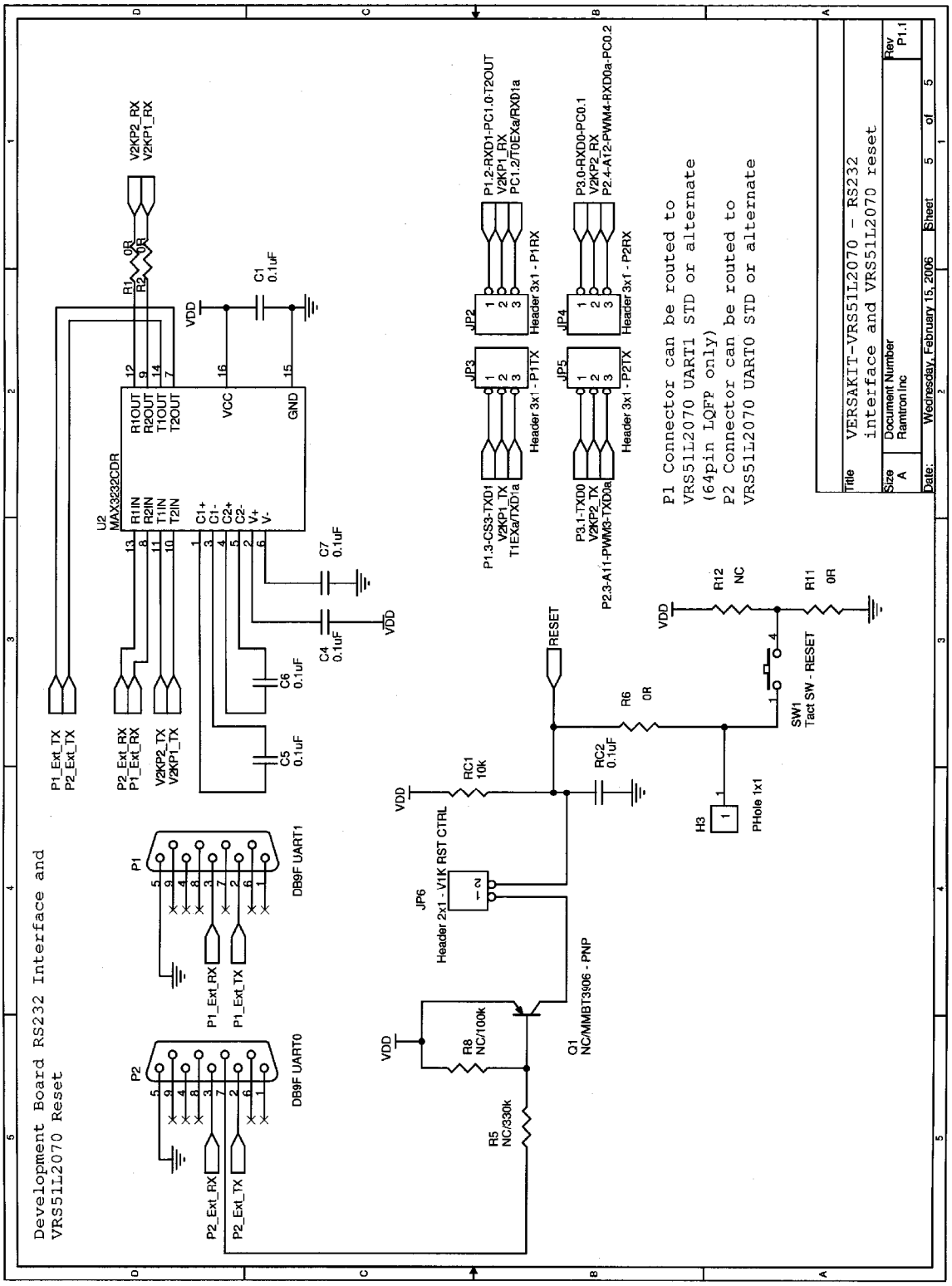
4.1 VRS51L2070



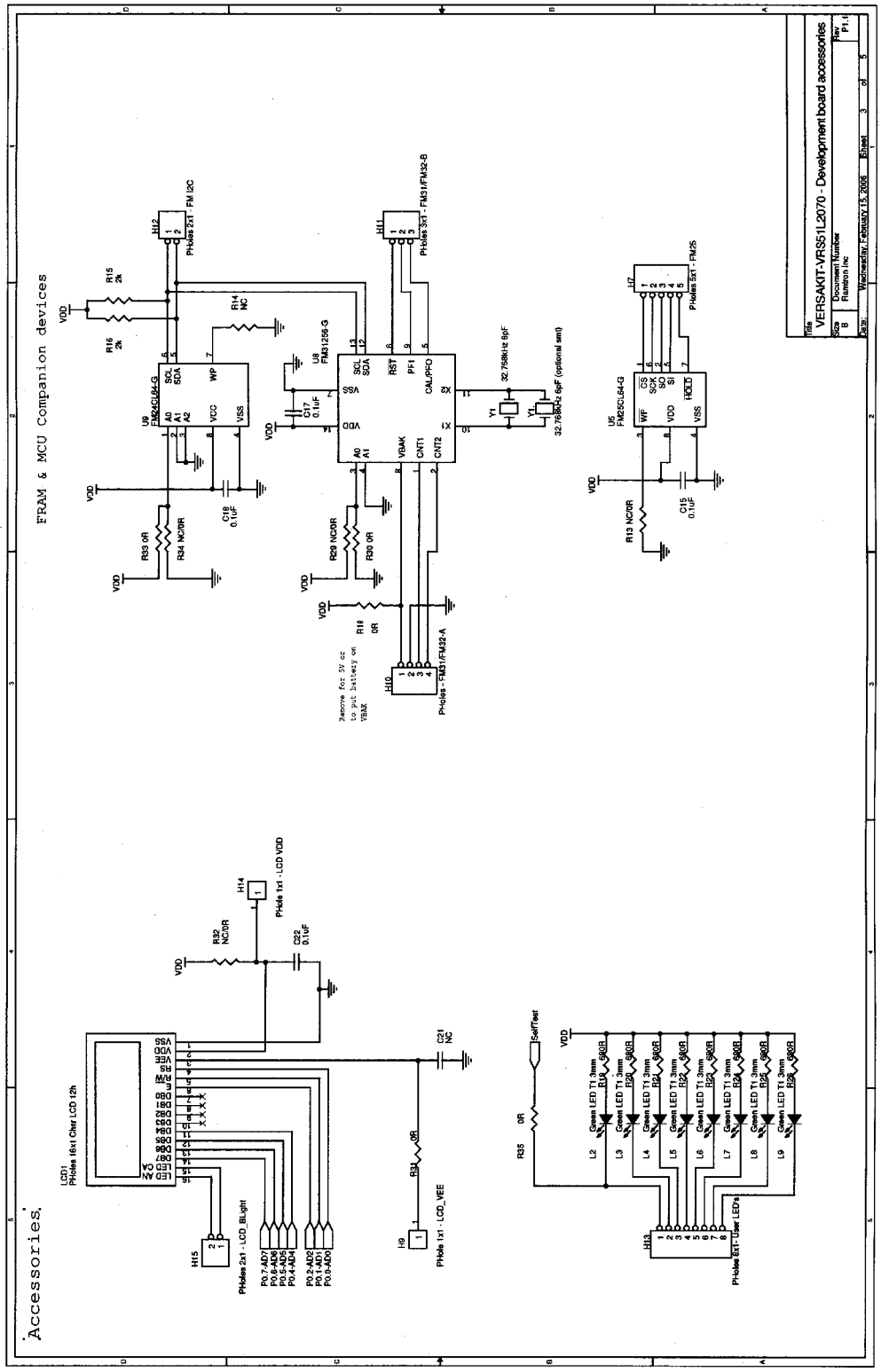
4.2 VRS51L2070 Peripheral Access



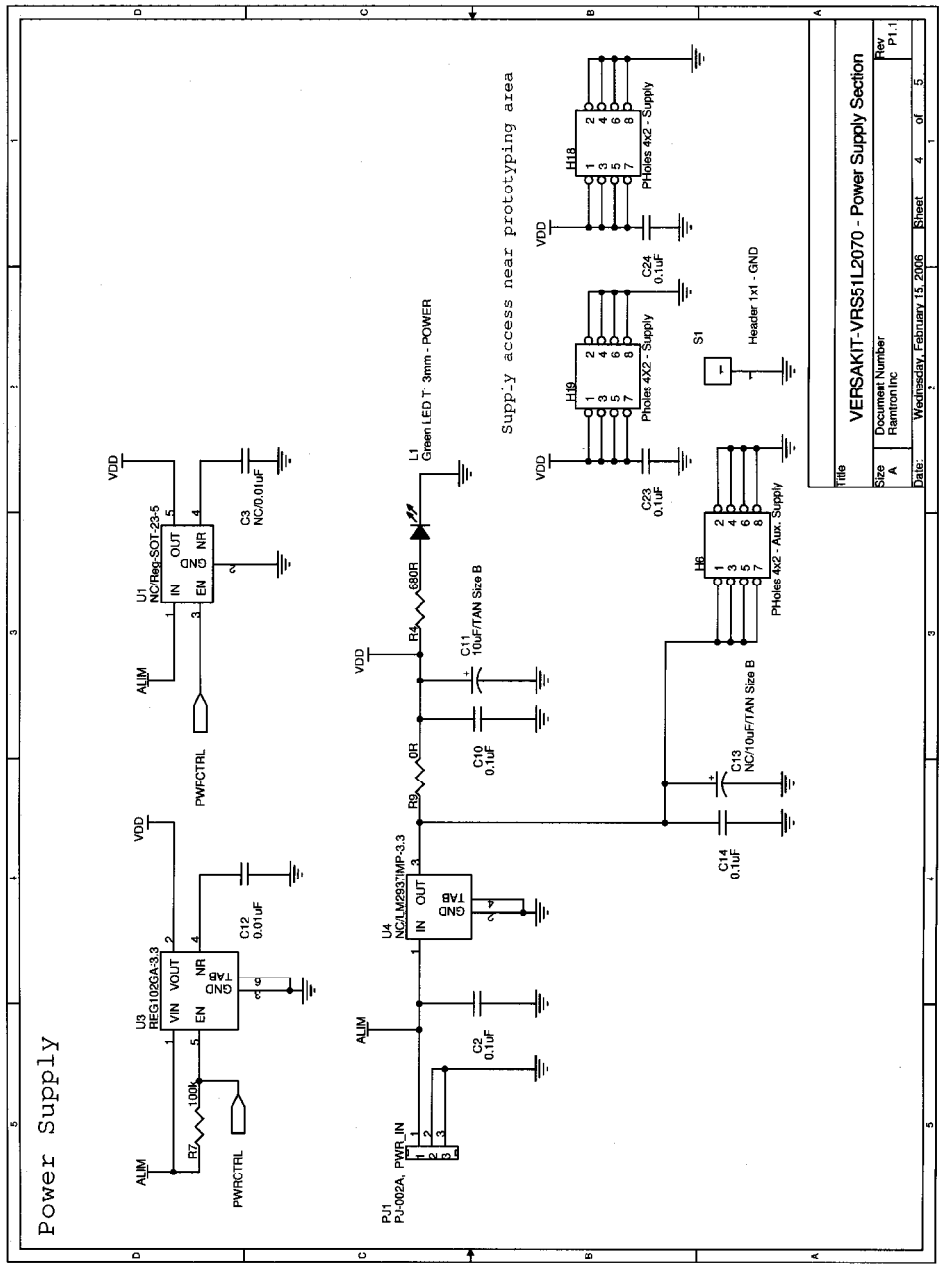
4.3 UART Transceiver and Reset



4.4 Accessories



4.5 Power Supply



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