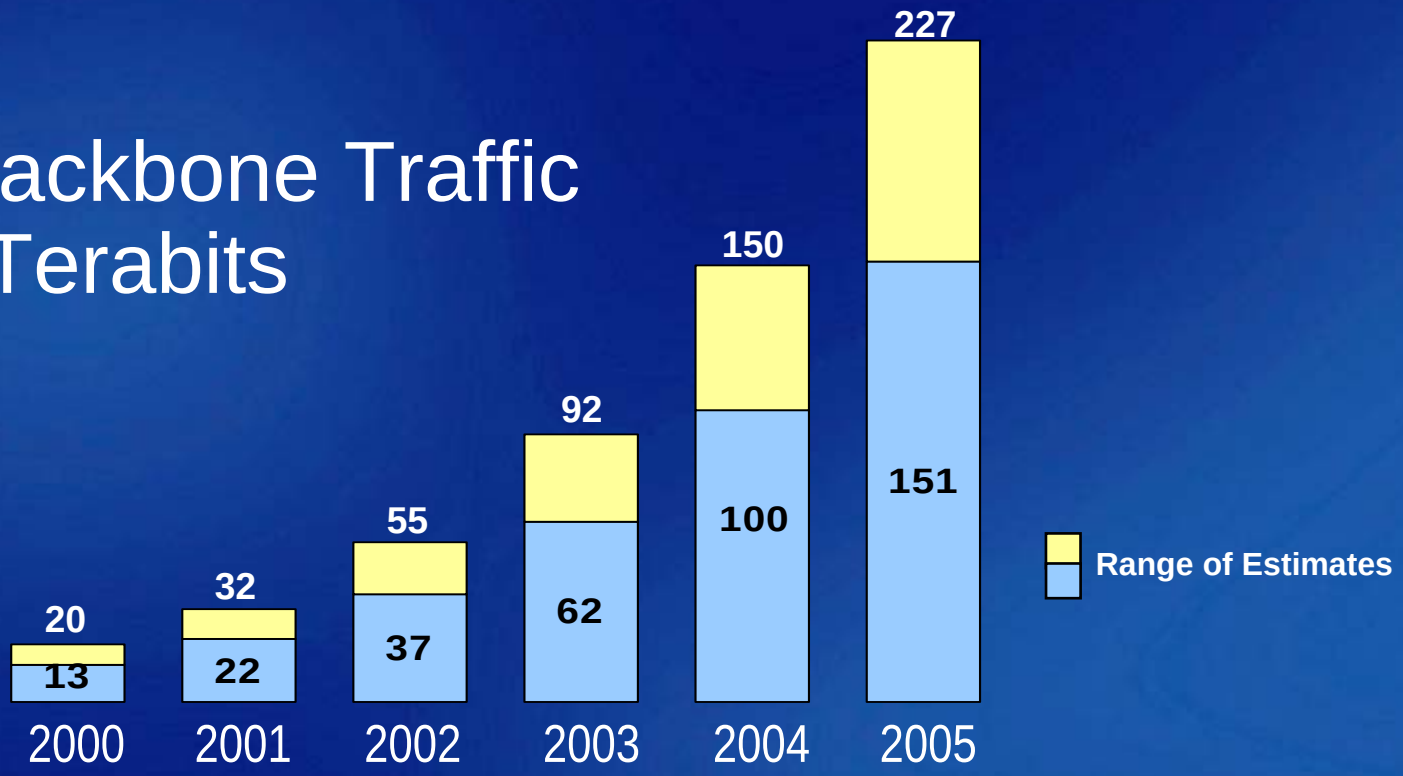
Solving the Connectivity Challenge

Traffic Demand Remains Healthy



- Carriers are finding innovative ways to address traffic demand such as reusing and redeploying systems and rerouting traffic
- Challenge for equipment suppliers and IC suppliers is to deliver flexibility

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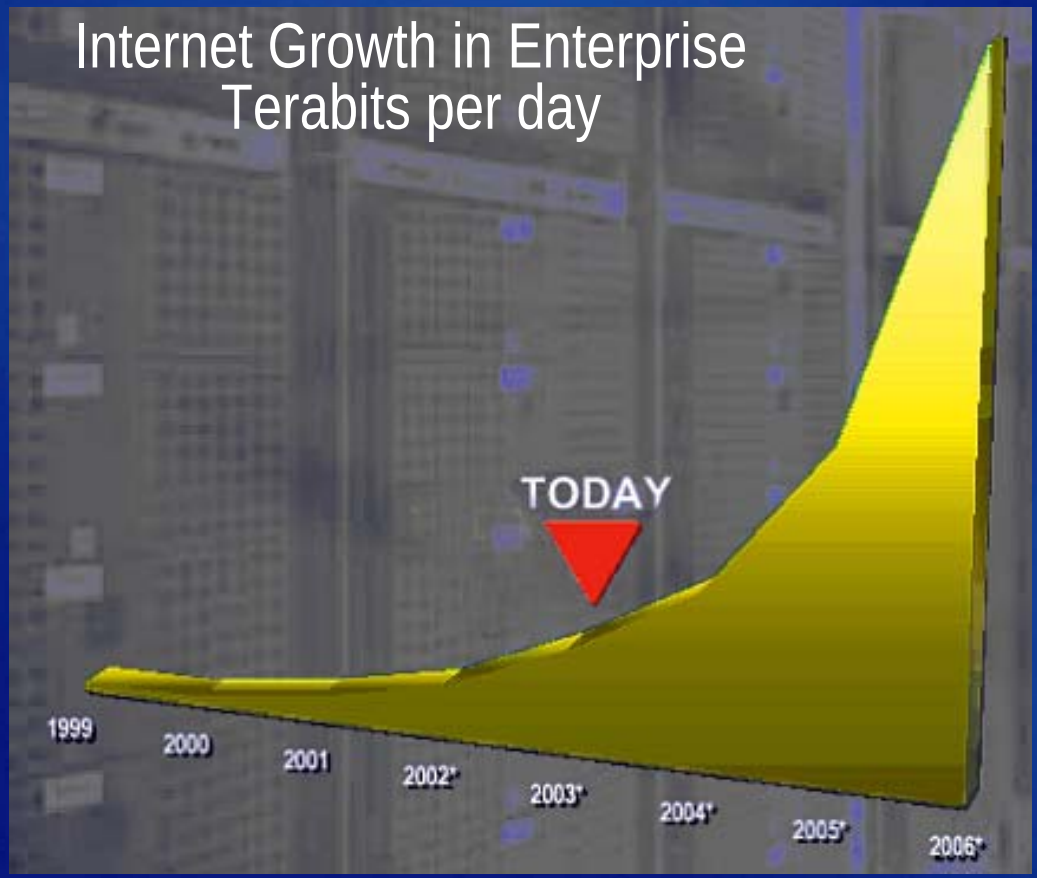
Source: Goldman Sachs Research, McKinsey.

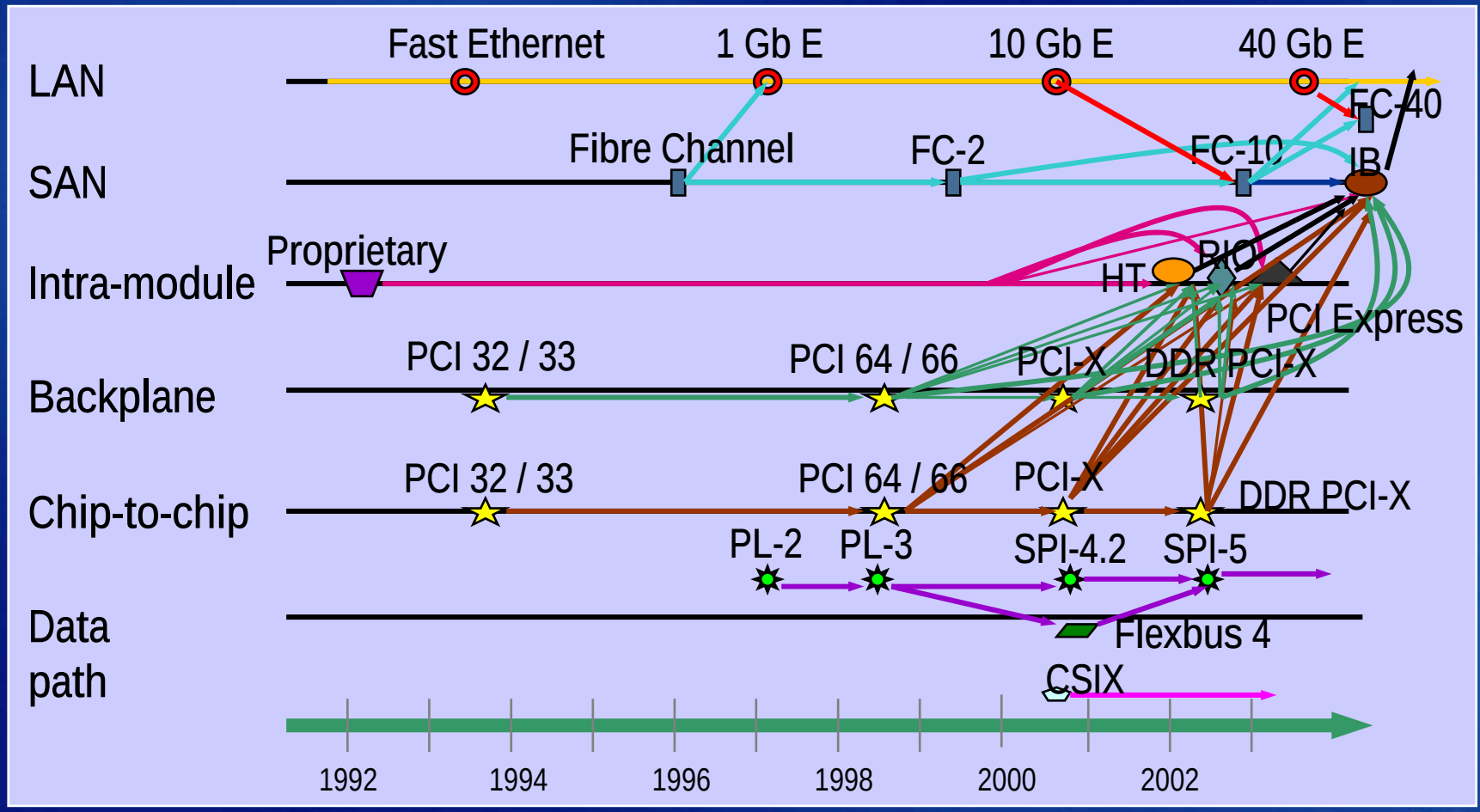
Industry 10 Gbps Deployment



- Driven by insatiable demand for data, voice and video
  - Wireless web, video conferencing, camera cell phones, NetMeeting, IP phone
- A sum of all parts:
  - Cost, power, density, reach
- 10 Gbps systems offer the best performance at the lowest cost per bit!

Source: IDC 2002 & Intel Market Analysis

Explosion of New Connectivity Standards



A typical Terabit System uses 2 or more interfaces at the same time!

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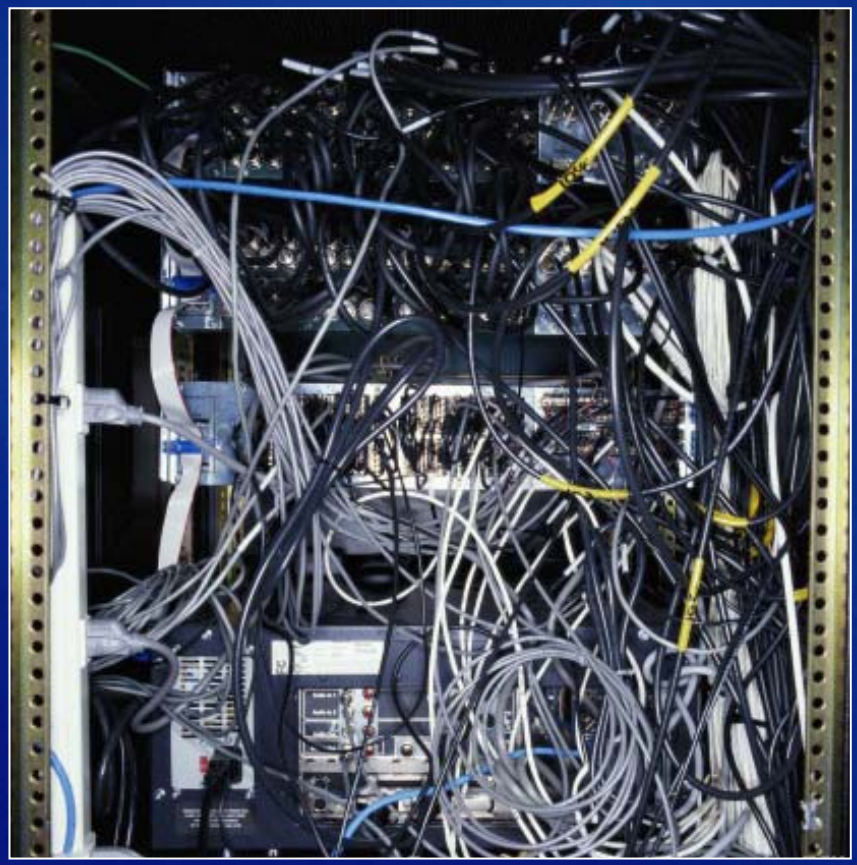
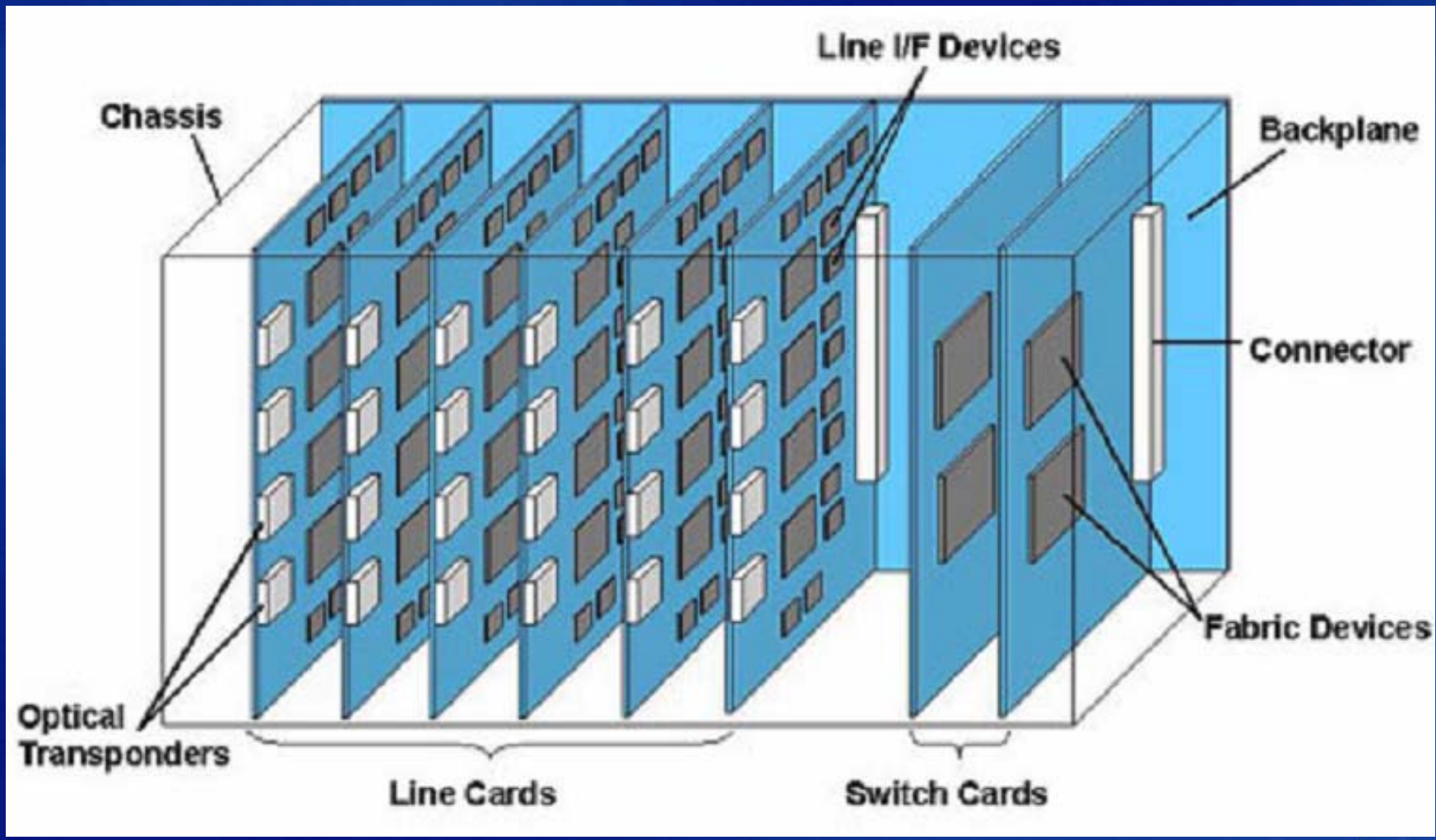
The Edge is a Mess…



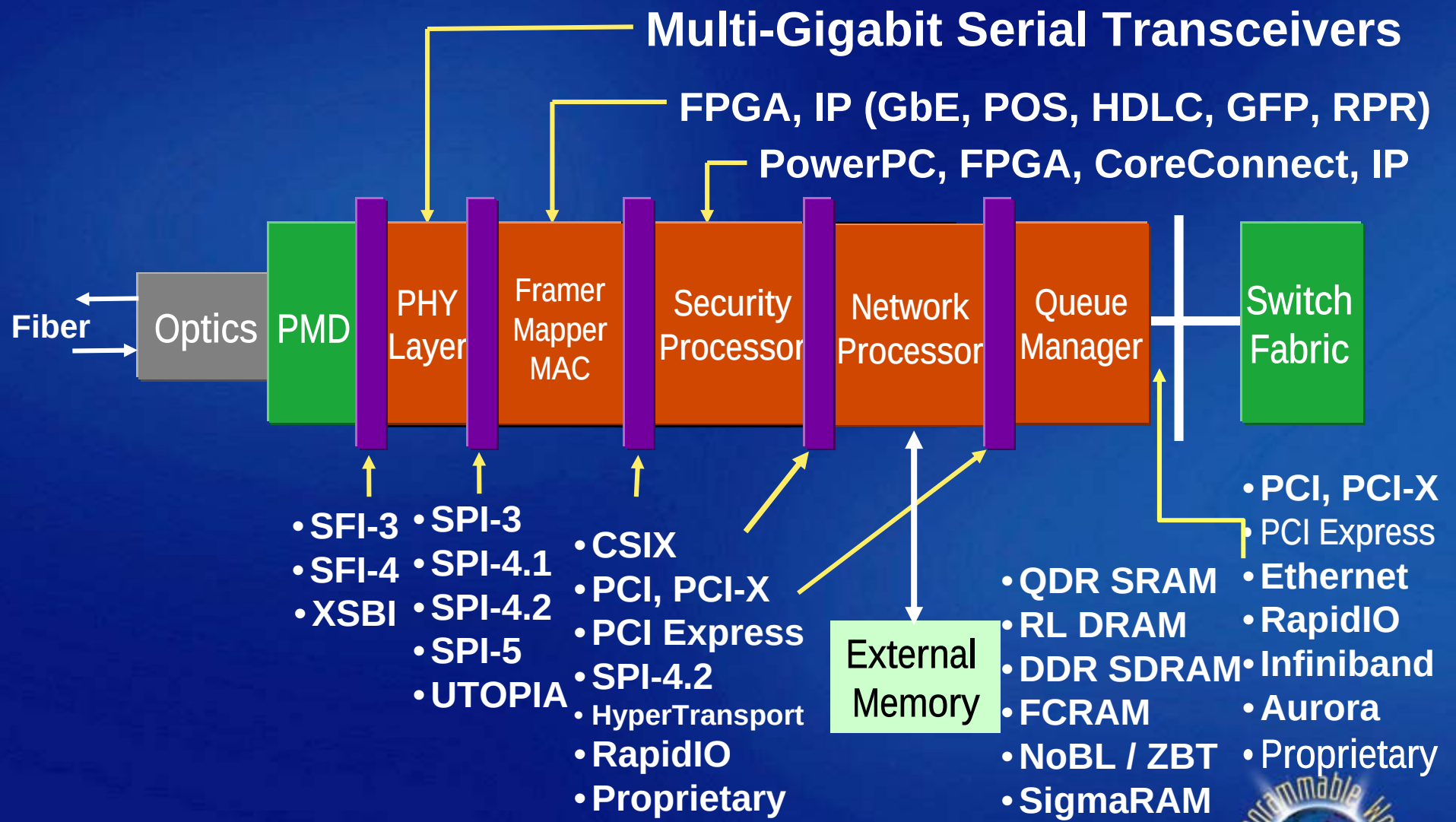
Actual Rack in Carrier POP

- Different physical routers dedicated to different users and services
- Intra-POP connectivity nightmare
- Complex standards and protocols
- Space, power, cooling are at a premium

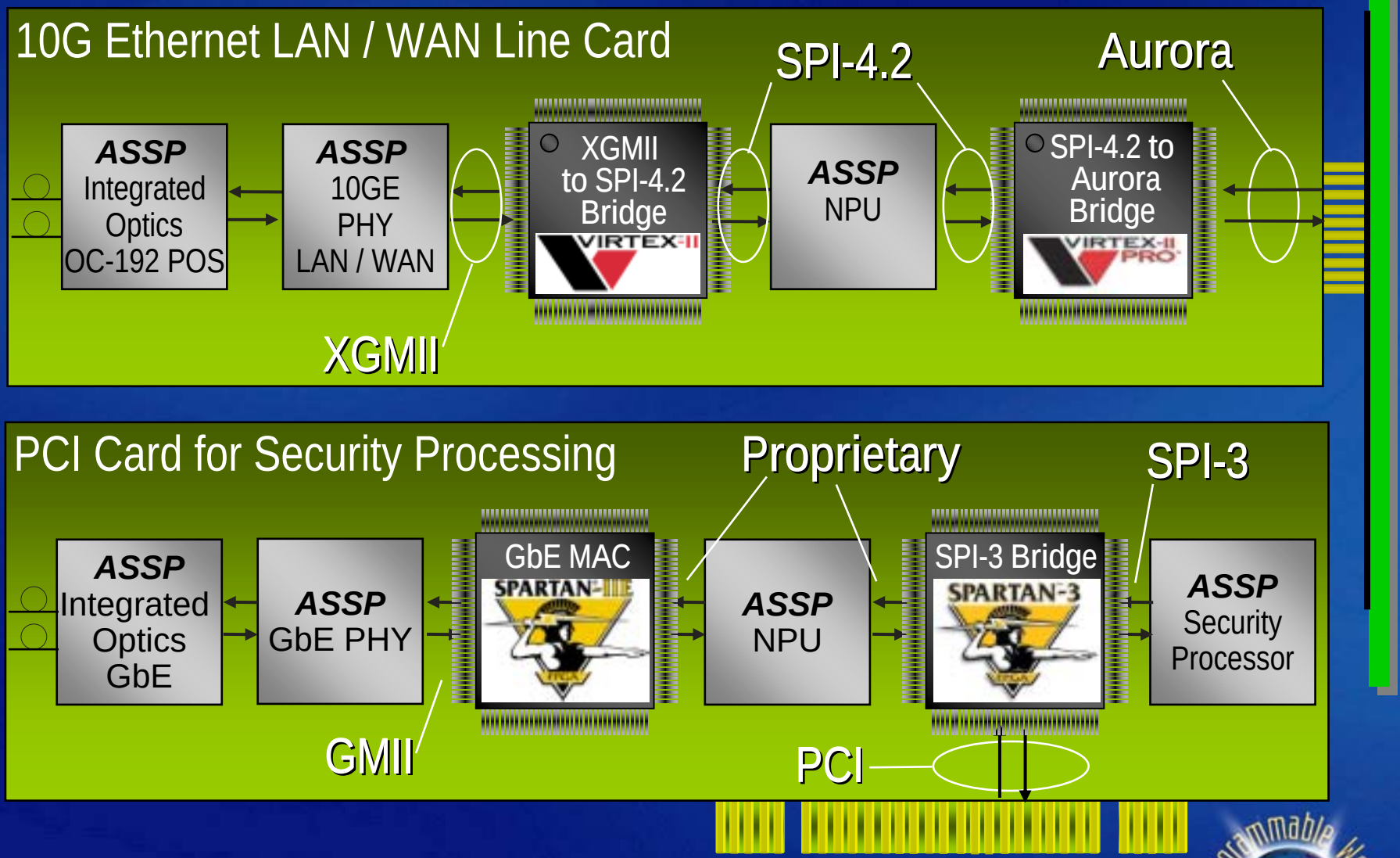
Typical Networking System



Protocol Interfaces

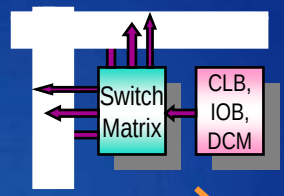


Diverse Component Mix

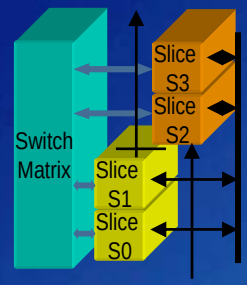


Connectivity Needs Powerful Platform FPGA Features

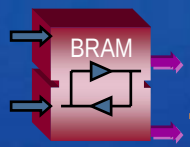
Active Interconnect™
Fast, predictable routing delays

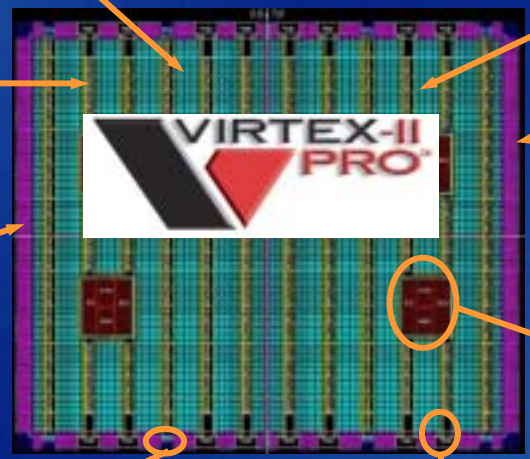


Powerful CLB
>300 MHz Performance

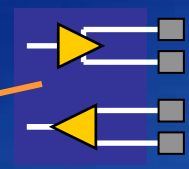


Dual-Port RAM
Fast & efficient logic;
Highest flexibility





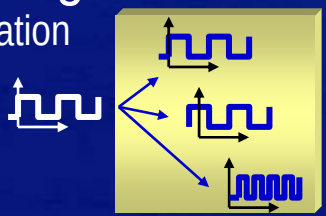
Programmable I/Os
840 Mbps LVDS
644 Mbps SDR



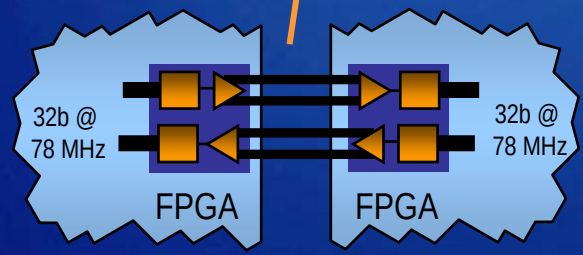
On-chip termination
Reduced lay-out complexity

EmbeddedPowerPC
300 MHz; 420 DMIPS

Digital Clock Managers
Precise frequency generation and phase control



Multi-Gigabit Serial Transceivers
Up to (24) 3.125 Gbps transceivers



XILINX®

Lowest Cost Parallel Interconnect Solutions

- PCI 32/33 effective cost as low as $0.75*
- Physical interfaces and system elements
  - 25 I/O standards, DDR I/O registers, DCMs
- Pre-engineered solution
  - Drop-in functionality
  - Pre-verified and fully compliant

PCI 32/33 and PCI 64/33

Real-PCI™

SPI-3 (POS-PHY Level 3)

SPI-4.2 “Lite” (2.5Gbps)

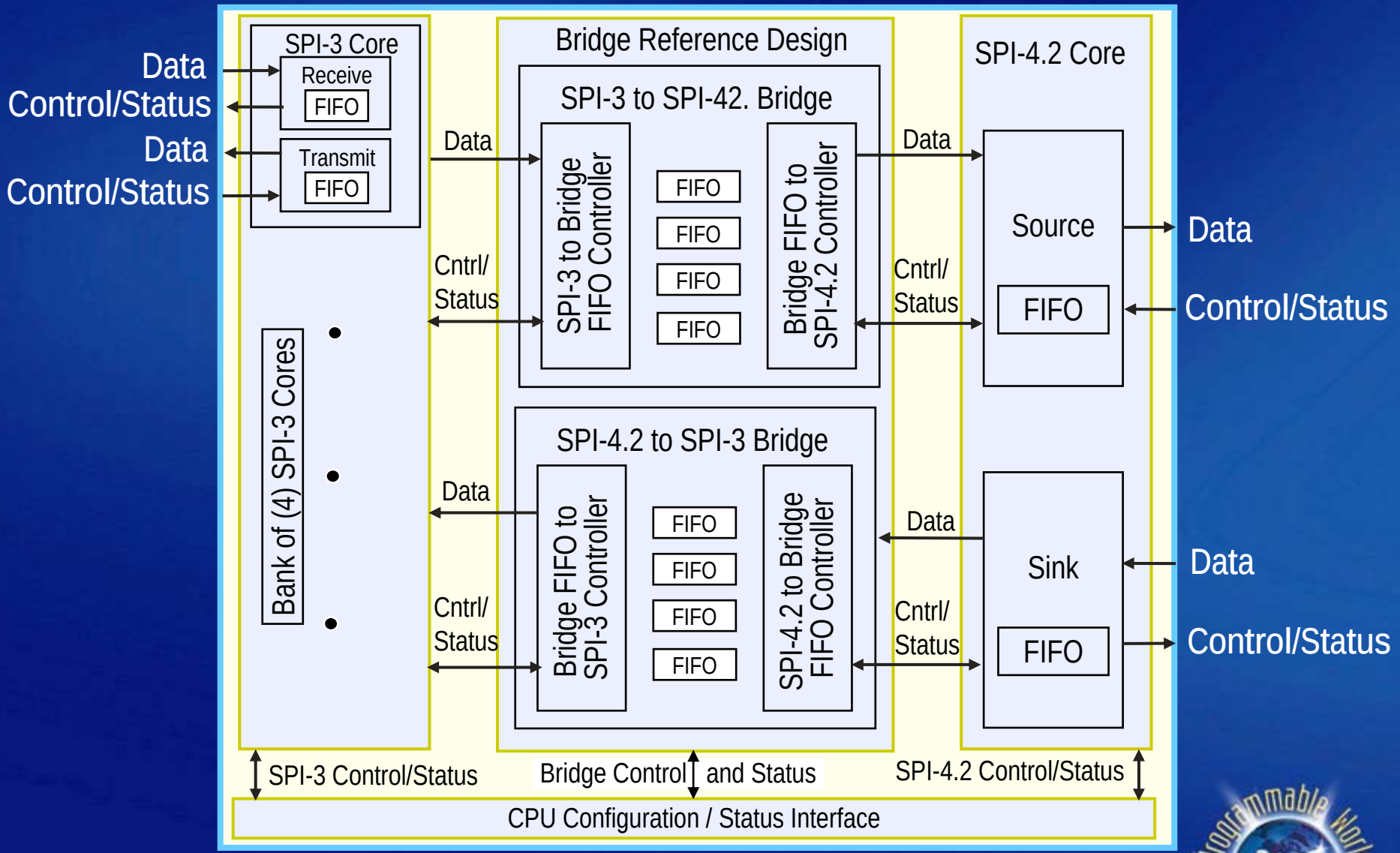
XILINX®

* Based on pricing for 2004, 250K units

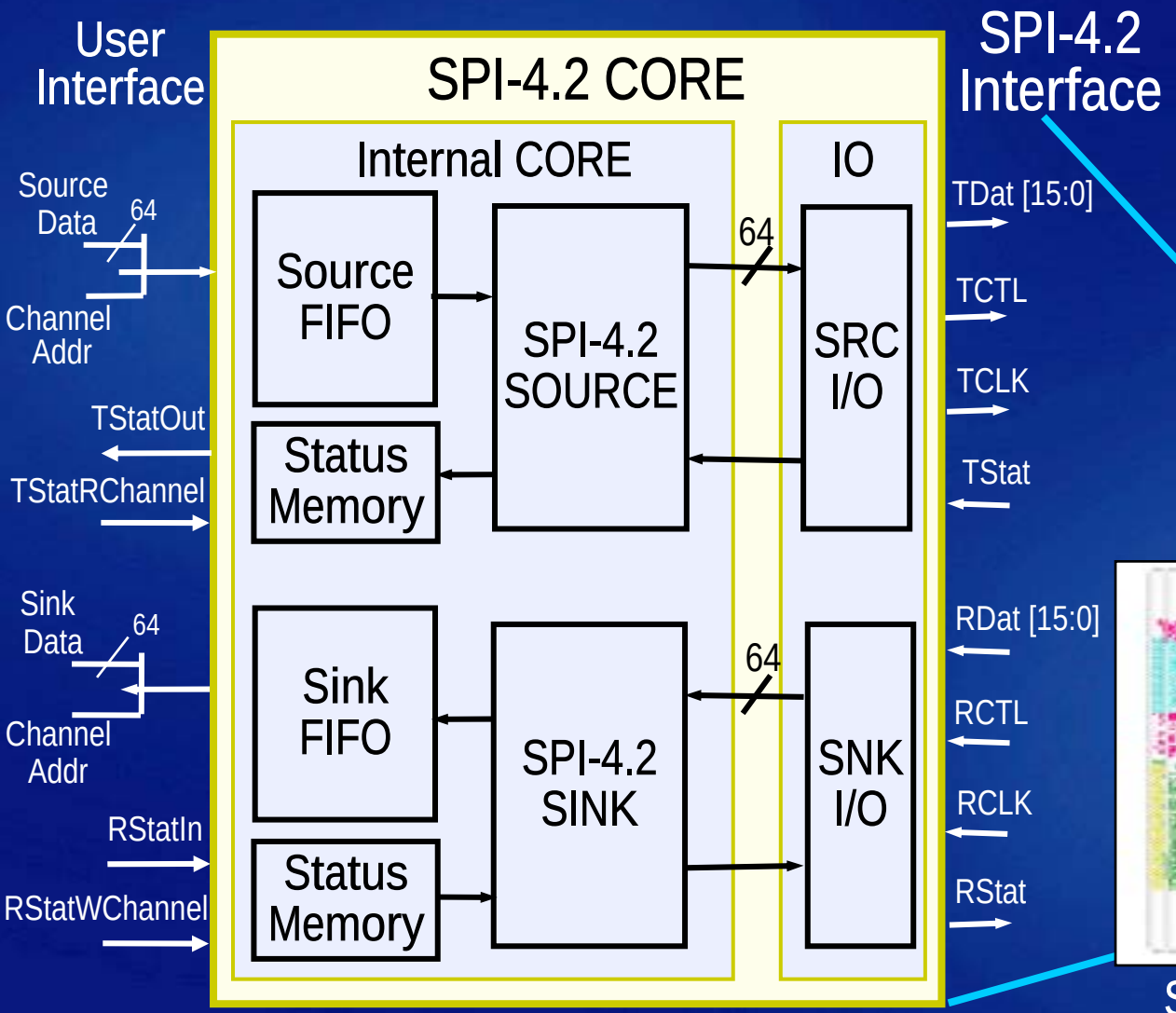
Bridging Case Studies

- Framer Aggregation
  - Quad SPI-3 to SPI-4.2
- Backplane Fabric Interface
  - SPI-4.2 to AURORA including NPU example
- Reconfigurable Computing Switch Fabric Network
  - Systran Federal Reconfigurable Computing Platform

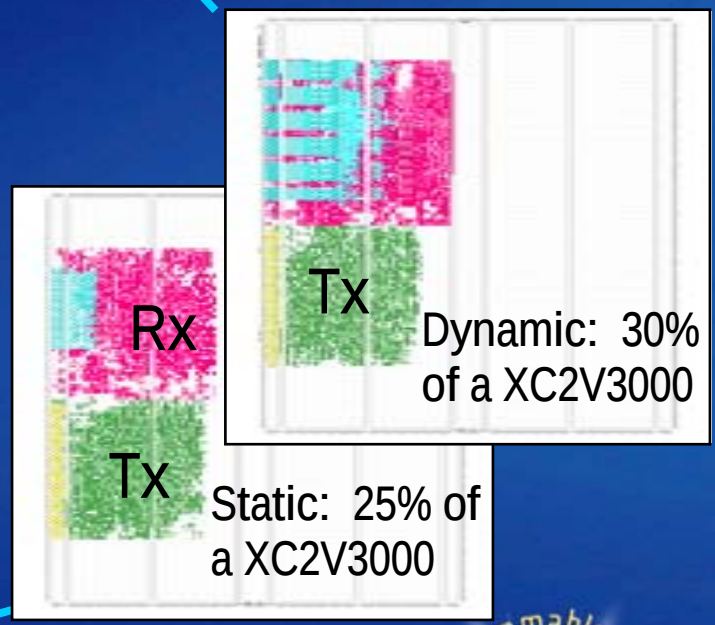
Quad SPI-3 to SPI-4.2 Case Study



SPI-4.2 Core Implementation



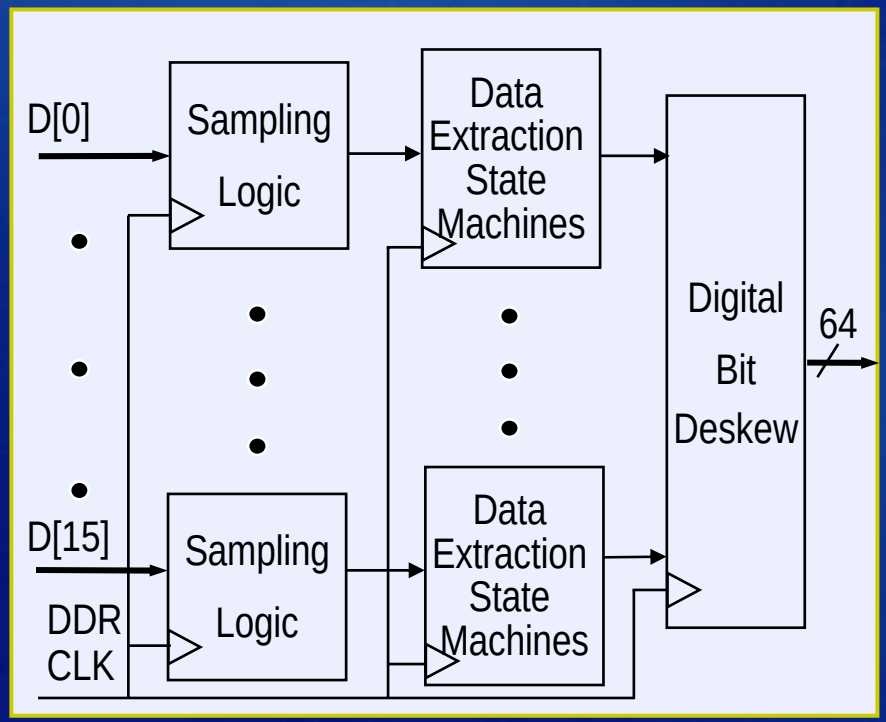
- Static or Dynamic - only front-end I/O changes
- Common pinouts for Static or Dynamic Alignment

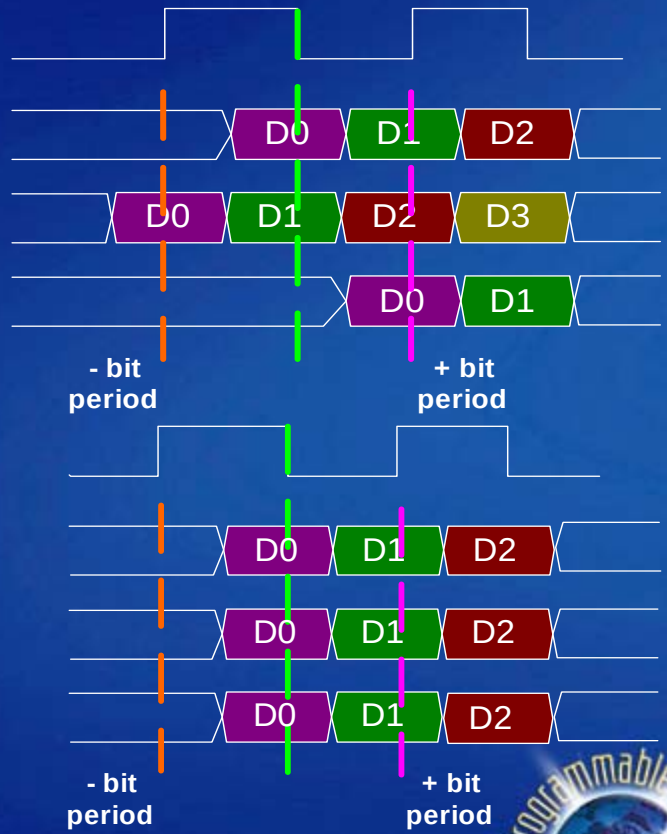


SPI-4.2 Floorplan

Dynamic Alignment

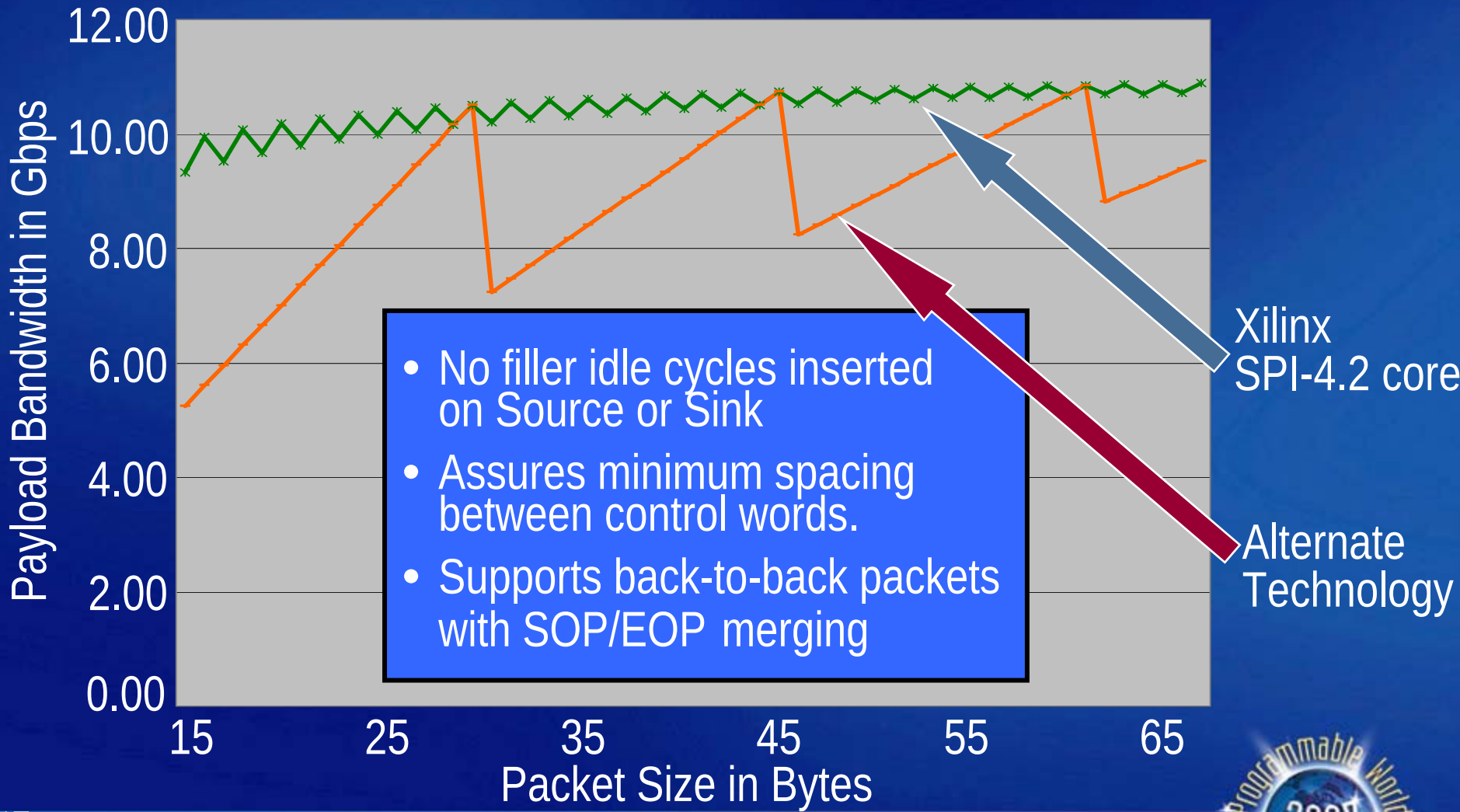
- Compensate up to +/- one bit period of skew
- State Machines produce 2-bits per rising/falling clock edge
- Digital Bit Deskew uses training patterns to deskew-realign all 16 channels into a 64-bit bus





High Bandwidth Solution

SPI-4.2 core optimized for data payload bandwidth



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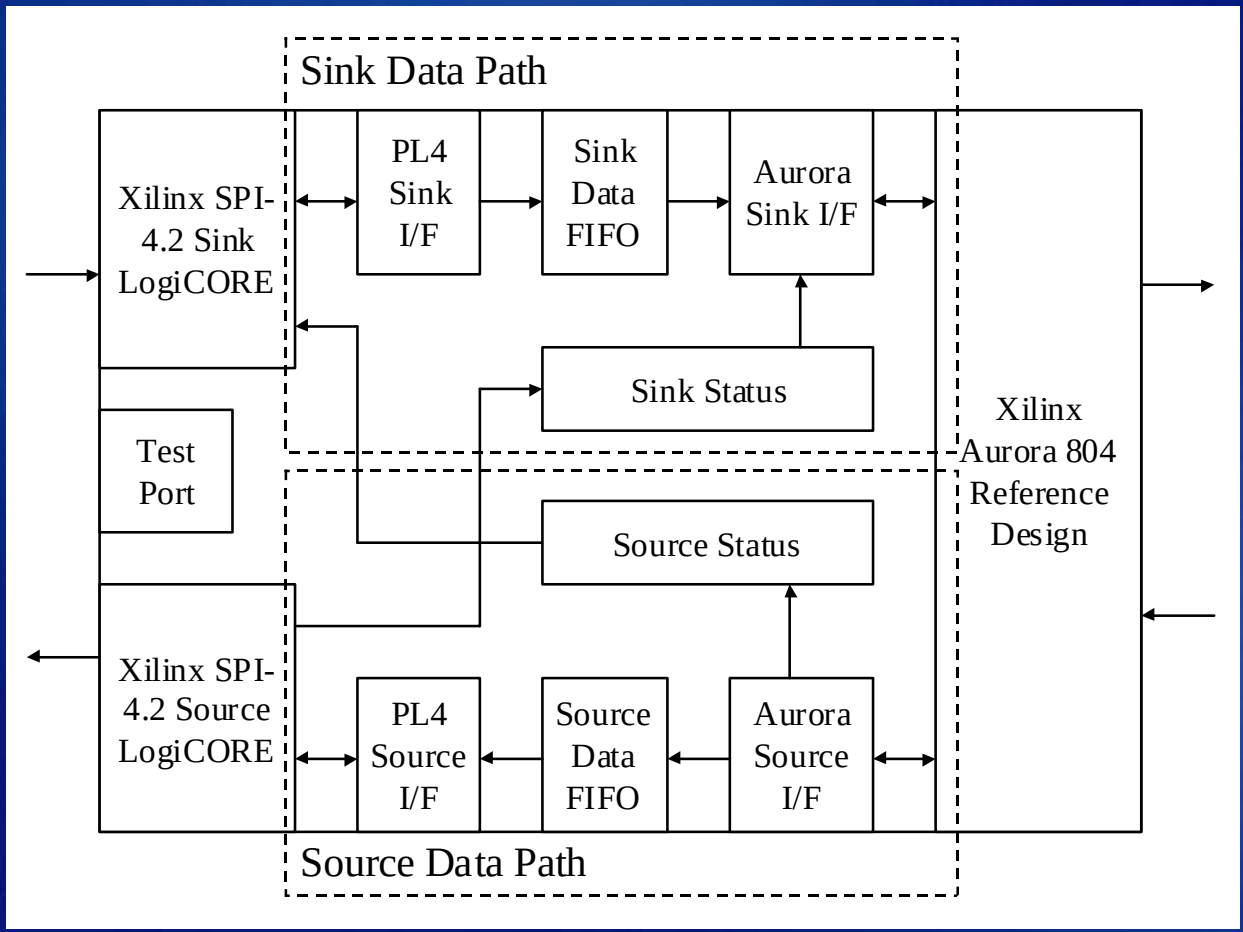
SPI-4.2 to Aurora Case Study

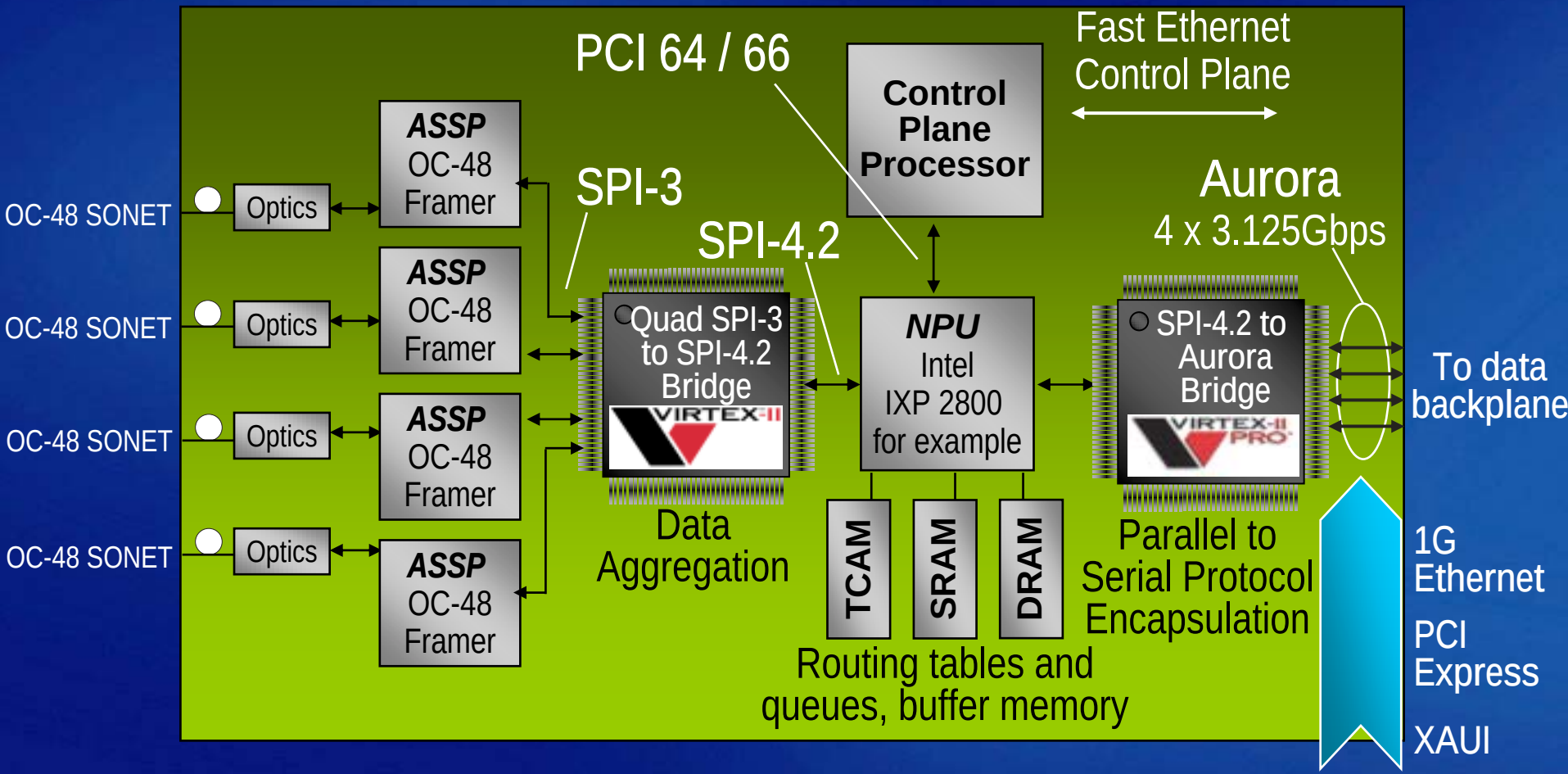
Line Card Bridge For Parallel Interface To Serial Backplane



Aurora

- Xilinx defined link-layer protocol
- Scalable & lightweight
- Provides a transparent interface to encapsulate upper layers of proprietary or industry standard protocols
- Ethernet or TCP/IP
- Preserves software infrastructure investment

NPU Application Example



Virtex-II Pro: Ideal for other PICMG ATCA backplane standards

XILINX®

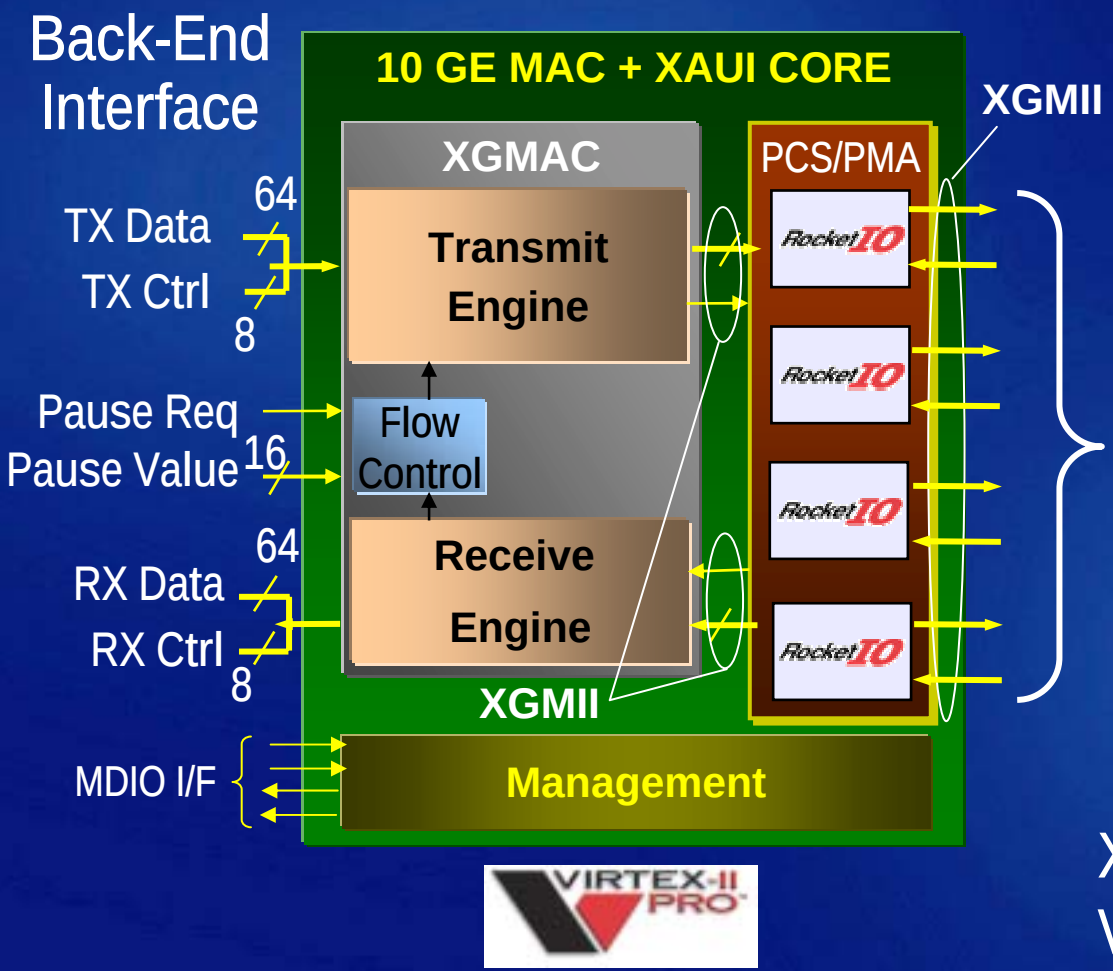
PCI Express - Complete Endpoint Solution

- Provides full physical layer, data link layer, and transport layer
- Compatible with the PCI Express base specification v1.0A
- Local Link universal packetized interface on the back-end
- World's first hardware demo at IDF, Fall 2002

Implementation example in Virtex-II Pro XC2VP50

- 24% Utilization Single lane
- 2.5G line rate using (1) RocketIOTM transceiver

10 GMAC with XAUI Interface



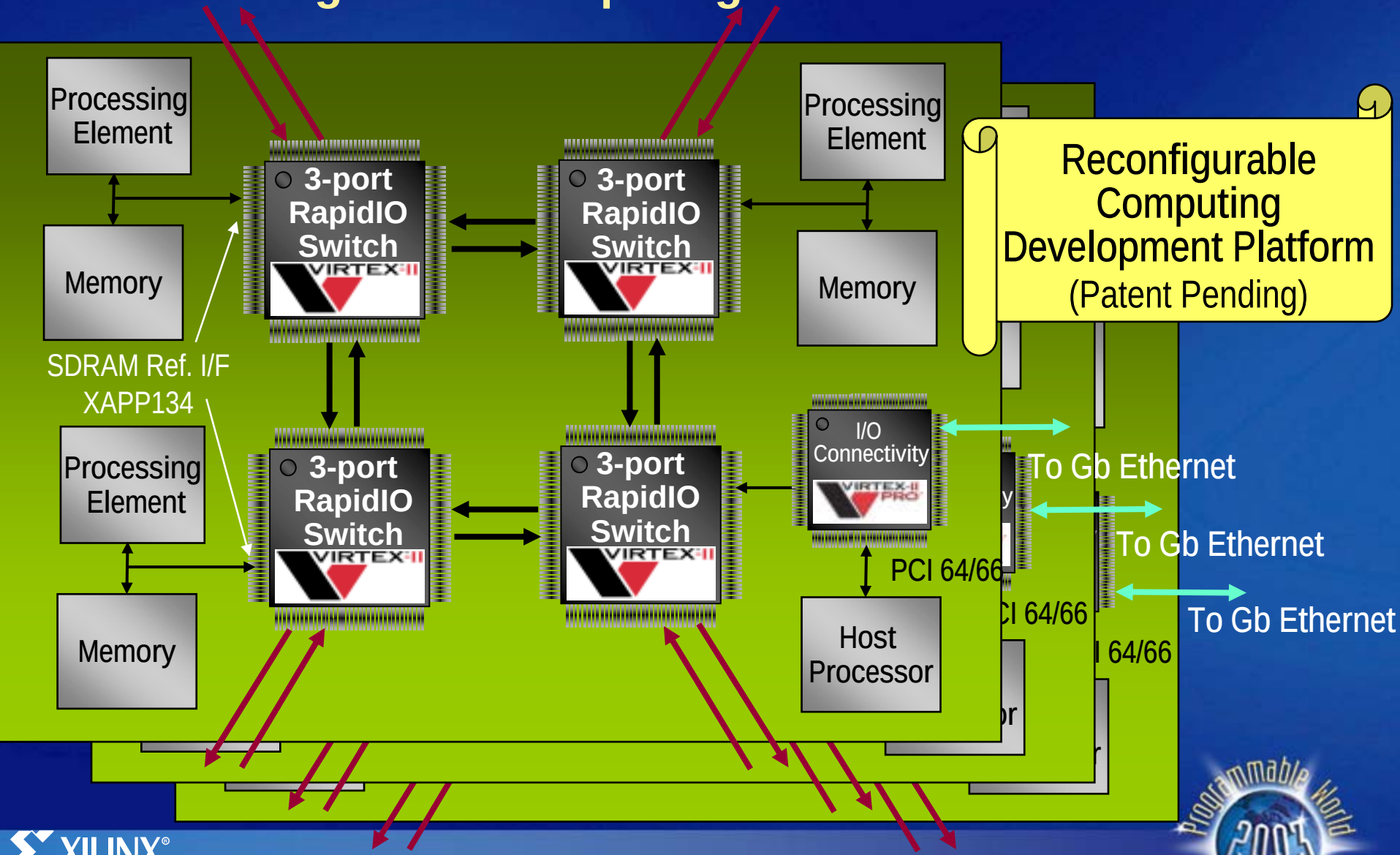
Virtex-II Pro Implementation

- ~ 3800 slices (40% of a 2VP20)
- 3 Global clock buffers
- 4 RocketIO transceivers

XAUI Floorplan
Virtex-II Pro XC2VP20

RapidIO Case Study: Systran Federal

Reconfigurable Computing Switch Fabric Network



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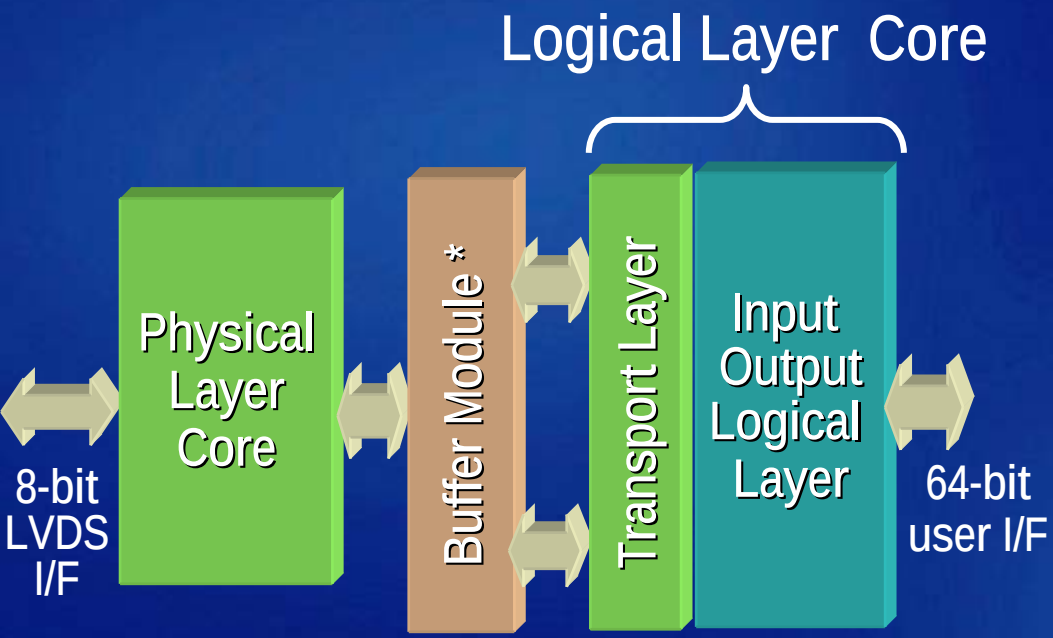
RapidIO IP Cores
Physical Layer & Logical Layer



- Complete RapidIO end point solution
- Implements Rev 1.2 of RapidIO Spec
- 8 Gbps aggregate bandwidth
- Physical Layer
  - Uses 19% of a XC2V2000
  - Supports HW error recovery
- Logical Layer
  - Uses 7% of a XC2V2000
- HW demo at CDC '02

VIRTEX-II PRO

Buffer module available as a design example

CMP COMMUNICATIONS DESIGN CONFERENCE

Programmable World 2003

XILINX®

Memory Connectivity using Reference Designs

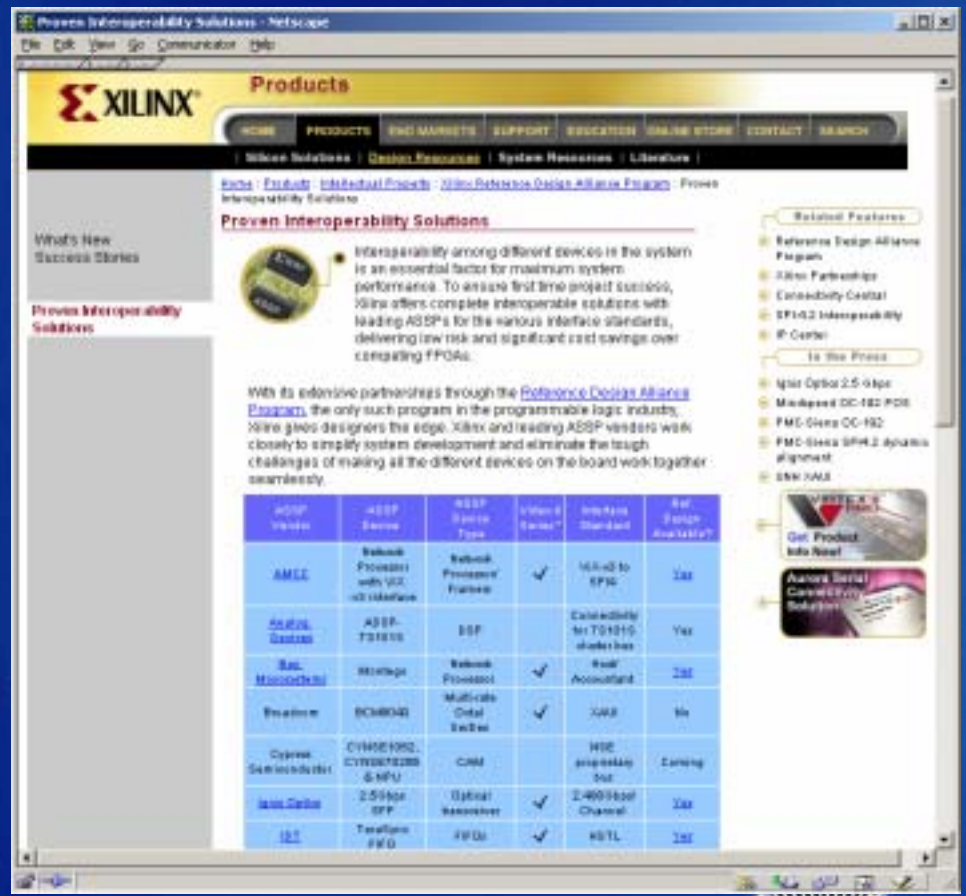
- Tailored to the device technology
- Fully synthesizable VHDL / Verilog
- User-customizable
- Readily transferable to commercial designs
- Full suite of evaluation boards available

SDRAM, SRAM,
FC RAM, RLDRAM

Accelerates development of robust, flexible memory interfaces

Interoperability and Standards Compliance

- Verified interoperability with ASSP suppliers
  - Increases customer confidence
  - Drives customer-ready reference designs
  - Simplifies PCB implementation
  - Improved time-to-market

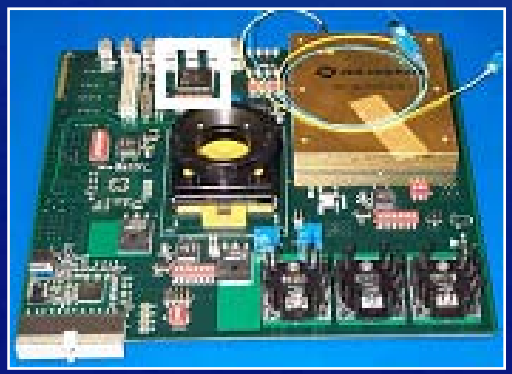


XILINX® http://www.xilinx.com/company/reference_design/interop_solutions.htm

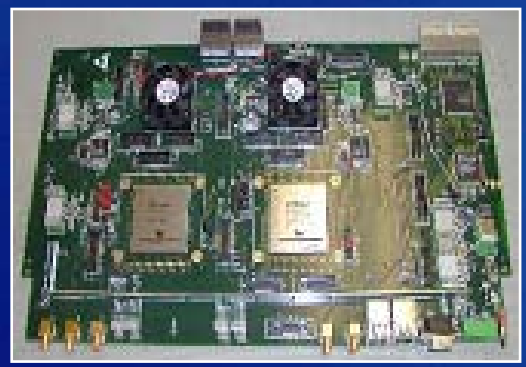
Proven Interoperability

Vitesse Meigs-II
10Gbps Ethernet MAC

AMCC Ganges-II
PHY device



Mindspeed M29730
PHY device



PMC S/UNI 9953
PHY device

- Validates...
  - Electrical signaling
  - Protocol compliance
  - Performance
- Proven in hardware
- Extensive ecosystem

OIF Physical and Link Layer Interoperability Demonstration

- Successful ***public*** interop test
  - Vitesse Meigs-II™VSC7321 MAC
  - NEC Ridge Tx/Rx/PHY chipset
- Used LVDS demo board
  - Virtex-II XC2V1000 + SPI-4.2 core
  - Dynamic Phase Alignment
  - 700 Mbps
- Only FPGA supplier to participate

OIF
OPTICAL·INTERNETWORKING·FORUM

OFC 2003
OPTICAL FIBER COMMUNICATION
CONFERENCE & EXPOSITION

http://www.oiforum.com/public/pressroom/OIF_OFC03.pdf

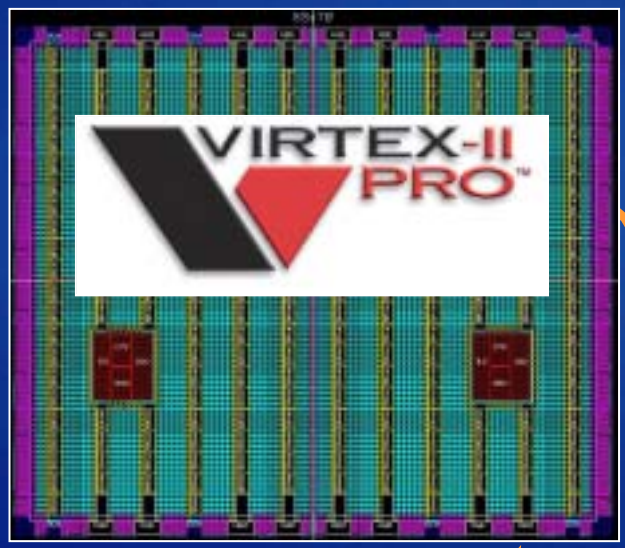
Ethernet Interoperability

- Xilinx Ethernet solutions tested by UNH Interoperability Lab
  - 10/100, 1GE, and 10GE MAC
  - Tested against IEEE compliance standards
  - Multiple configurations tested, including XAUI
- UNH using Xilinx board for pre-test and pattern generation
- Only FPGA supplier participating

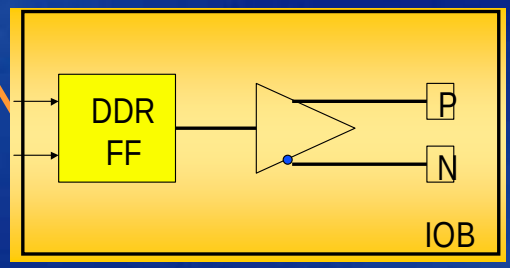
University of New Hampshire InterOperability Lab

10GEA 10 Gigabit Ethernet Alliance

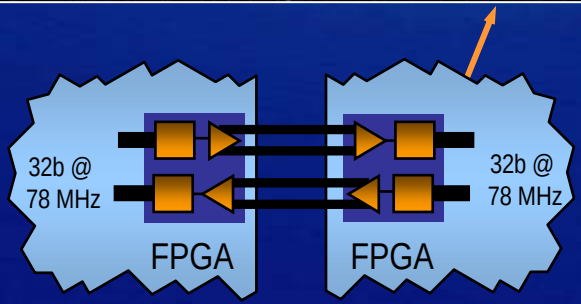
Serial and Parallel Connectivity on One Platform



SelectIO™-Ultra for parallel interfaces

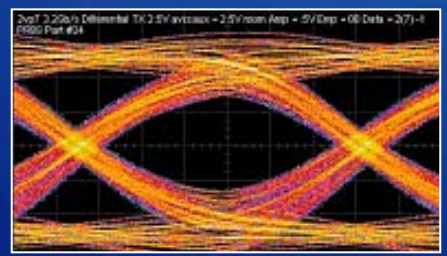


- 25 I/O Standards
- XCITE Technology
- Dedicated DDR Registers
- 840 Mbps LVDS
- 644 Mbps SDR

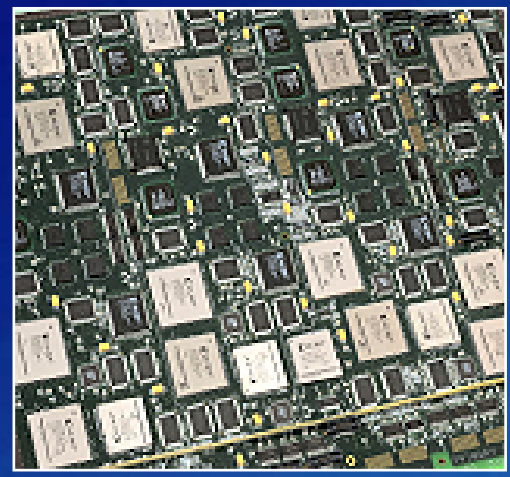


Multi-Gigabit Serial Transceivers

Up to (24) 3.125 Gbps transceivers



Ultimate Connectivity



LAN / WAN / MAN

- 10/100 Ethernet (MII)
- 1Gb Ethernet (GMII)
- 10Gb Ethernet (XGMII)
- 1Gb Ethernet (Phy)
- 10Gb Ethernet (XAUI)
- OC48
- OC192
- OC768

Boards / Backplanes

- PCI 32/33
- PCI 64/66
- PCI-X 133
- RapidIO
- Ser. Fibre chan.
- 10GE(XAUI) SONET
- RapidIO
- CSIX
- HyperTransport
- InfiniBand
- PCI Express
- Aurora

Chip-to-Chip

- PCI 32/33
- PCI 64/66
- PCI-X 66, 133
- RapidIO
- SFI-4
- 10GE (XAUI)
- SPI-3 / SPI-4.2
- Flexbus 4
- CSIX
- HyperTransport
- XSBI
- PCI Express

VIRTEX-II PRO

- Parallel Standards – *enabled by SelectIO™-Ultra technology*
- Serial Standards – *enabled by RocketIO™ technology*

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Programmable World 2003

Solving the Connectivity Challenge

Platform FPGAs + IP Cores + Proven Interoperability

- Design to new emerging standards
- Update as the standard evolves
- Reduce risk and minimize “re-spins”
- Deliver more robust and competitive end products

xilinx.com/connectivity

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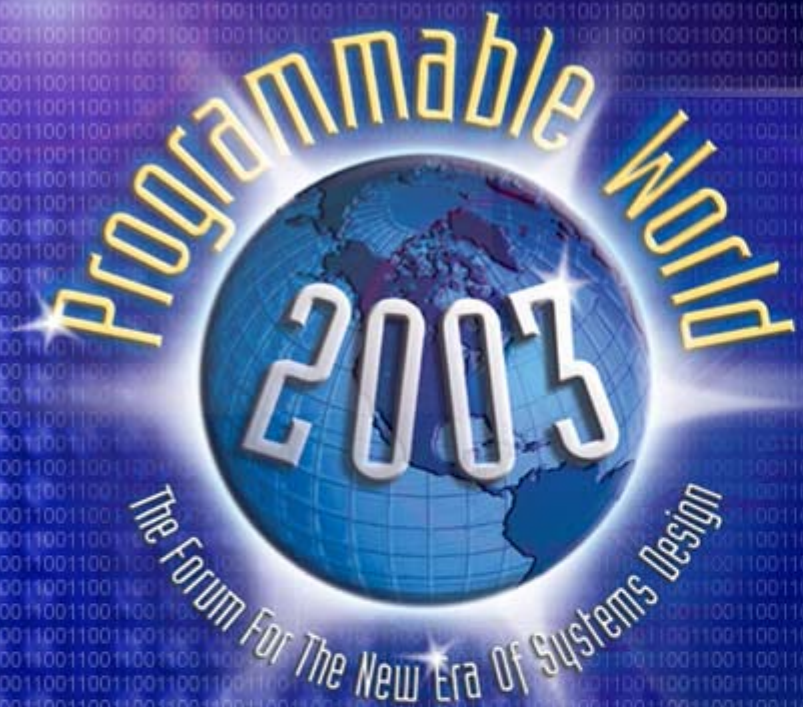
References

- Helpful Links
  - Connectivity Central: http://www.xilinx.com/connectivity
  - Aurora: http://www.xilinx.com/aurora
  - Proven Interoperability: http://www.xilinx.com/company/reference_design/interop_solutions.htm
  - Signal Integrity Central: http://www.xilinx.com/signalintegrity
  - Metro Access Networks: http://www.xilinx.com/esp/optical
- Design Resources - Available on PW03 Resource CD
  - Datasheets: SPI-4.2, Ethernet MAC, 10G Ethernet MAC, RIO
  - Memory Interface Reference Designs / Resources: RLDRAM, FCRAM, DDR SDRAM, QDR SRAM



Thank You!