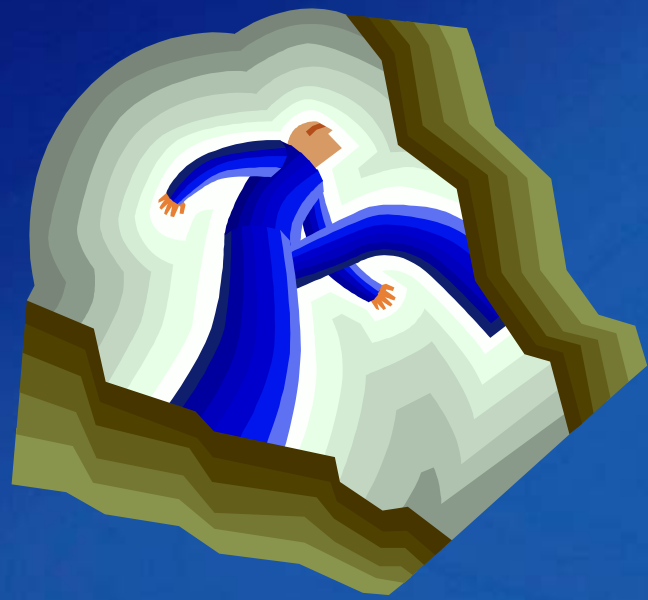
Platform Design Methods for Integrating Standard Processor Cores and Programmable Logic for Embedded Systems

Presentation Content

- Communications Platform Challenges
  - Platform Design Criteria
- The Perfect Marriage
- Design Options – Platform FPGA and Platform ASIC
- Two Examples: VPN Gateway and IP Phone
  - Explore performance, function partitioning, simulation, emulation and software features
- Tips for Design for Portability
- Embedded FPGA Blocks in IBM 90nm
- Summary
- Contacts and References

Challenges

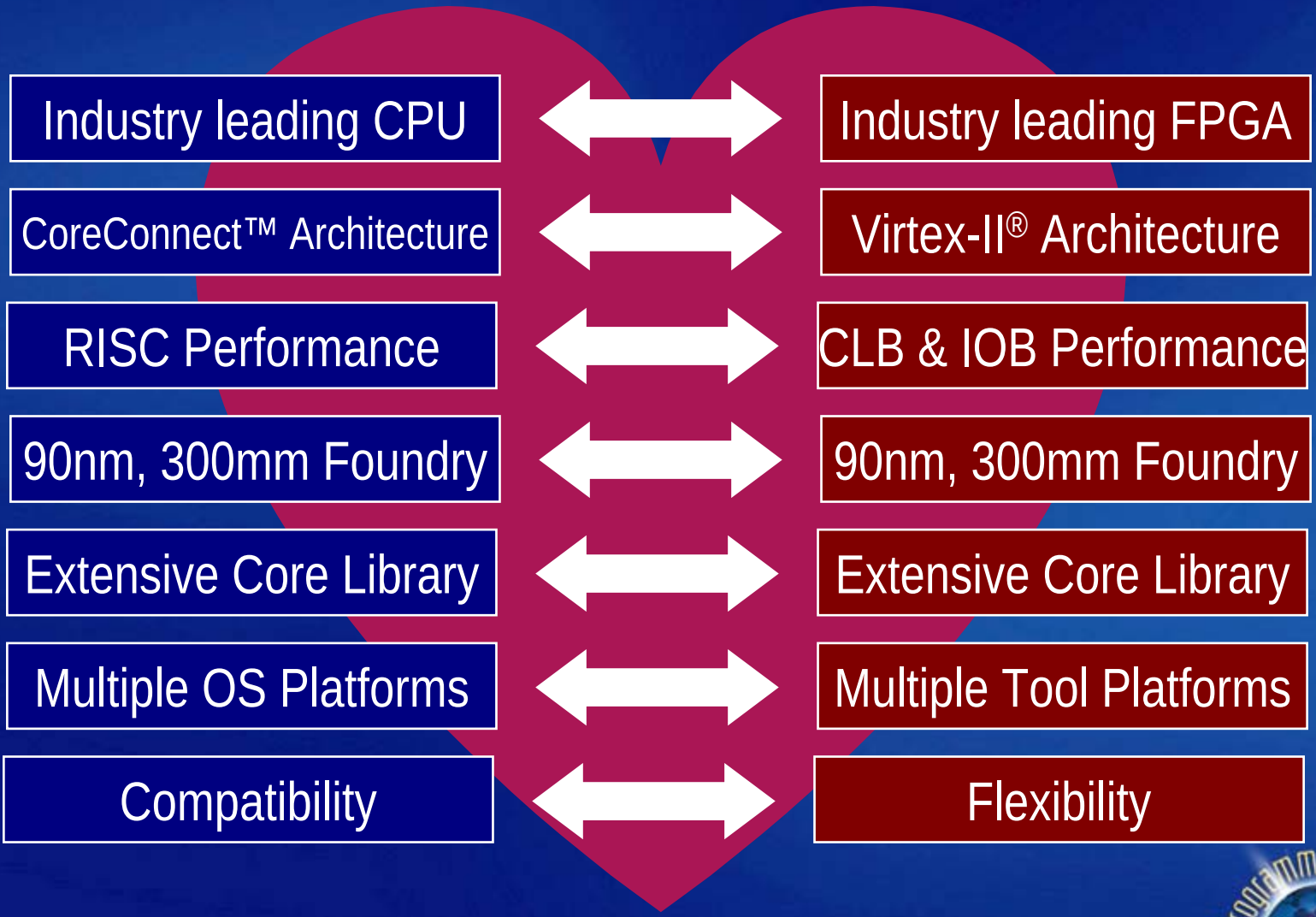
- New standards: 802.11g for wireless
- New interfaces: RapidIO, SPI4.X
- New applications: VPN, VoIP, WLAN
- Critical function and performance requirements
- High levels of integration, chip density, complexity
- System density & packaging versus power & thermal constraints



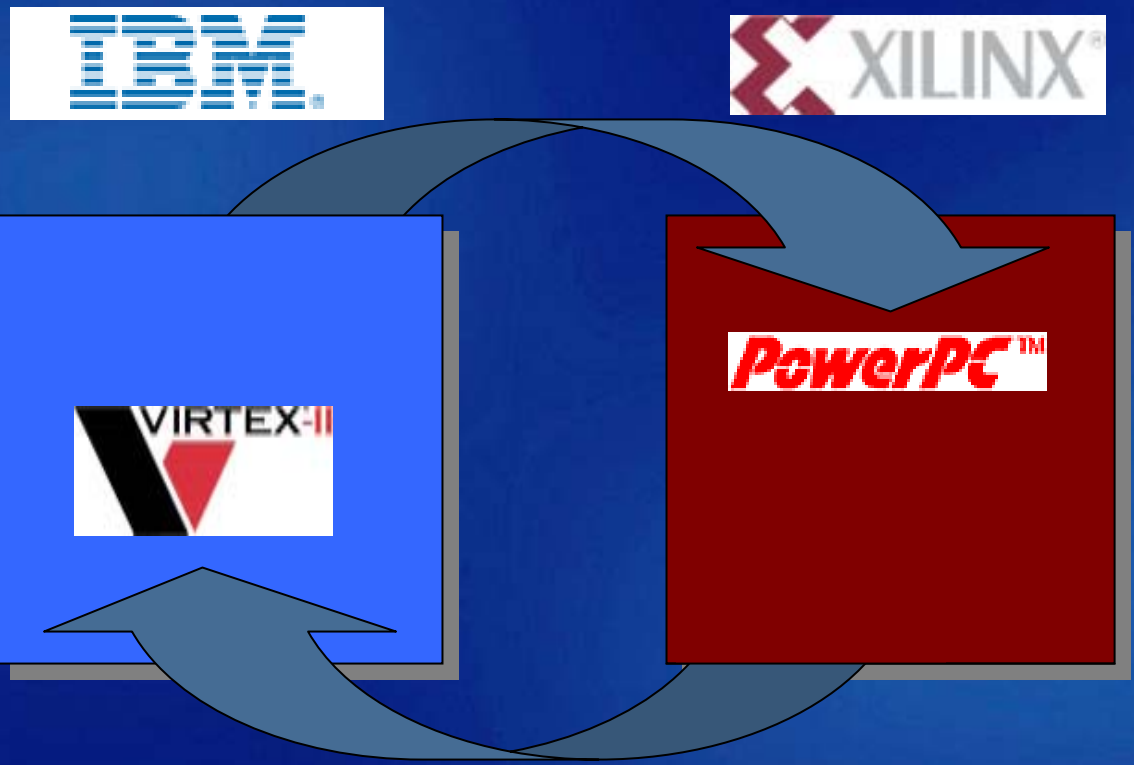
Platform Design Criteria

- Logic Design Criteria
  - Development cost
  - Available skills
  - Technology risks
  - Standard architecture
  - Tools availability
  - Flexibility/reuse
- System Design Criteria
  - Software base
  - Legacy support
  - Chassis & board space
  - Power & thermal
  - System performance
  - BOM cost
  - Building blocks
  - Volume requirements

A Perfect Marriage



IBM – Xilinx Covers the Entire Design Spectrum

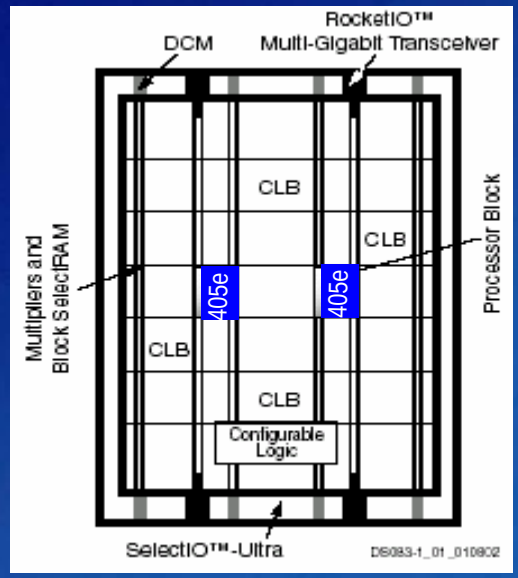


Platform ASIC **Platform FPGA**

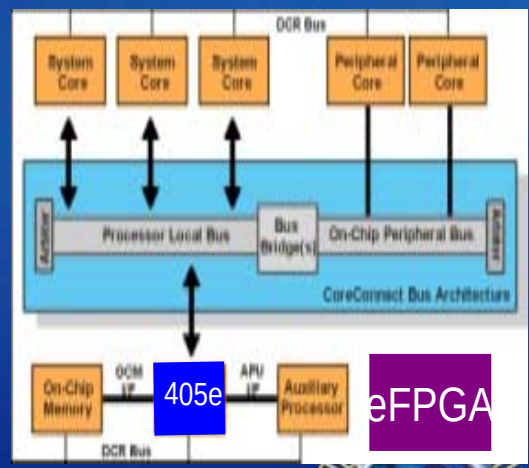
High-volume **Flexibility**

Platform Design Options

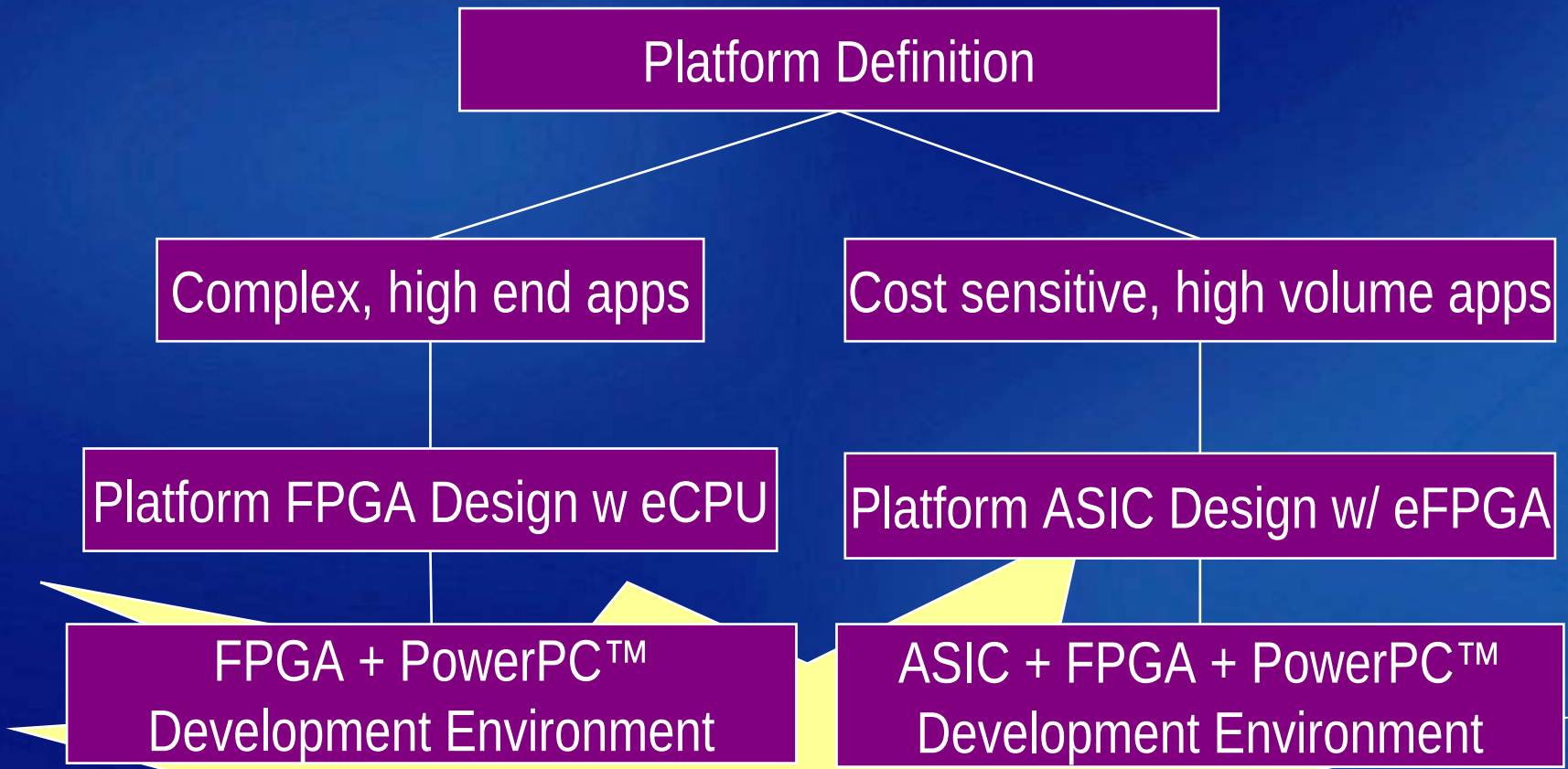
- Platform FPGA with embedded CPU
  - Fastest TTM, most flexibility



- Platform ASIC with embedded FPGA
  - Dense integration for low cost, high volume applications



Platform Design Options



PowerPC® + Virtex-II FPGA Value

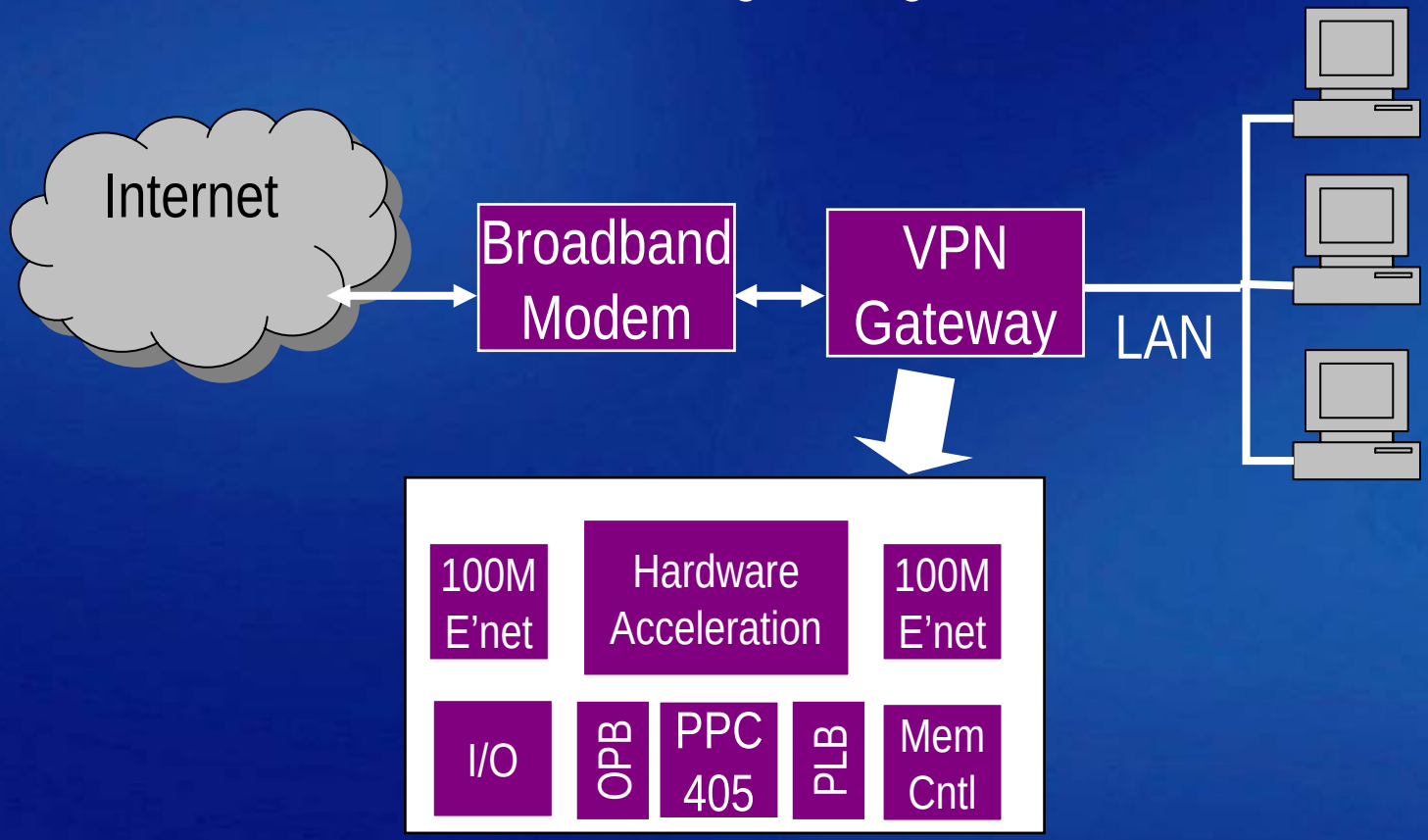
- Right the first time methodology
- Design flexibility; product flexibility
- Standard libraries, extensive support
- Pre-validated platform cores
- Best performance for software and hardware programmability
- Strong roadmaps with legacy protection

Example Platforms

- PowerPC® & Xilinx FPGA platforms covering the following design issues:
  - Fast turn around and system enablement
  - Standard product mixed with custom logic
  - Integrated tools for simulation and emulation
  - FPGA used to mitigate logic risk and add flexibility
  - Support for performance expansion and product derivatives
  - Available software

VPN Gateway Application

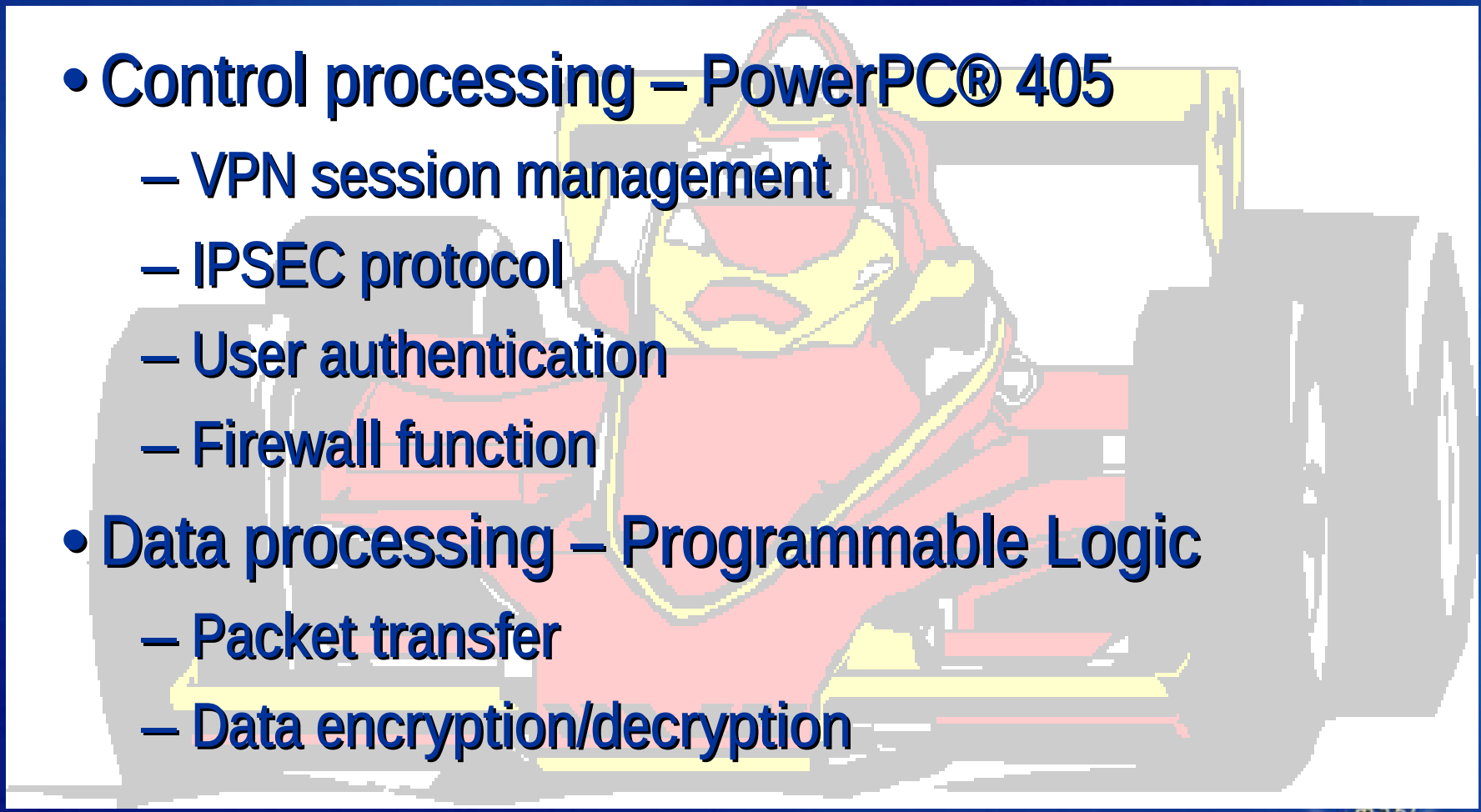
Platform FPGA design using Virtex-II Pro®



Virtex-II Pro with PowerPC 405 processor block

Performance Exercise

- Control processing – PowerPC® 405
  - VPN session management
  - IPSEC protocol
  - User authentication
  - Firewall function
- Data processing – Programmable Logic
  - Packet transfer
  - Data encryption/decryption



Performance Requirements

System Control -Embedded OS MV Linux/VxWorks - IP Firewall - VPN Session Manager - 30 VPN tunnels	PPC405 processor block - 333MHz, 500 MIPs - VPN performance 60Mbps (mixed packet sizes)
Hardware Accelerator Functions - 3DES, DES, AES, MD5, SHA	Xilinx High Speed Encryptor/Decryptor - App note XAPP270 - Approximately 5000 LUTs
Network Connections	WAN – 100 Mbit Ethernet LAN – 100 Mbit Ethernet

Partitioning Exercise

- Balance function between CPU platform and programmable logic
- Separate low risk, standardized functions from high risk functions.
- Minimize design risk and maximize first-pass success
- Maximize enablement support
- Expansion and derivative plan

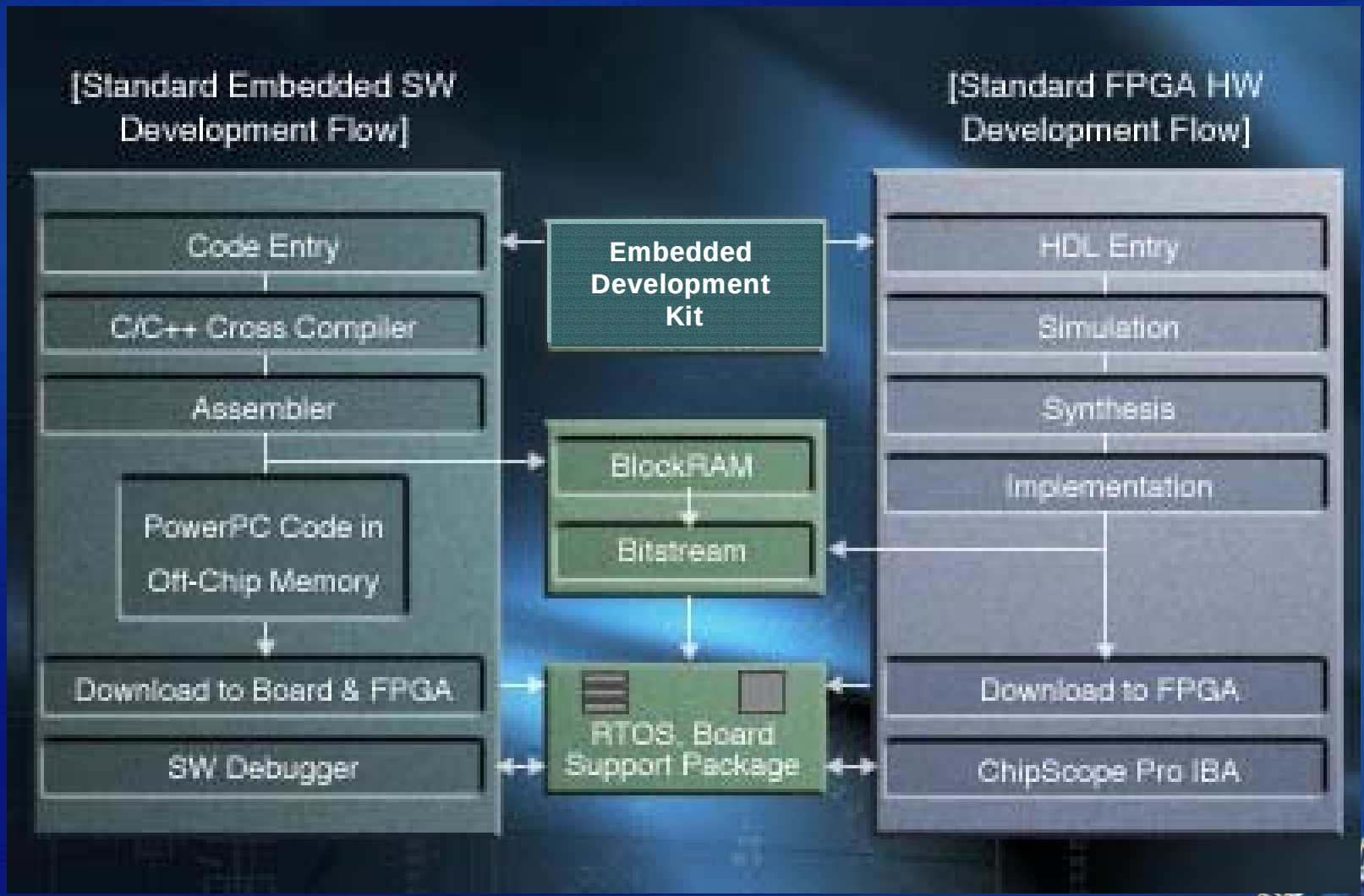
Function Partitioning

Module	Xilinx Virtex-II Pro® FPGA development sfw & tools	Standard part
System Processor	PPC405 processor block inside Xilinx VirtexII Pro PowerPC® support sfw & tools	Hard core w/ Core Connect peripherals
Peripheral I/O	10/100 Mbps Ethernet MACs, 64MB RAM interface, 4MB ROM interface	Xilinx library cores
3DES, DES accelerator	Implement XAPP720 app note - Approx 5040 LUTs	New logic

Design Emulation Option

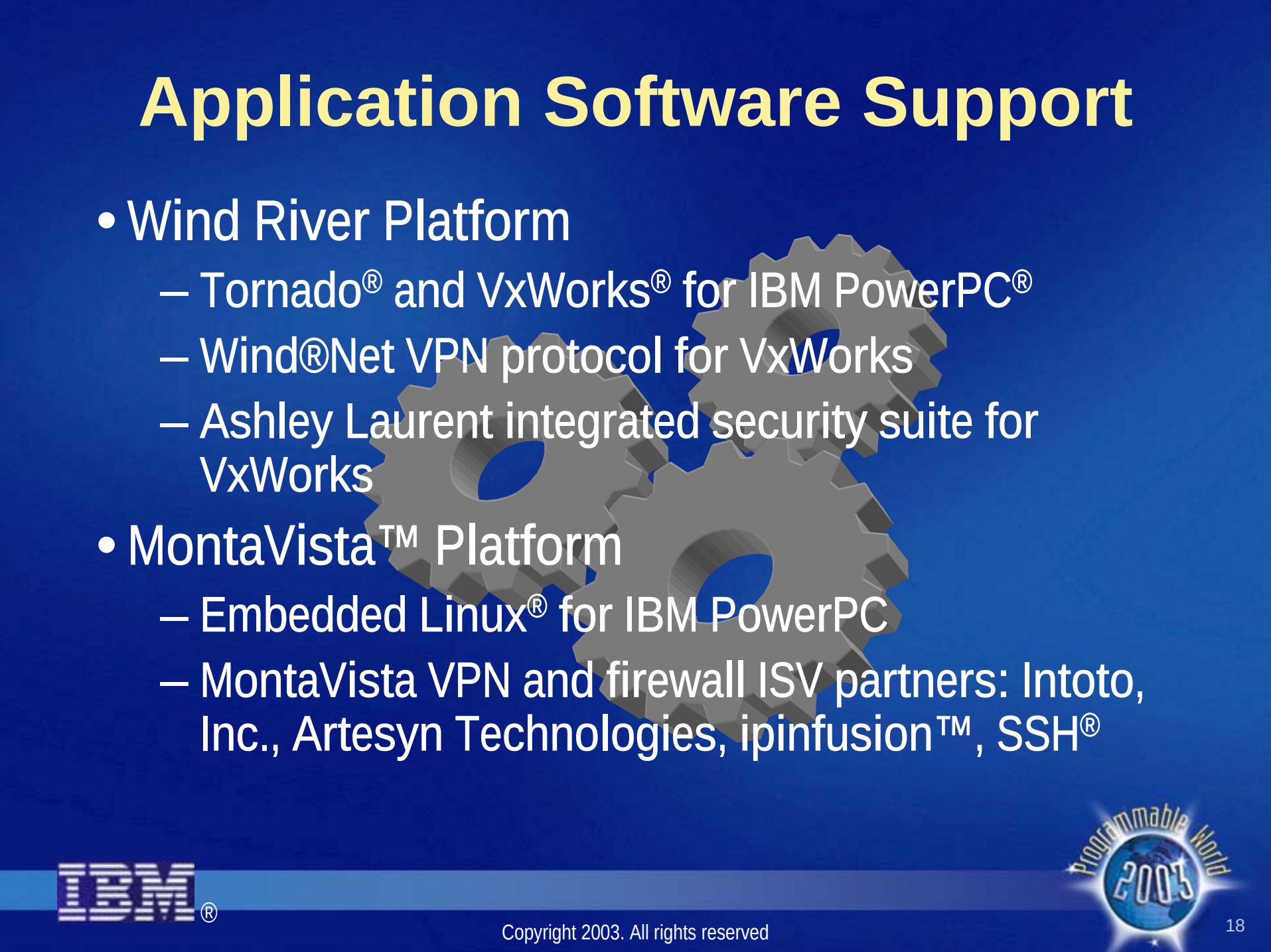
- **Xilinx: Virtex-II Pro P4/7-FG456 evaluation kit**
  - Supports 2VP4 or 2VP7 Virtex-II Pro FPGA
  - Single embedded PowerPC 405 w/ Core Connect bus
  - GNU based C compiler, assembler, linker and debugger
  - 8 M x 32 SDRAM memory
  - Expansion slot for user I/O
  - Configuration through JTAG and ISP PROMs
  - 2 x 16 character LCD

Combined Tool Flow



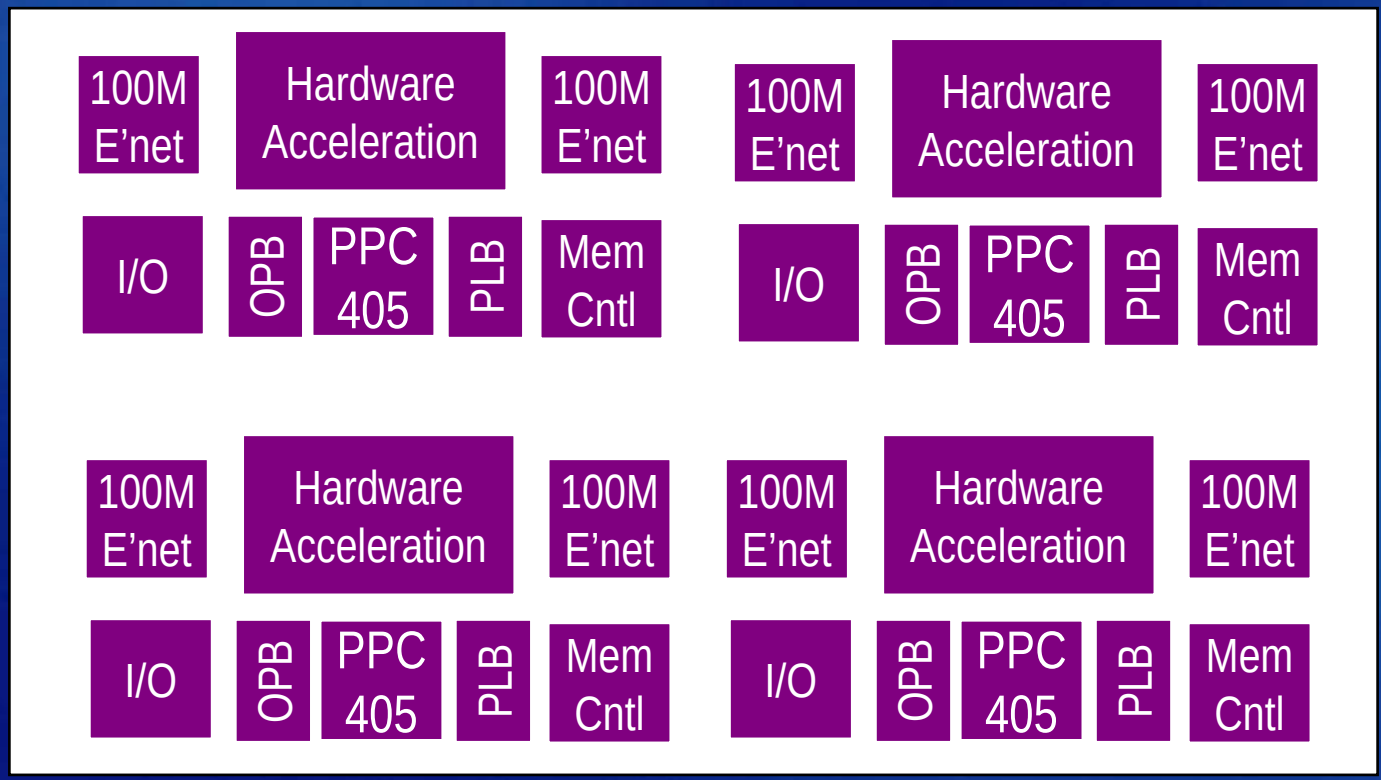
Application Software Support

- Wind River Platform
  - Tornado® and VxWorks® for IBM PowerPC®
  - Wind®Net VPN protocol for VxWorks
  - Ashley Laurent integrated security suite for VxWorks
- MontaVista™ Platform
  - Embedded Linux® for IBM PowerPC
  - MontaVista VPN and firewall ISV partners: Intoto, Inc., Artesyn Technologies, ipinfusion™, SSH®



Performance Expansion

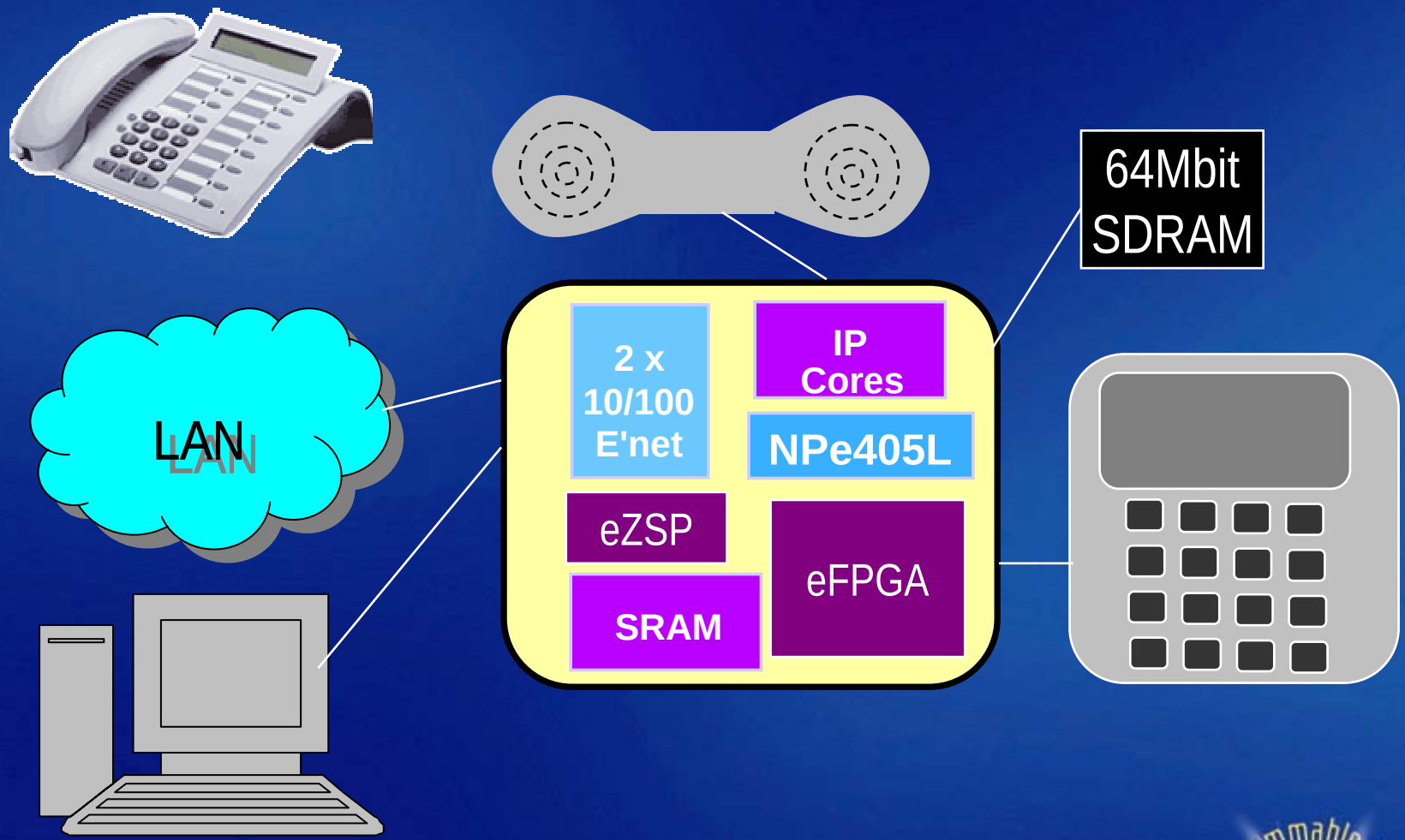
- A Virtex-II Pro with four PowerPC® 405 processor blocks can be used to produce a higher connectivity VPN solution



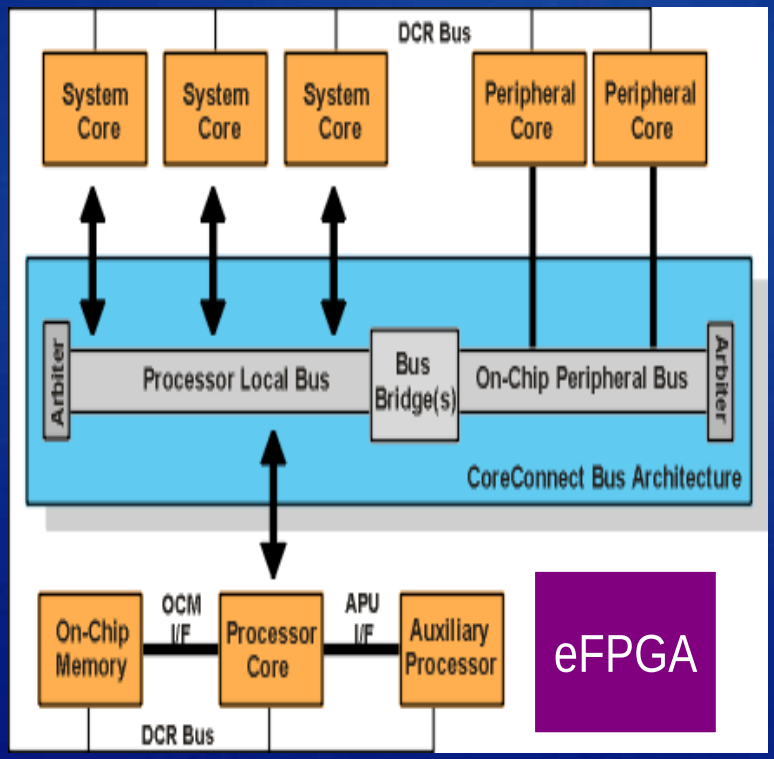
Xilinx Virtex-II Pro XC2VP125

Platform ASIC Example

IP Phone Application



Platform ASIC with PowerPC® CoreConnect™ and Embedded FPGA



Processor Local Bus
- Synchronous, 8 masters
- 32-, 64-, and 128-bit architecture
- Bus Pipelining, Split xactions

On-Chip Peripheral Bus
- Fully synchronous
- 32-bit address, 32-bit data bus
- Supports bus masters & slaves
- Bridge functions on PLB or OPB

Add eFPGA cores to PLB or OPB

All cores designed to CoreConnect™ specifications with time-consuming performance, functional, and timing pattern issues resolved

Performance Exercise

- Control processing
  - Send and receive IP packets from LAN interfaces
  - Switch packets between LAN, phone client and PC
  - Process commands from phone pad interface
  - Display status on LCD display
- Data processing
  - Process G.729a, G.711 voice CODEC
  - Process speakerphone, ADC/DAC

Performance Requirements

ASIC Technology	IBM 90nm
System Control - Embedded OS	100 MHz, 150 MIPs NPe405L 64Mb SDRAM, Boot ROM
DSP Functions - G.729a G.711 Voice CODEC - H.323 Speakerphone - Stereo/Mono ADC, DAC	100 MHz, 400 MIPs, 200 MMACs ZSP400 144 - 256KB eSRAM
Human Interfaces - LCD panal - Phone pad - LED's & function buttons	LCD interface, GPIO
Network Connection	2 x 100Mbit E'net

Function Partitioning

System Processor	Verified PPC405 core layout w/ SDRAM mem ctl, SRAM, DMA, UART, GPIO, JTAG. Max 300MHz	Pre-validated hard or soft cores
Common I/O	10/100 Mbps Ethernet MACs, ROM interface	Soft cores
Codec, ADC/DAC functions	LSI ZSP400 tied to 405 PLB	Hard core w/ software library
Custom LCD and phone pad interface	Programmable logic via internal eFPGA tied to OPB	Hard core

ASIC Development Tools

- Design Entry
  - Cadence Composer™, IBM Wizard™
- Simulation and Power Analysis
  - Cadence, MTI ModelSIM™, Synopsys VSS™
  - Synopsys DesignPower™, PowerCompiler™
- Logic/Physical Synthesis
  - Cadence BuildGates™, IBM BooleDozer™
  - Synopsys Design Compiler, Physical Compiler
- Test and Clock Synthesis
  - Cadence DFTS, LogicVision ICBIST
- Static Timing Analysis
  - IBM EinsTimer™, Synopsys PrimeTime™
- Post Layout Timing Analysis and Optimization
  - IBM CMOSChks, ChipEdit, ALSIM, 3DNoise

Swift Models and Software Simulation

- Based on Synopsys Smartmodel™ functional simulation
- Created from Verilog RTL and netlist
- Use core level Swift model for SoC design
- PowerPC core customers can contact IBM Design Center for access.
- Simulator Configuration Guide for Synopsys Models, simcfg.pdf, at http://www.synopsys.com

Power PC® 405EP Evaluation Platform

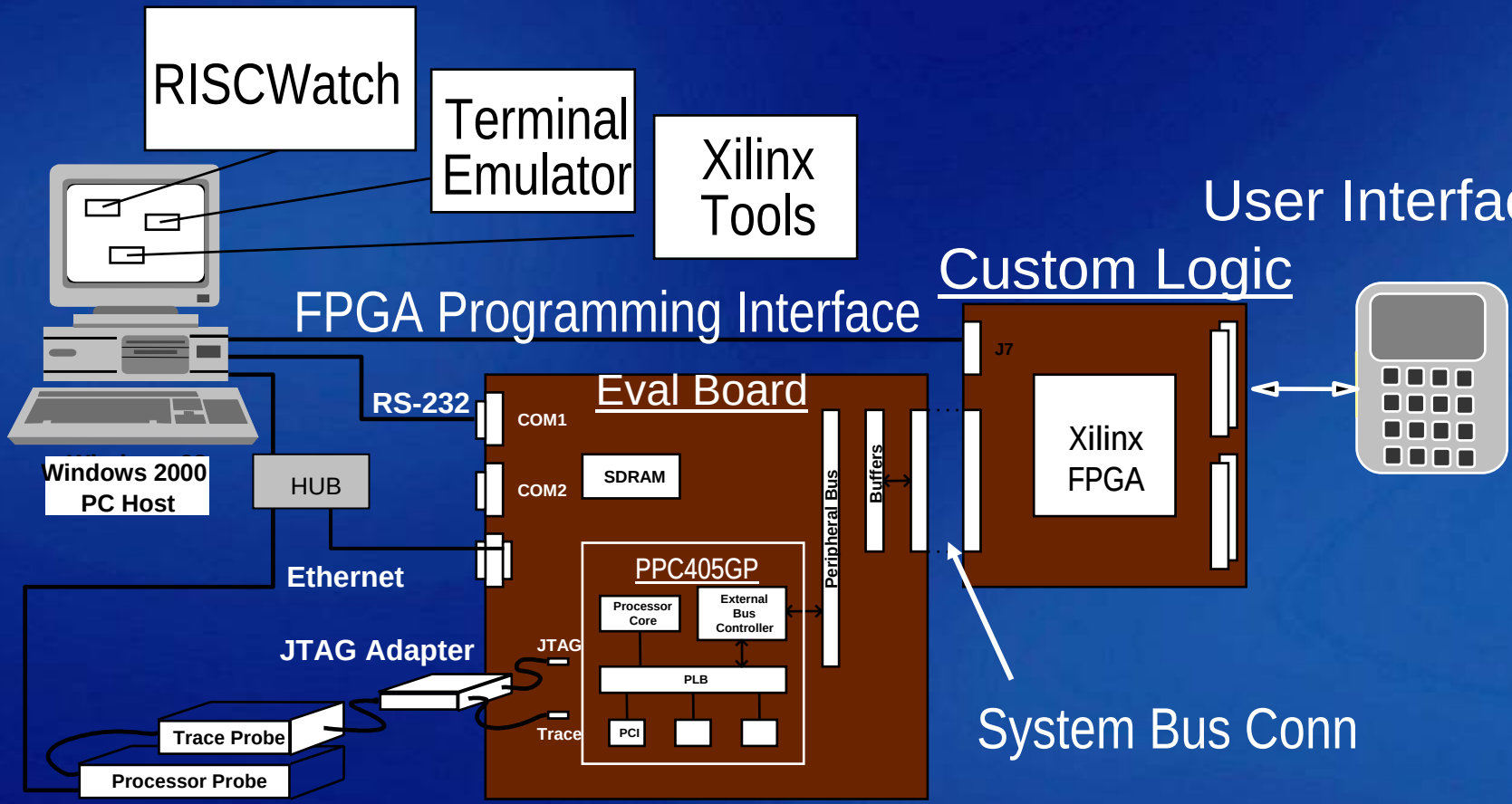
External Bus Connector for FPGA daughter board

32-bit PCI

Serial, Keyboard/Mouse, LAN

RiscWatch trace tool connection

Emulation System



Emulation System

Eval Board

-PPC 405GP System-on-Chip
-COM I/O
-Ethernet port
-SDRAM
-PCI Slots
-ROM monitor ← RiscWatch
-OS Open
-Linux

RISCWatch

-GUI User Interface
-User-Defined windows
-Command files
-JTAG interface to 405GP
-Built in debug support

Application Software Support

- Wind River Platform
  - Tornado® and VxWorks® for IBM PowerPC®
  - Windriver partner, Pingtel – IP Phone Software
  - Windriver partner, Micro PKI – C Security Toolkit Designed for Embedded Devices
- MontaVista™ Platform
  - Embedded Linux for IBM PowerPC
  - MontaVista ISV partner, Access Ltd – Netfront® Information appliance software

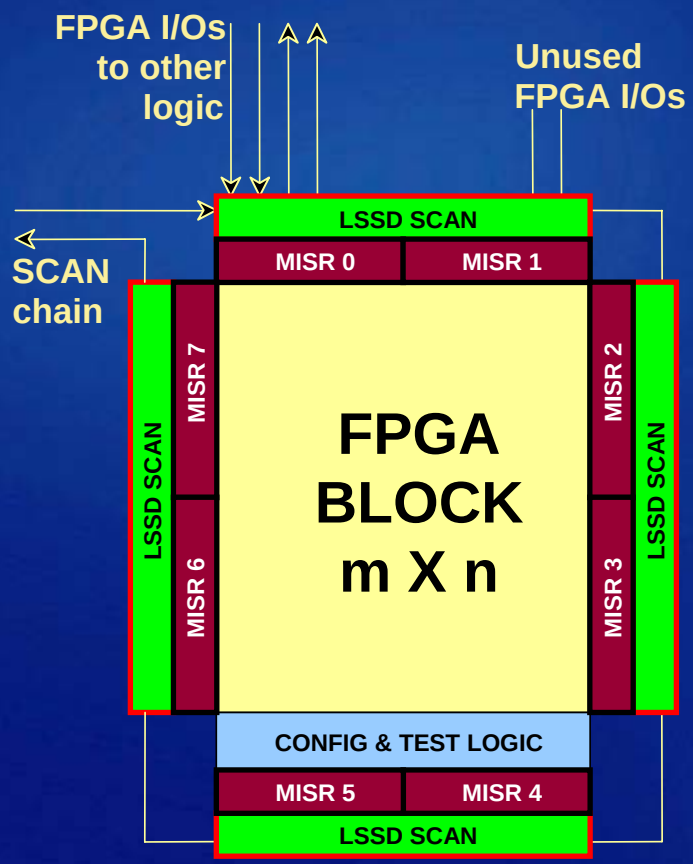
Portable Software Tips

Category	Standard OS	Open Source OS
API's	Application framework software	Use standard API – POSIX
Drivers	Device driver library and device driver development kit	Open source drivers
Make/Build	Application framework software and specific conversion kits	Leverage porting and emulation kits

More on Embedded FPGA's

- Collapse multiple designs into a single ASIC
  - Families of chips w/ similar functions
  - Design upgrades & added features post-tapeout
  - Accommodate evolving industry standards
- Bug-fix capability for specific high-risk logic
  - Control for dataflow
  - New vs. reused logic
  - Parallel design & verification
- Provide embedded debug & test circuitry on-demand
- Prototyping of design updates
- Customizing designs to unique customer requirements

Embedded FPGA Block

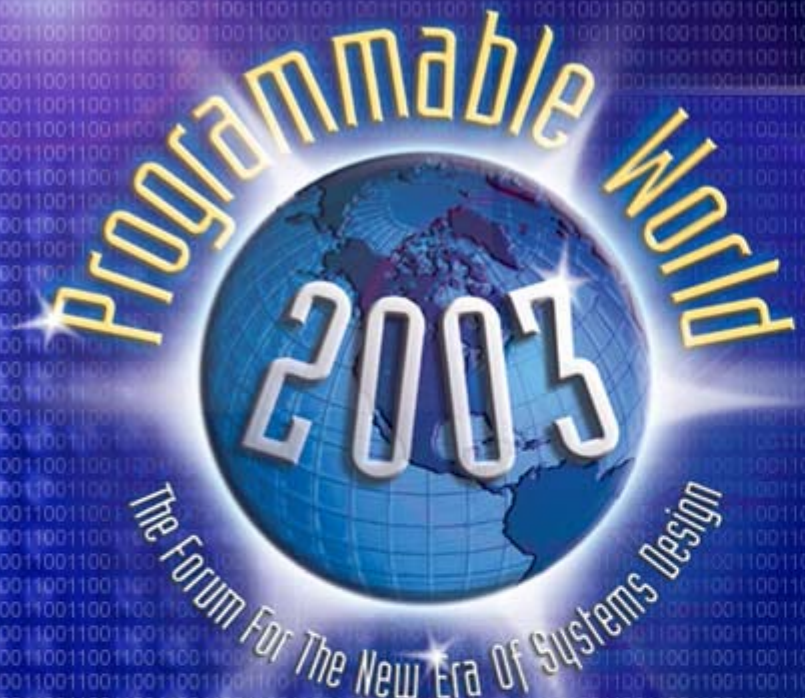


- Cores are derivatives of Xilinx Virtex-II architecture
- IBM methodology & toolset used for overall ASIC processing
- eFPGAs handled as custom hard cores
- Xilinx toolset used to configure, P&R, & time FPGA macros
- Xilinx basic FPGA fabric in IBM's 90nm 9SF fab process
- Virtex-II s/w base complete & in use
- Three sizes: 128, 256, 384 CLB's; 3, 5, 7 sq mm image
- Up to 400K programmable gates

Summary

- IBM PowerPC™ plus Xilinx Virtex-II® FPGA performance and flexibility
  - Platform SoC or Platform FPGA options
- PowerPC Value
  - Standard and open source OS platforms
  - Compilers, simulation tools, development kits w/ real time debugging
  - SoC peripheral cores via Core Connect architecture
- Xilinx FPGA Value
  - Effective risk management for custom logic
  - Large library of pre-validated core logic
  - High speed, flexible interface support via RocketIO
  - Integrated software development with real time logic development
- PowerPC + Virtex-II = Reduced design complexity and risk for faster TAT

IBM®



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Contacts and References

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