The Future of Programmable Digital Signal Processing:

Breaking The Moore's Law Barrier

Agenda

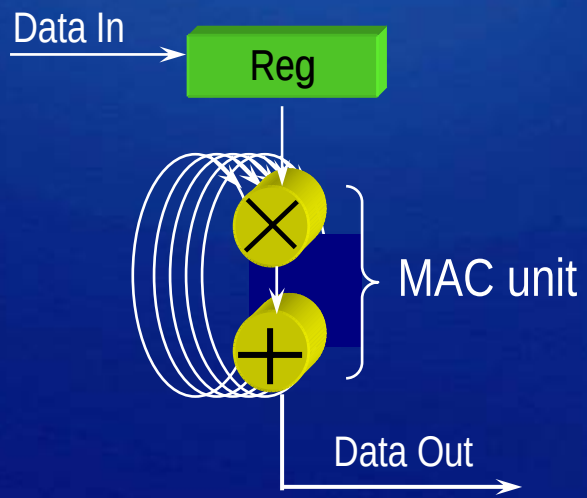
- FPGAs - outstanding extreme DSP engines
- Applications requiring extreme DSP
- Market dynamics favoring FPGAs for extreme-performance DSP
- Tool chain requirements to unlock this power
- Demonstration of FPGA DSP tool chain
- New low-cost FPGA for extreme DSP
- Summary

FPGAs Mean Parallelism

256 Tap FIR Filter Example

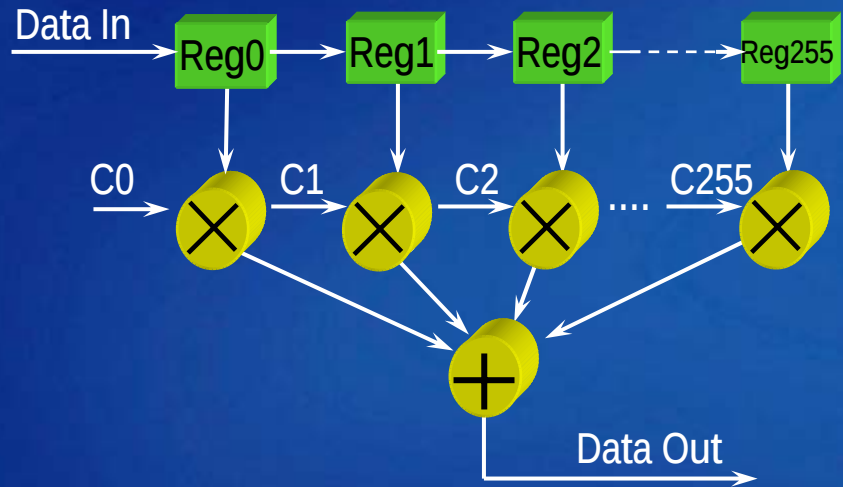
Conventional DSP Device

(Von Neumann architecture)



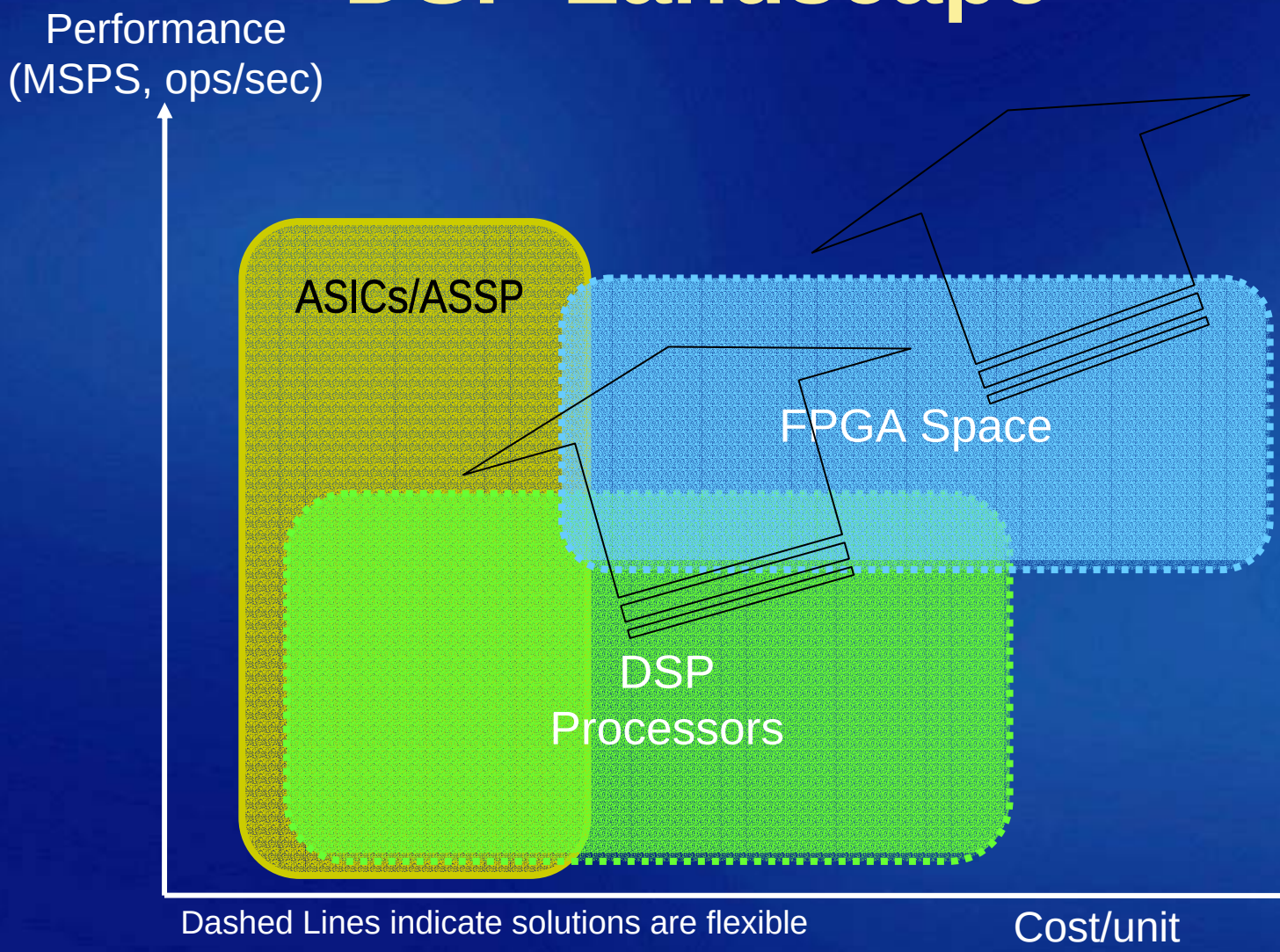
256 Loops needed to process samples

FPGA



All 256 MAC operations in 1 clock cycle

DSP Landscape



High-Performance Digital Signal Processing Fuels Hot Markets

Communications
Cellular base stations
Wireless and wired modems

Video
Broadcast video
Digital video
Plasma displays
Set-top boxes

Industrial
Machine-vision systems
Medical imaging
Test and Measurement

Military-Aerospace
Communications, radar, sonar

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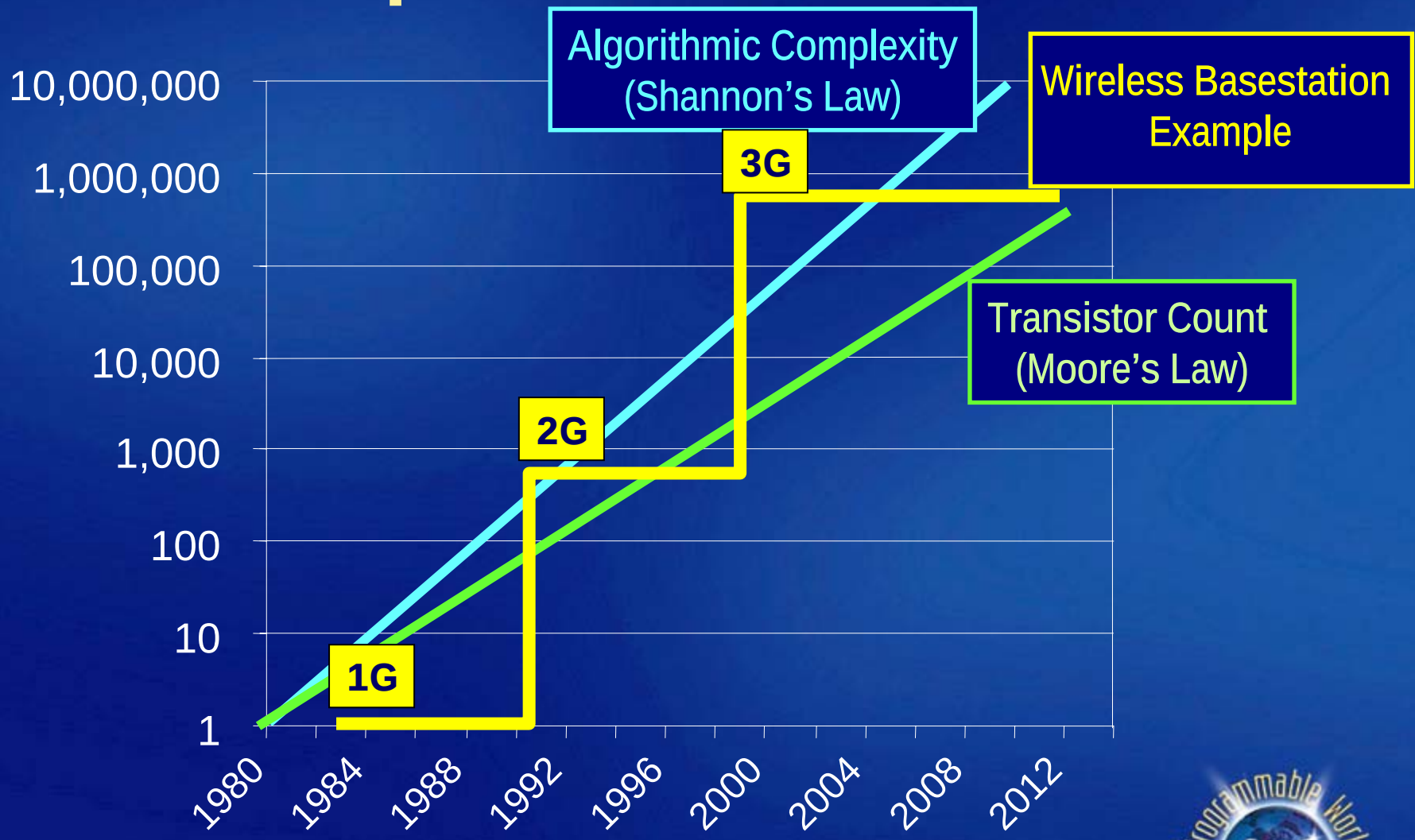
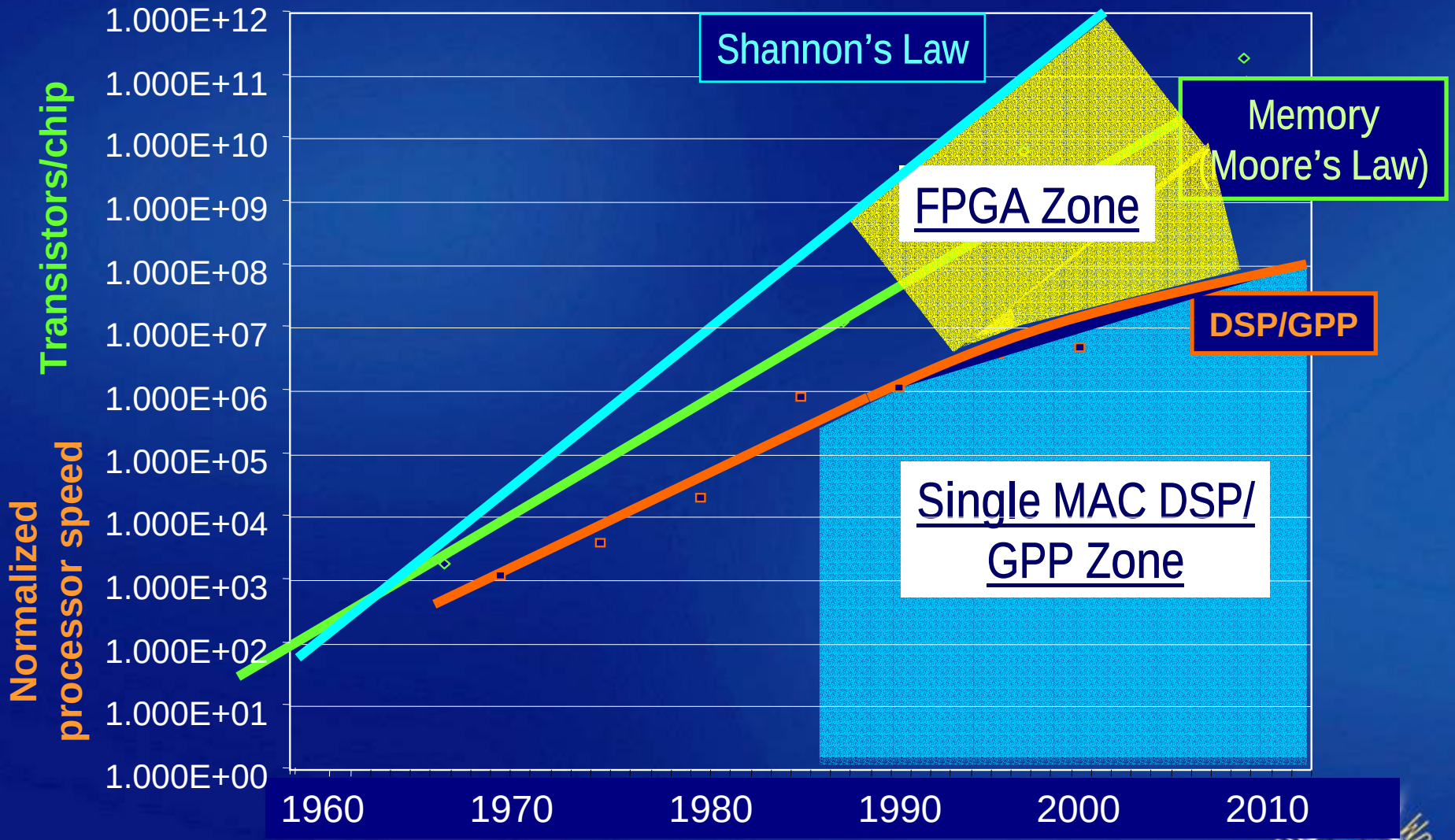
Algorithmic Complexity Outpaces Moore's Law



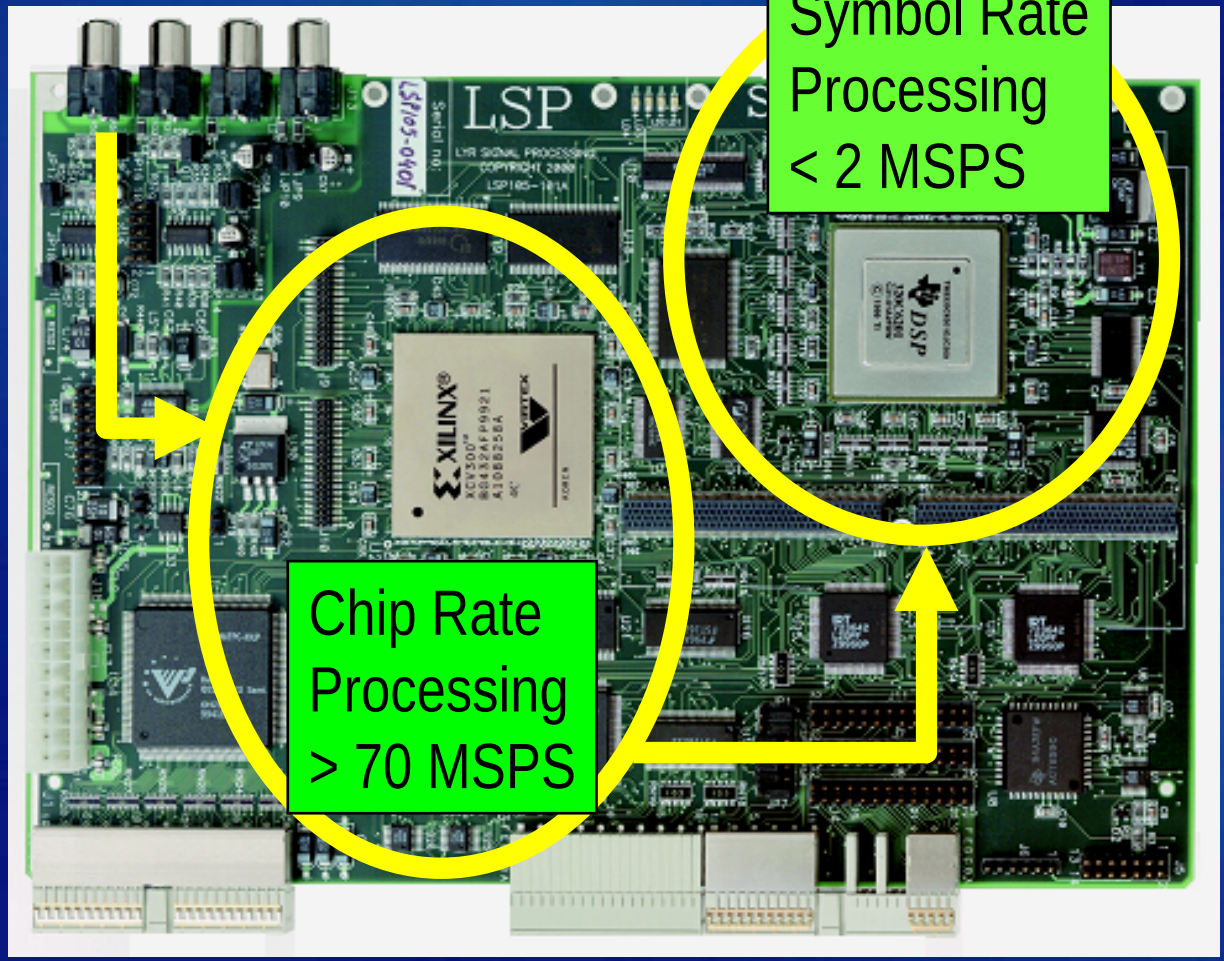
Source: Morphics and Jan Rabaey, BWRC

High Performance DSP



Source: Morphics and Jan Rabaey, BWRC

DSP Processors and FPGAs in Wireless Base Stations



- FPGAs and DSP Processors used jointly in many other applications:
  - Imaging
  - Industrial
  - Military

Why Both Co-exist

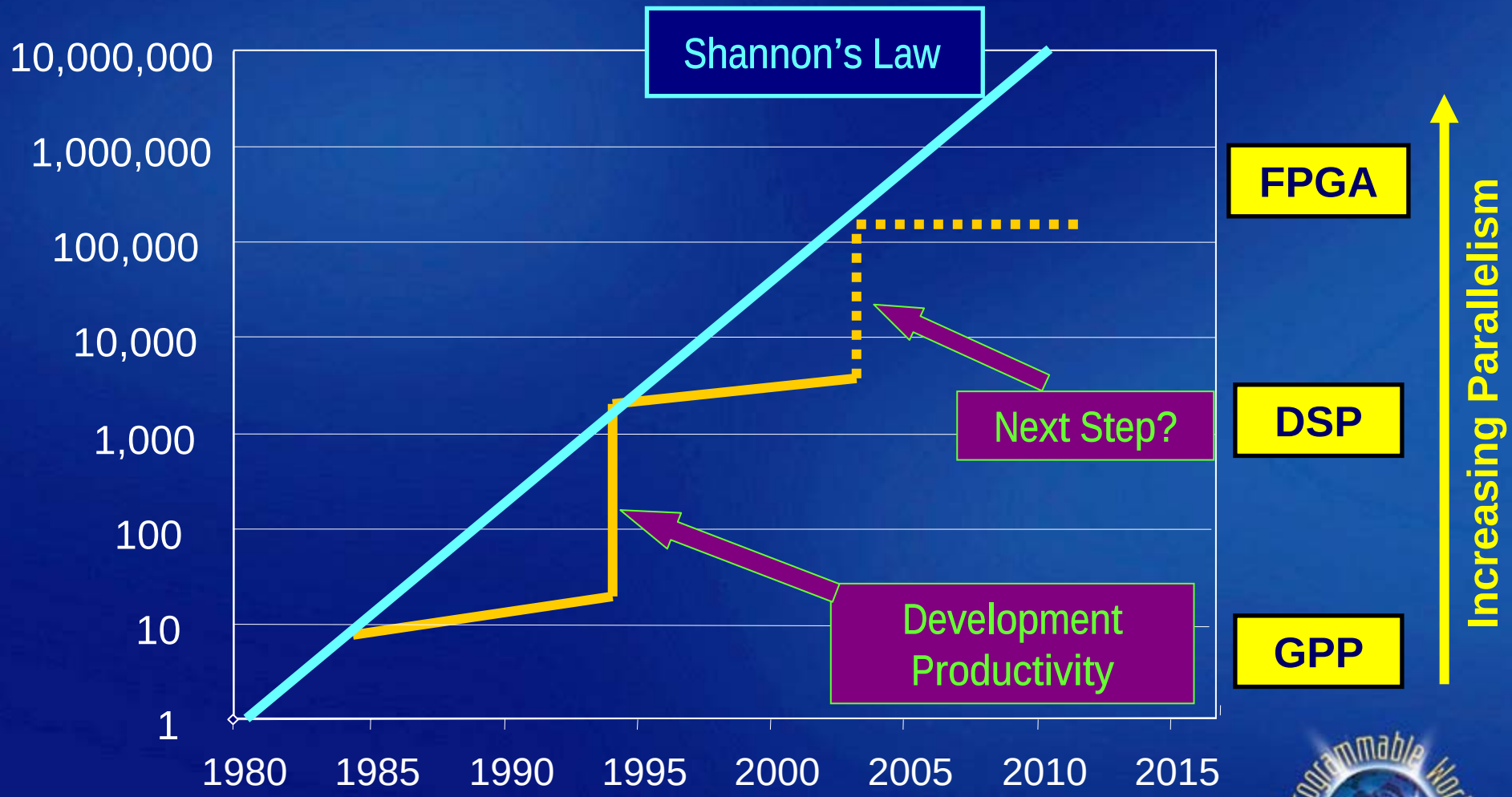
FPGA

- Extremely High Performance
  - Massive Parallelism
- Reconfigurable Hardware
- Exceeds Moore's Law
- Different density devices
- System Integration
  - Platform FPGA

DSP Processor

- High Performance
- Software Programmable
- Pervasive - Legacy code
- Decision/Control
- Low Power
- System Integration
  - OMAP

Development Tools and IP Cores Drive Productivity Gains



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Extensive IP Core Library to Accelerate Productivity

- Basic Elements
  - Addressable shift register (SRL16E), converter, counter, delay element, up/down sampler, multiplexer, register, parallel to serial & serial to parallel converter, etc
- Math functions
  - Accumulator, adder/subtracter, serial multiplier, inverter, logical, sine/cosine table, scale, negate, relational, CORDIC
- Memory
  - Dual and single-port RAM, FIFO
- FFTs
  - 16 - 32K point complex FFT
- Filters
  - DA FIR filter, CIC filter, Multi-channel FIR filter
- Forward Error Correction (FEC)
  - Reed-Solomon encoder/decoder
  - Convolutional encoder
  - Viterbi decoder, general purpose (puncture/de-puncture)
  - Viterbi decoder, 802 Compliant
  - Interleaver/de-interleaver
  - TPC Encoder/Decoder
- Direct Digital Synthesizer

Exceptional Performance of Xilinx LogiCORE™ Products

- Verified IP Core Library Metrics:
  - World's Fastest Viterbi Decoder (k=7) - 203 Mb/sec
  - TPC Decoder - 155 Mb/sec (802.16, 802.16a)
  - CDMA Turbo Convolutional Codec, 3GPP2 compliant
  - Reed Solomon Decoding to 10Gb/sec rates
  - Universal Modulator (J83 Annex A, B, C)

Extreme performance with minimal design effort

http://www.xilinx.com/dsp

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Traditional Design Flow for High-End Signal Processing

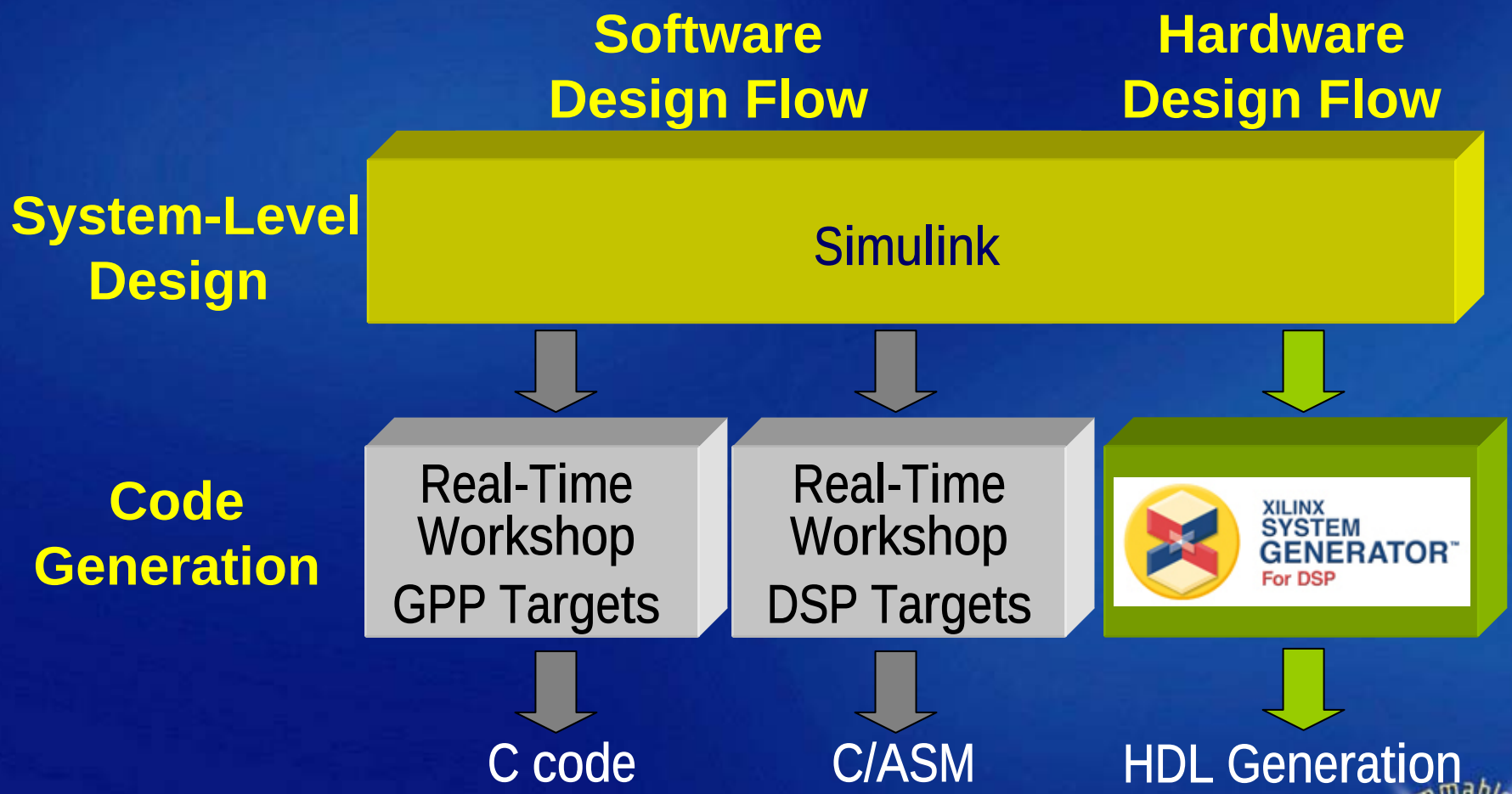
	DSP Designers Traditionally Used	FPGA Designers Traditionally Used
Languages	MATLAB C, C++, Assembly	VHDL, Verilog
Tools	DSP Development Systems	FPGA Place & Route
Debug	Debuggers - Mature	JTAG Probes/ChipScope

What DSP Designers Told Us

- High-level System Language
- Insulation from low level FPGA implementation
  - VHDL, Verilog, P&R, Bit-streams
- Common IDE for DSP & FPGA development
- Ability to tie in (legacy/new) HDL from FPGA designer
- Simple debug using hardware in the loop (akin to DSP development systems)
- Simulation models need to map 1:1 with hardware solution

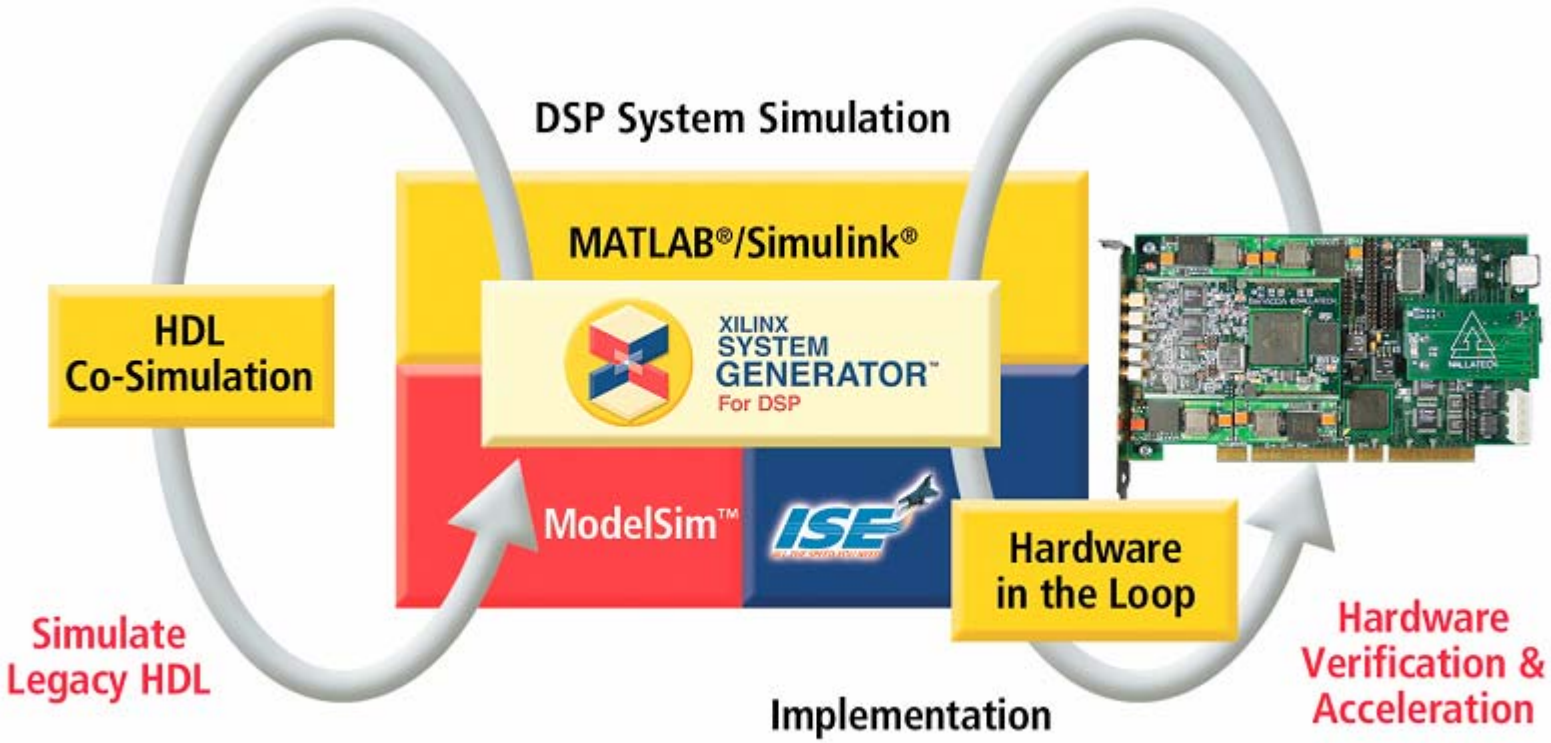
Tomorrow's Systems DEMAND a highly Integrated Development Environment (IDE) for maximizing DSP system performance

Simulink - A Unified IDE for System-Level Design



Simulink is a registered trademark of The MathWorks

System Generator™ for DSP



Simplifying System Level Design for FPGA based DSP Systems

http://www.xilinx.com/systemgenerator_dsp

10-Minute Demonstration

- Demo1
  - 16-QAM demodulator with packet framing
  - Use of Xilinx PicoBlaze 8-bit microcontroller in the receiver
  - Using hardware co-simulation capability of System Generator for DSP
- Demo 2
  - Modeling of slave OPB* peripheral using Simulink & System Generator for DSP
  - Simple DA FIR Filter implemented on Virtex-II Pro FPGA
  - PowerPC is used to control filter coefficient reloading

See Xilinx Application Note: XAPP264 for more information
http://www.xilinx.com/xapp/xapp264.pdf

* On-chip Peripheral Bus (OPB)

Demo Key Messages

- Simulink is a unified IDE for high performance DSP system design
  - High level of abstraction
  - Seamless Integration of FPGAs, DSPs, GPPs
  - Data path and control path can be implemented on Xilinx FPGAs using System Generator for DSP
  - GPPs on Xilinx FPGAs include:
    - Hard Embedded GPP - PowerPC™ 405 (420 DMIPs)
    - Soft GPP - MicroBlaze™ (100+ DMIPs)

PowerPC is a registered trademark of IBM Corporation

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Spartan-3 Pricing Enables New Applications

- 276 BMACs/s performance* for $100** (3S4000)
- Data Path - Rich DSP Fabric
  - 104 embedded multipliers, SRL16 logic, 1.8Mb of memory
  - 60+ DSP algorithms built as IP Cores
- Control Path
  - MicroBlaze processor for control path
    - 68 DMIPs at 85 MHz

Enables Customer-Premises Equipment, Consumer, Automotive, Industrial Control Type Applications

* 8-bit MAC ** 2004 projections for 250Kunit volumes

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Summary

- Algorithmic complexity is outpacing Moore's Law
- FPGAs are the solution for extreme performance DSP applications
  - Often in conjunction with a DSP processor
- IDE available today enables DSP designers to target FPGAs
- New Spartan-3 FPGA family reduces cost for high performance DSP and enables new applications

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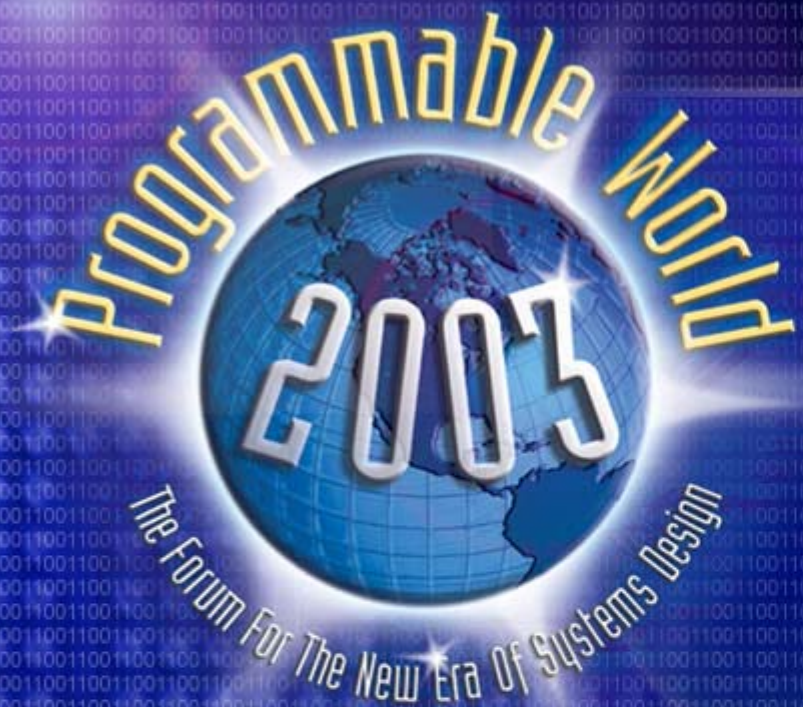

Thank You!

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