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Programmable Systems Transform the Design and Implementation of Adaptive Optics Systems Platform

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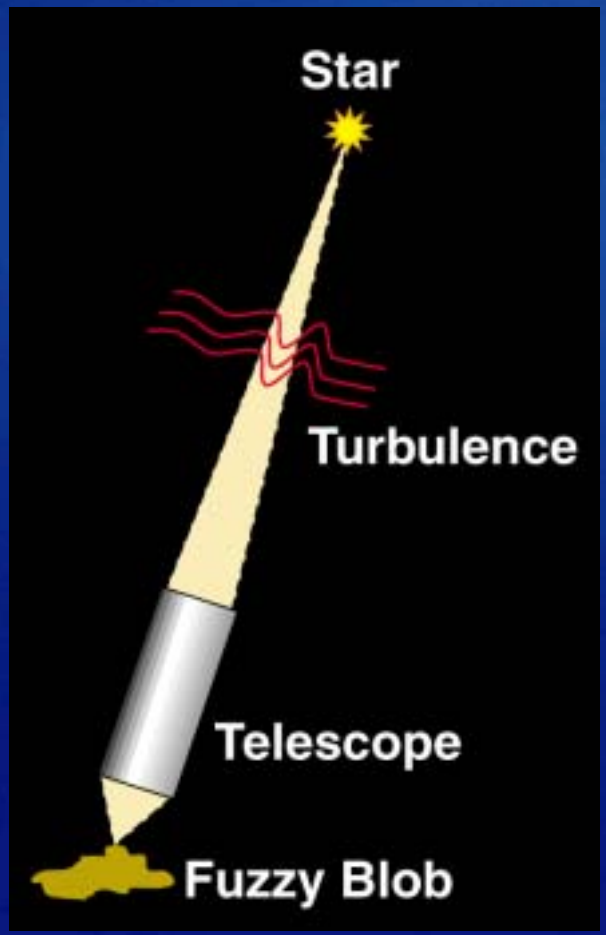
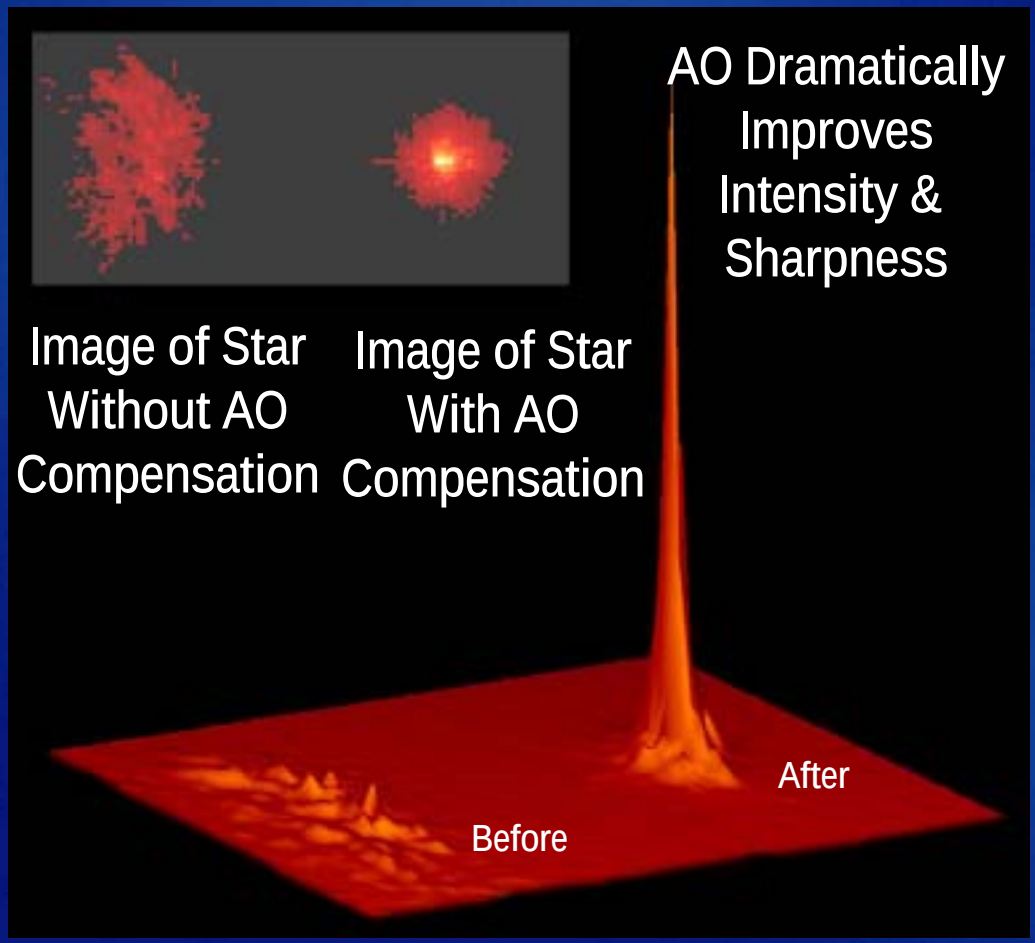
Adaptive Optics Primer

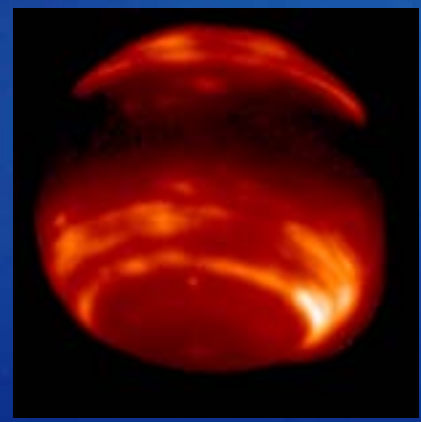


- The Earth's Atmosphere Is Not a Homogenous Medium
- Turbulence Causes Index of Refraction To Vary Both Spatially and Temporally
- Light From a Point Source Is Spread Out and Distorted
- Images Collected By The Telescope Lack Clarity and Detail

AO Processing Corrects For Atmospheric Effects



Neptune Without AO

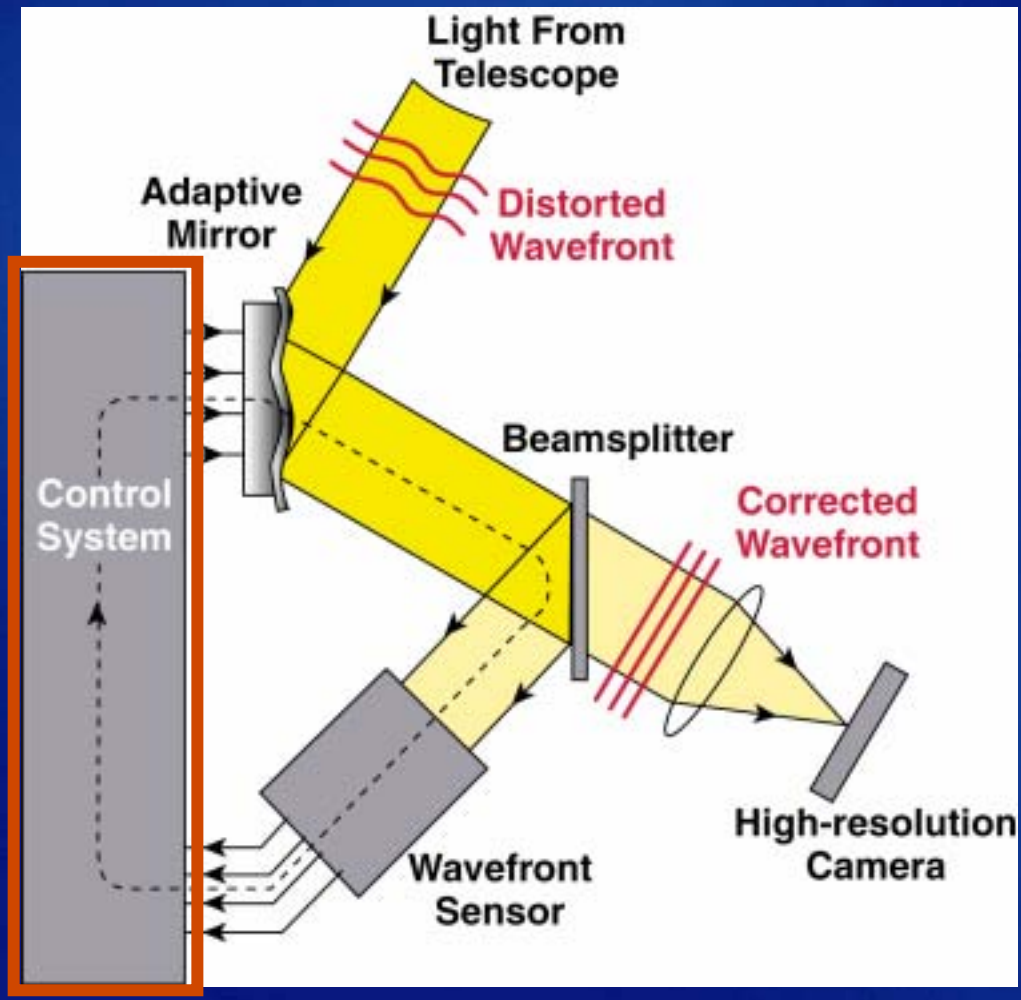


Neptune With AO

Why AO Is Important …

- Astronomers Use AO To Improve The Resolution of Large Ground Based Telescopes
  - Without AO, Giant Telescopes Resolve No Better Than Something You Can Buy At a Department Store
  - With AO, They Can Outperform Hubble
- Laser Communication Systems Use AO To Increase Range and Reduce Bit Error Rates
- Mil-Aero Programs Employ AO For Many Reasons
  - High Resolution Reconnaissance and Surveillance
  - Precision Targeting, Tracking, and Engagement
- FPGA Technology Can Bring a Dramatic Cost Reduction To The Application of These Systems

Real-Time AO Control System



- Wavefront Sensor (WFS) Measures Distortion
- Control System Processes WFS Data To Drive Mirror System
- Adaptive Mirror Applies Conjugate of The Distortion
- Real-Time, Closed Loop, Image Processing System

Today We Will Construct a "Simple" AO Processor System

- Turbulence Degrades Wavefront In Many Ways
  - Low Order Effects Cause Wavefront to Tilt Back and Forth
  - Higher Order Distortion Effects Distort The Shape of The Wavefront (Coma, Astigmatism, Aberrations etc.)
- Designing a Tilt Correction System Using Virtex-II Pro
  - Tilt Causes The Image To Dance Around
  - While The High Resolution Camera Is Exposing The Image, The Dancing Motion Blurs Fine Detail
  - To Correct The Dance, The Adaptive Mirror Is "Steered" At High Speed to Keep The Object Centered In The Camera

AO Image Processing Characteristics

- Streaming Based Flow of Image Pixels
- KHz Imaging Frame Rates
- Repetitive, Systolic Number Crunching
- Processing Algorithms Are Multiply-Accumulate Based
- High Data Rates Are The Processor Design Driver
- Need High Throughput With Low Latency

An Excellent Fit For Xilinx FPGA Technology

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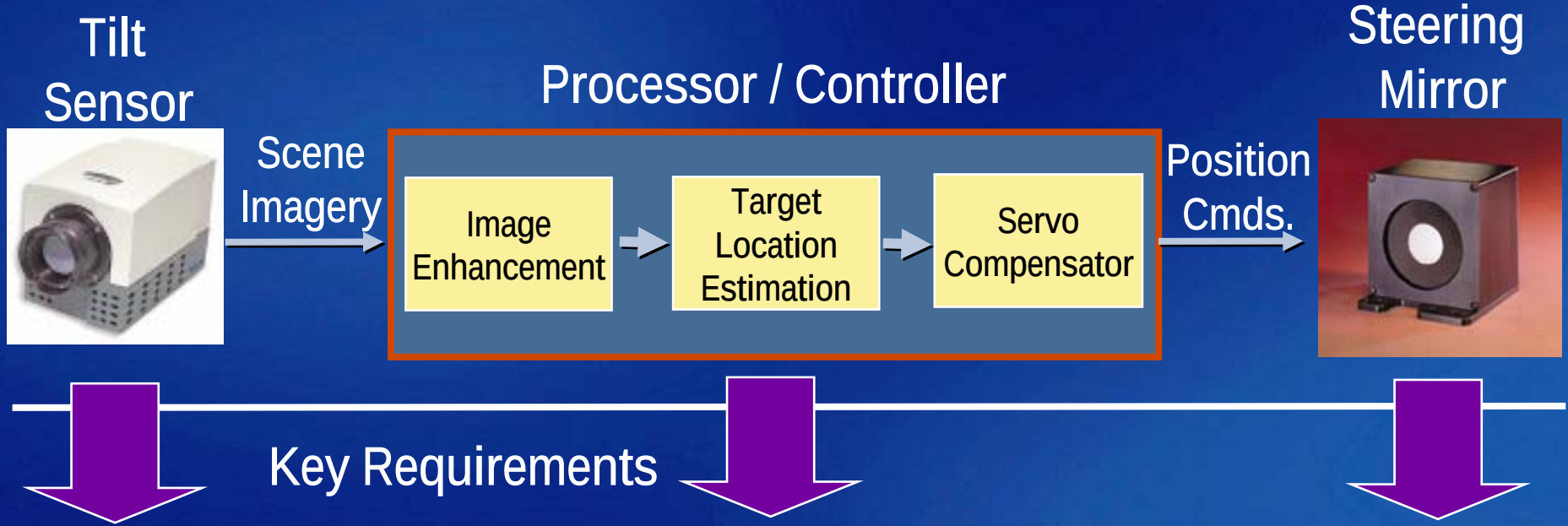
Data Flow Diagram Of Processing Functions



Key Requirements

- 6000 Frames Per Second
- 128x128 Pixel Array
- 12 Bit Data Samples
- Fiber-Optic Output
- RS232 Control Port

- Object Centroiding
- Closed Loop Mirror Control Loop
- Sensor Interface / Control
- Video Display Generation
- 16 Bit D/A Output
- Low Processing Latency, Small Package

- Analog Position Interface (Azimuth / Elevation)
- RS232 Command and Control Link

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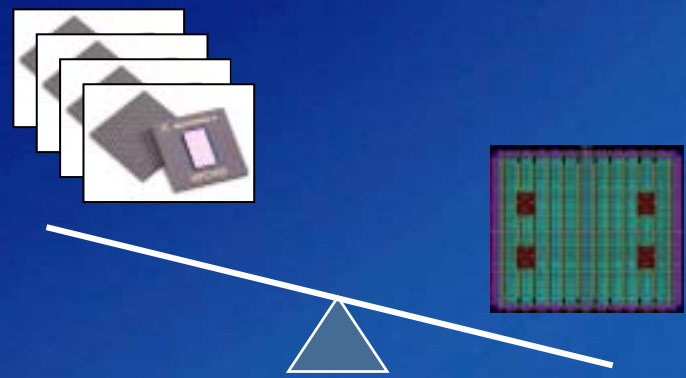
Processor Design Tradeoffs

- Multi-Processor, S/W Based Architecture
  - Readily Available Commercial Boards
  - "S/W Based Processors Are Easier To Program"
  - Larger Package, Based Upon Multiple Boards From Multiple Vendors
  - Limited Parallelism, Determinism, Interface Capabilities
  - Weight, Volume, Power
- Platform FPGA Approach
  - Significantly Simpler H/W Design
  - Improved Performance, Determinism, Latency
  - Tremendous I/O and Interface Flexibility
  - "FPGA Programming Is Hard"
  - Ideal Configuration Encourages Build to Print Solution = Cost + Risk



Platform FPGA Best Addresses Our Packaging and Performance Requirements

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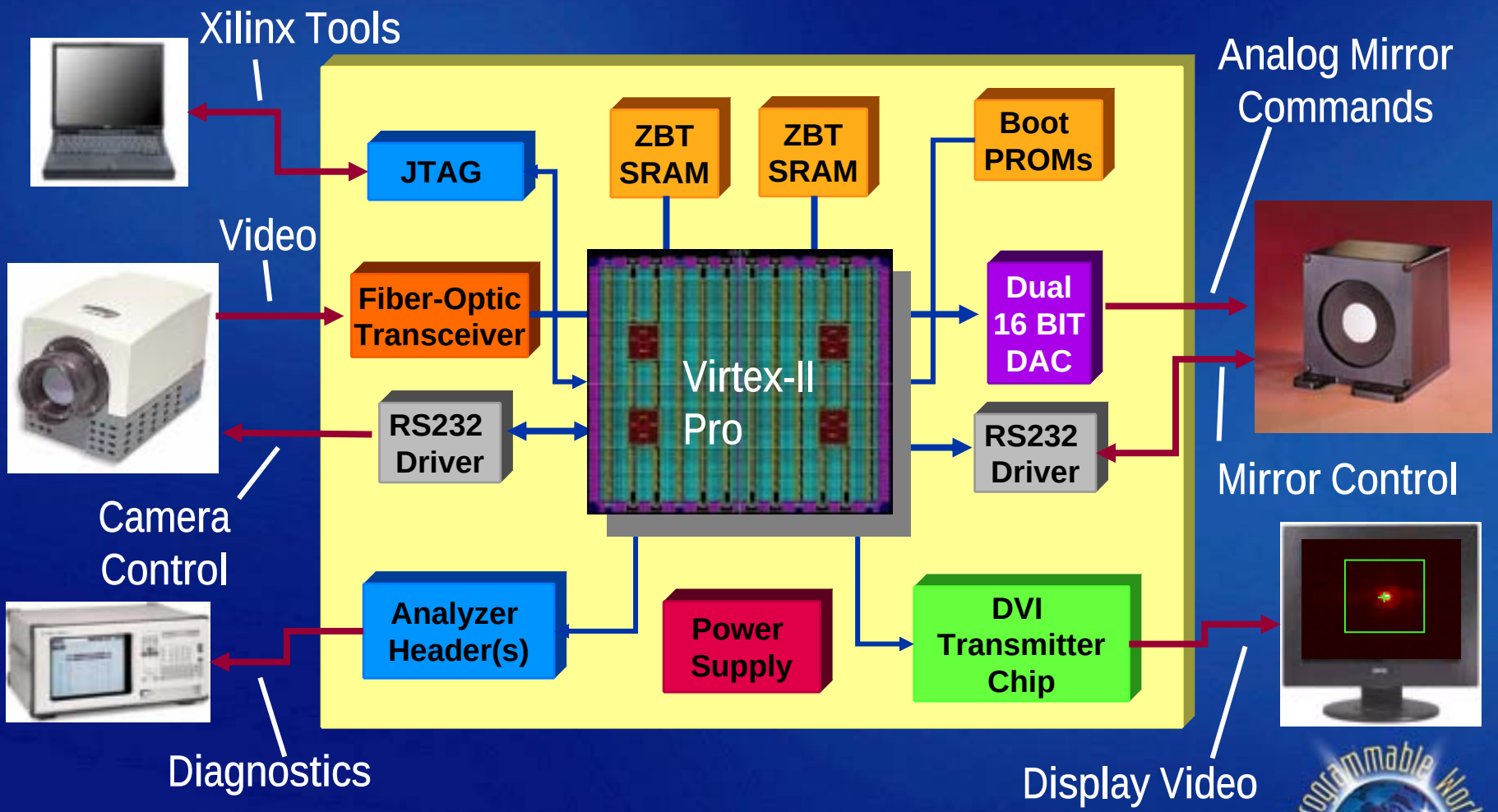
Why Choose Xilinx ?

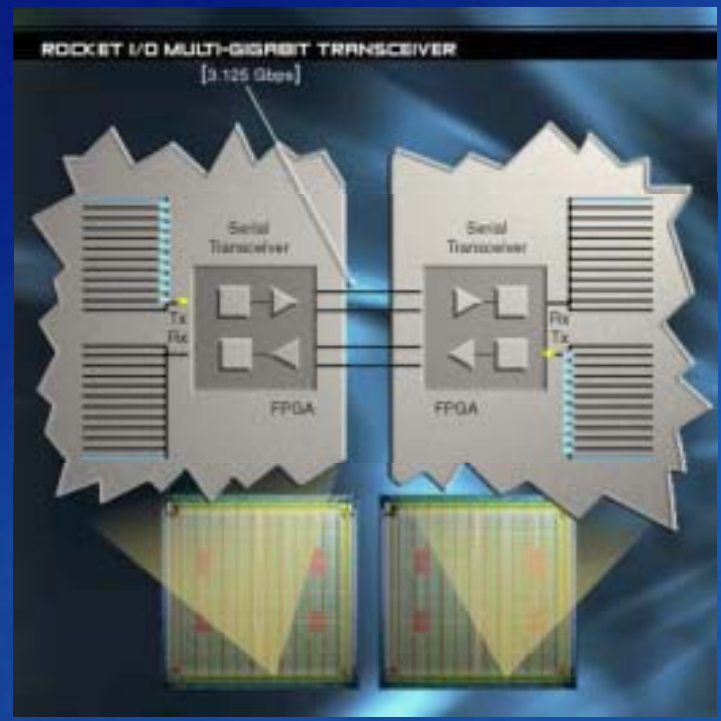
- Boeing's View on FPGA Tradeoffs
  - Many Capable Devices Exist For The Job
  - Still Primarily a Xilinx vs. Altera Trade
- Why We Choose Virtex-II Pro Over Stratix
  - Virtex-II CLB Is a Better Fit For Our DSP Applications
  - Stratix Has No Embedded Microprocessor Core
  - Stratix Advantages Aren't Enablers For Most Of Our Apps
  - Broad V2-Pro Family Supports Diverse Applications
  - Commercial FPGA Board Vendors Mostly Use Xilinx
  - Xilinx Offers Unique DSP Design Tool Capabilities
  - Xilinx Customer Support Has Helped Us to Succeed

Creating a Processor Solution Around V2-Pro



Addressing The Image Data Transfer Problem

- Our Processor Must Interface to a Serial Fiber-Optic Data Link
- This is a “Transfer Pixels From A to B” Problem
- Low-Latency and Protocol Simplicity Are Highly Desired
- Fiber-Channel, Rapid-I/O, 1394b Are “Overkill”
- Prefer a Programmable Serial Transceiver to “Keep It Simple”



MGTs Are A Nice Match For This Application

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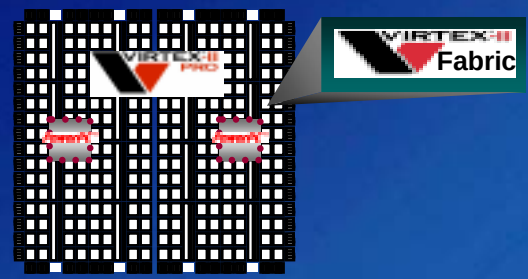
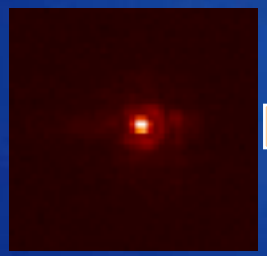
Addressing The DSP Algorithm Challenge

- Tilt Correction Processor Functions
  - Programmable 2D Image Convolver
  - Image Statistics and Thresholding
  - Computation of Intensity Center of Mass
  - Low-Latency Encourages Assembly Line Approach
- V2-Pro Features That Benefit This Application
  - Embedded Multipliers Allow Single Clock Cycle Execution of The Convolver and Centroid Computations (True Parallelism)
  - Block RAM Offers Configurable, Video Delay Line Buffers
  - SRL16 Yields Programmable Filter Coefficients and Logic-Efficient Delay
  - “Free” Pipelining Via Abundant Flip-Flops and LUT RAM

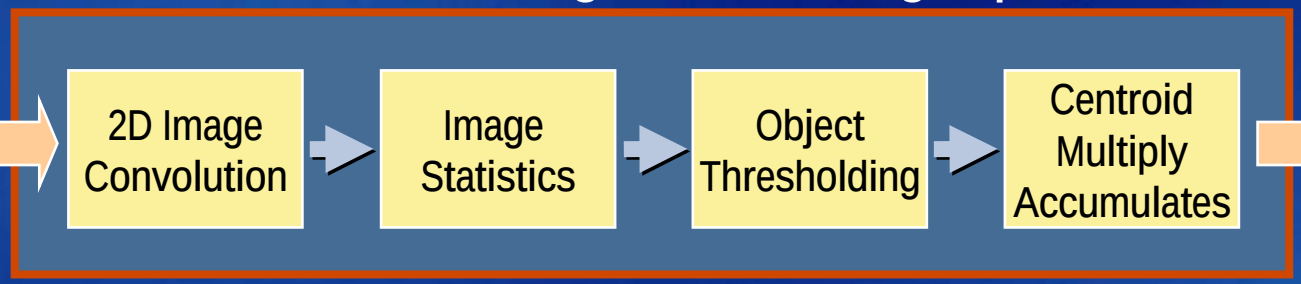


High-Level Modeling Of The Pixel Processing

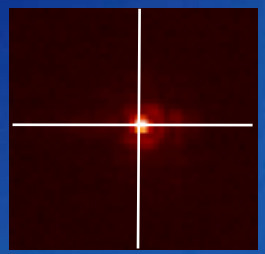
Input Image

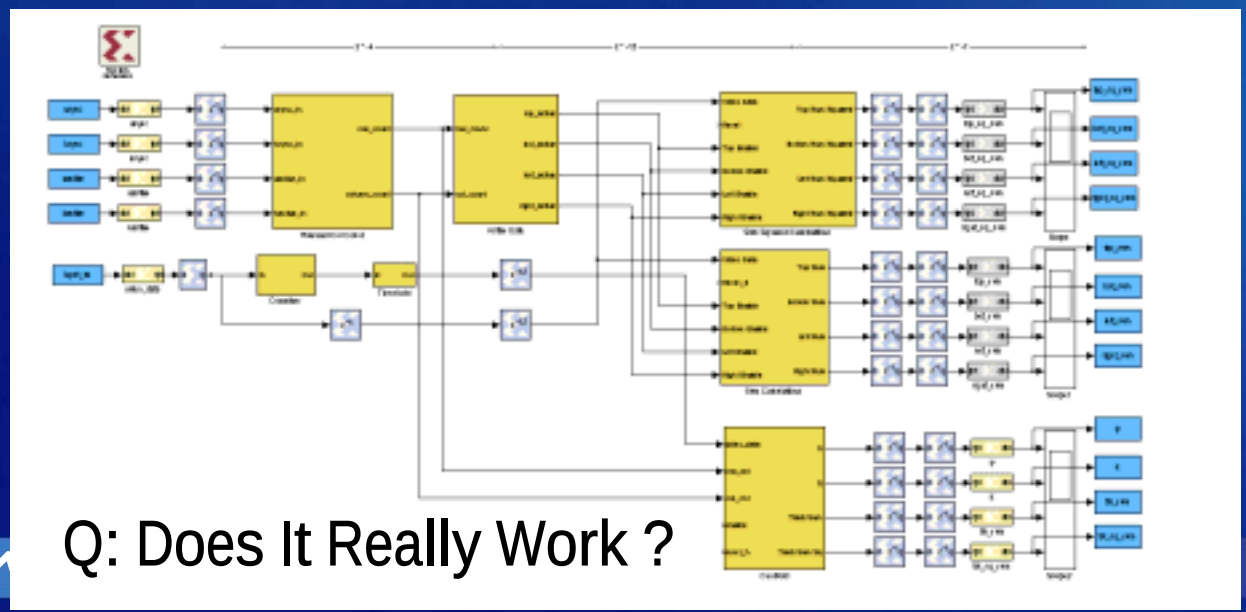


Tilt Corrector Image Processing Pipeline



Centroid Position

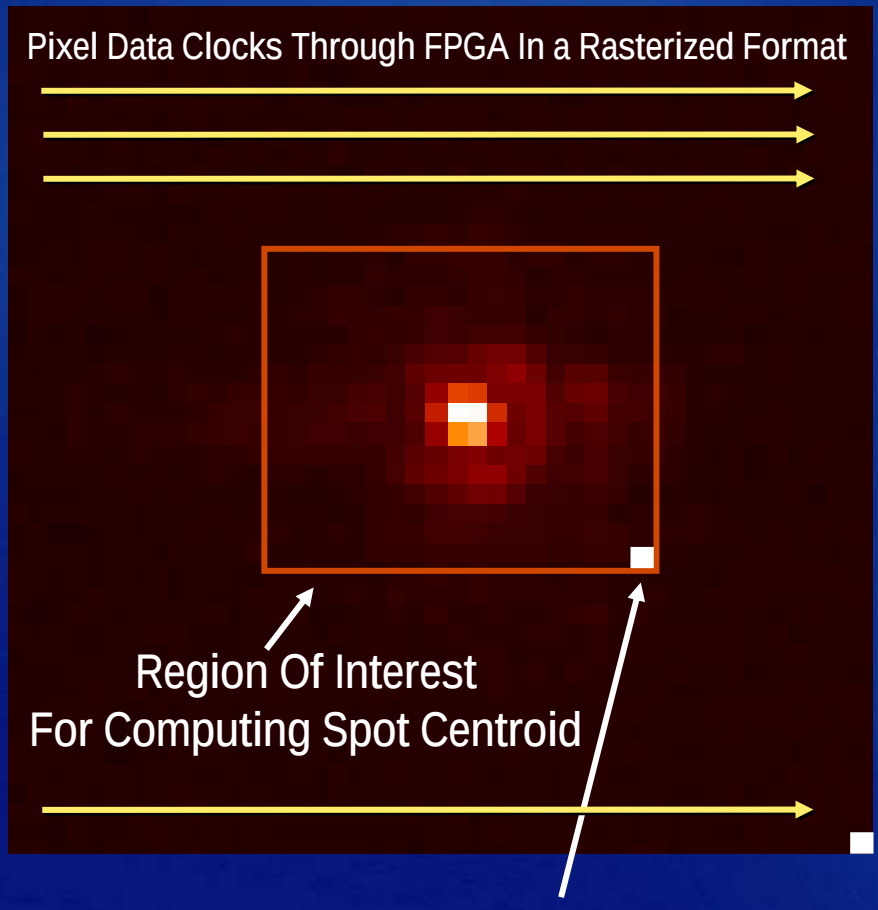




Q: Does It Really Work ?

System Generator Model Of Pixel Processing Functions

FPGA Approach Minimizes Processing Latency



- Image Data Is Processed As It Clocks Into The FPGA Pipeline
  - No Buffering, Frame Grabbing, DMA to Memory etc.
- Target Location Available As Soon As Last Pixel Has Clocked Through The Pipeline
- Reduced Latency = Higher Control Loop Bandwidth
  - Reject More Image Dancing

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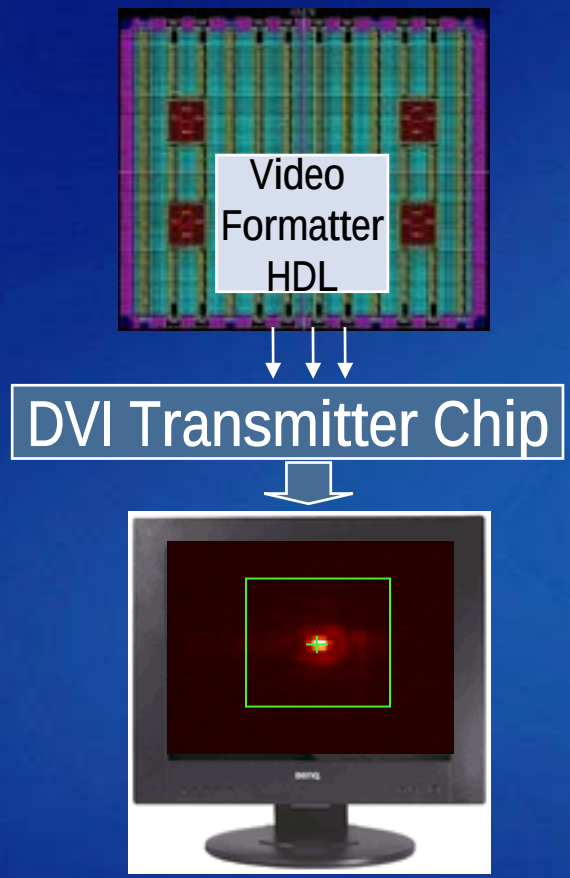
V2-Pro Allows Concurrent Graphics and Processing

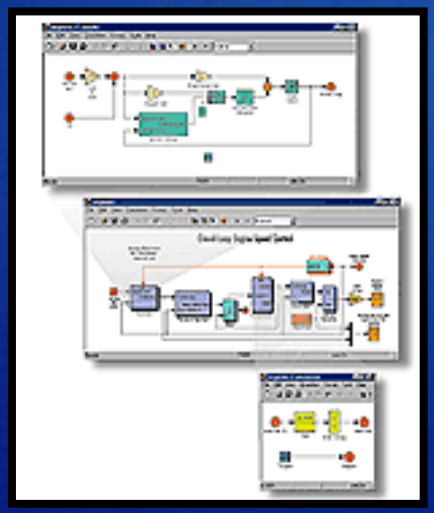
- Video Formatter Takes Input Video Stream and Passes It On To a DVI Transmitter Chip
  - Eliminates Need For a Dedicated Graphics Display Card
- FPGA Processing is Fully Parallel
  - Video Formatter Doesn't "Influence" Pixel Processing Pipeline
  - Mitigate Bus Contention When Using a Multi-Board, Multi-Processor Approach



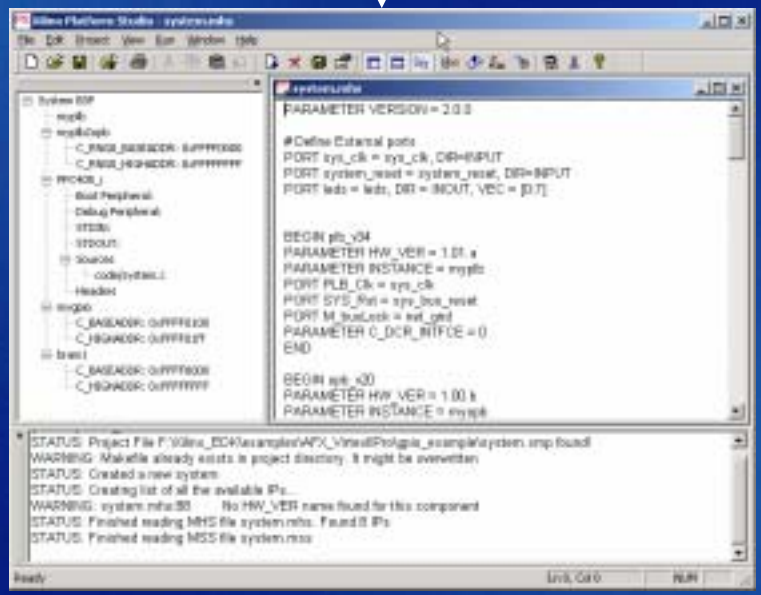
We Still Need a Servo Control Loop ….

- Servo Compensator Processes Object Centroid and Derives Commands to Move The Steering Mirror
  - Feedback Loop Used to Keep Object Centered Within The Image
- These Are Not Computationally Intense Functions
  - Much Better Fit to Software…
- Virtex-II Pro Gives Integrates This Back-End S/W Capability Via The PPC 405
- Mathworks Offers Tools To Efficiently Develop Control Systems
  - Simulink, Real-Time Workshop, State Flow etc.

Xilinx Platform Studio Provides S/W Integration



Simulink Control System
And Application C Code



Required Peripherals For PPC System

Application Object Code

Netlist For PPC And Peripherals

Integrate Output With Our SysGen and VHDL “Plumbing” Using The ISE Design Environment

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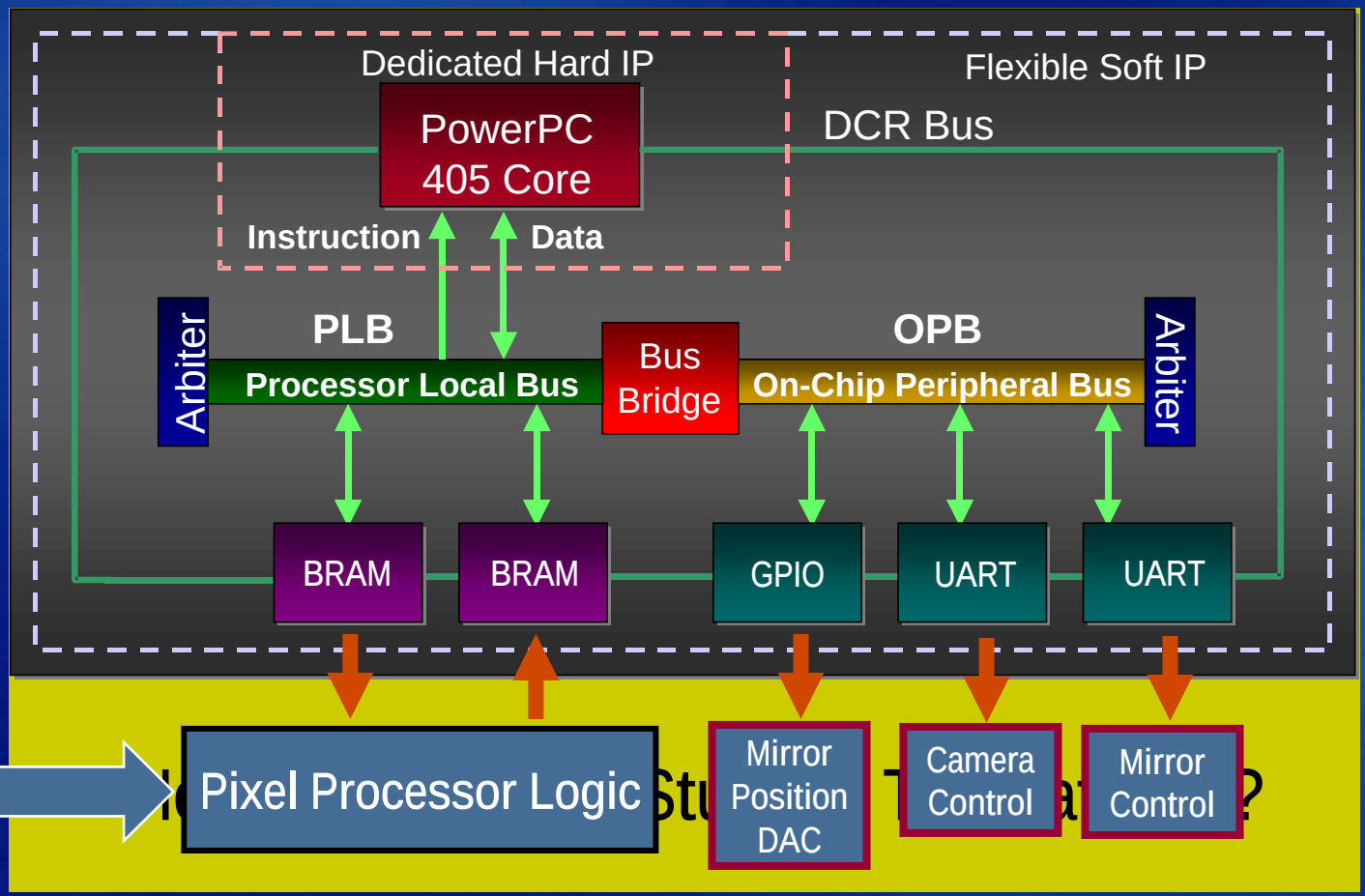
Integrating The PPC Core With Our FPGA Application



We Use Xilinx S/W Libraries to Complete The Design

- Xilinx EDK Includes Key Items Needed to Build a Functional, Embedded Micro-Controller
  - Boot Code, Device Driver S/W, Network Stack, Lightweight Kernel etc.
- GPIO, UART, BRAM, 405 Bus Interfaces Are Graphically Configured Via Platform Studio
- User Concentrates Primarily On The Development of Application C-Code

Summary

- Platform FPGAs Are An Excellent Fit to Adaptive Optics
  - Our Example Applies To The More Complicated, High-Order Wavefront Processing
- Virtex-II Pro Enables a Complete, Integrated Processing System
  - A Single Device Can Replace What Once Required a Number of Loosely Coupled Processor Boards
- High Level Design Tools Enable Rapid System Development and Afford Practical FPGA Solutions
  - The H/W and S/W Functions Can Be Readily Applied to Other Programs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