
Agilent Technologies
Programmable World
2003
The Forum For The New Era Of Systems Design
Addressing the Growing Verification Challenge for Highly Integrated Systems
Accelerating FPGA Validation & Debug
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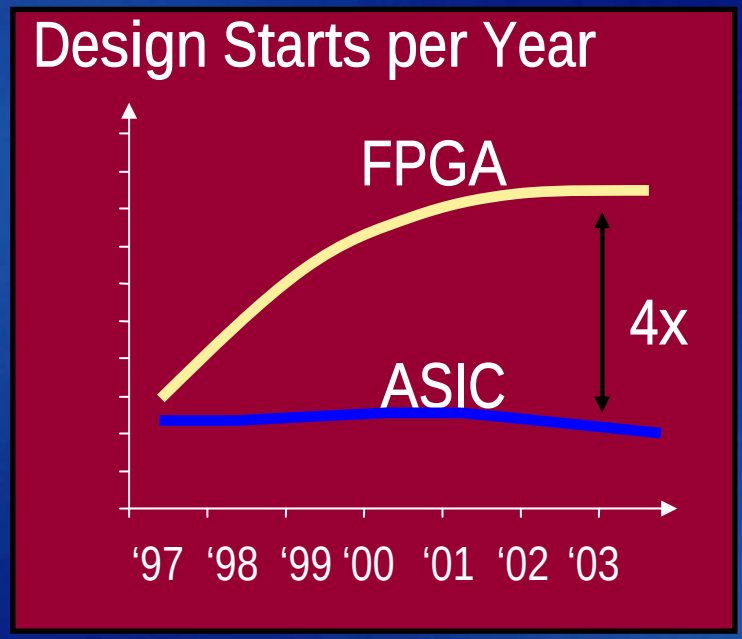
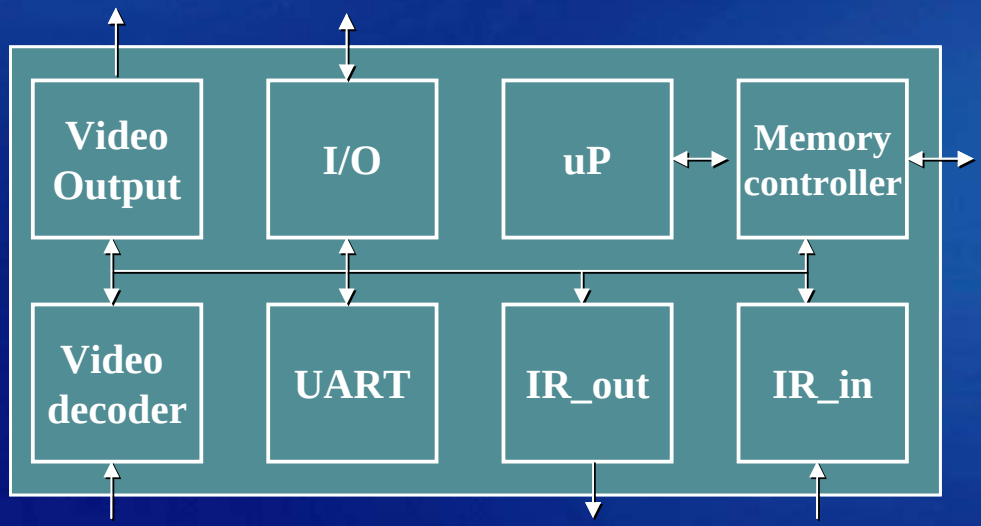
The Move to Programmable Logic



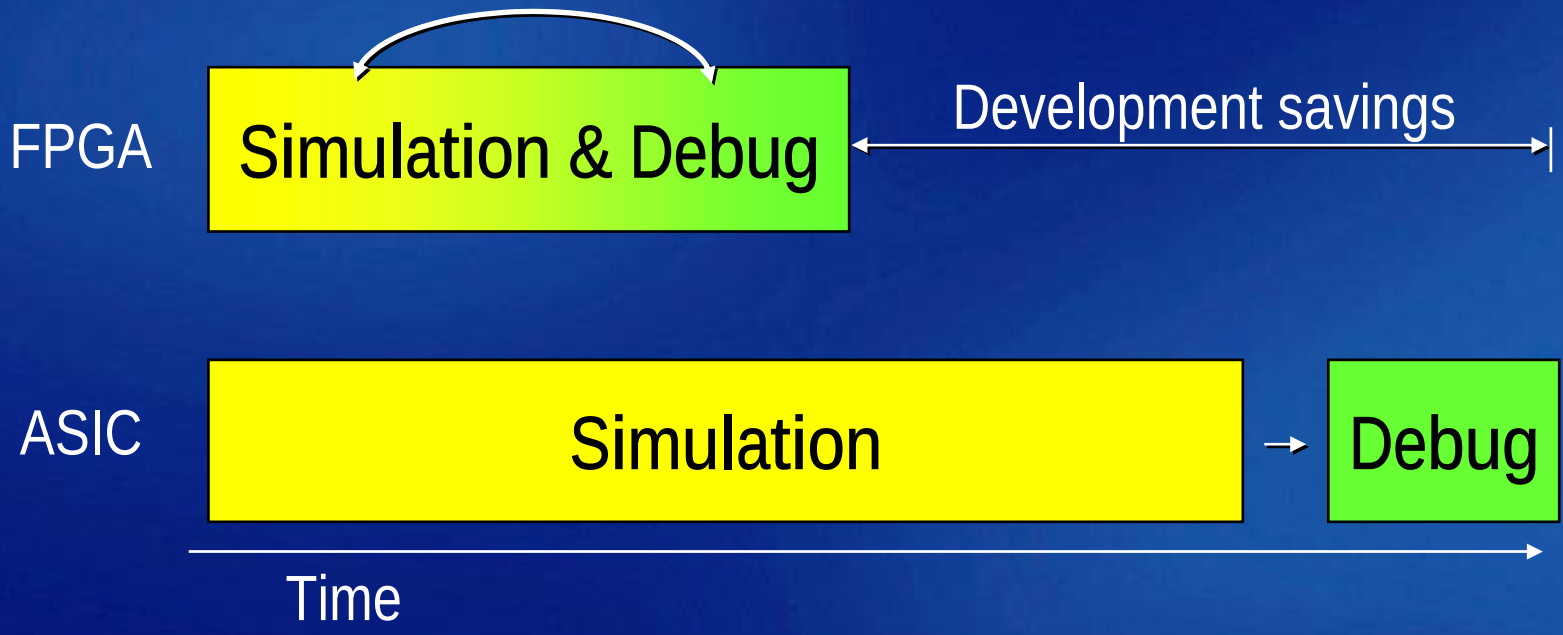
- Fast time to market with lower costs
- FPGA density and features → system integration with advanced capability

Higher Levels of System Integration

- Critical signals are “invisible”
- Complex “embedded” subsystem integration
- Significant HW/SW interaction



Accelerated Validation



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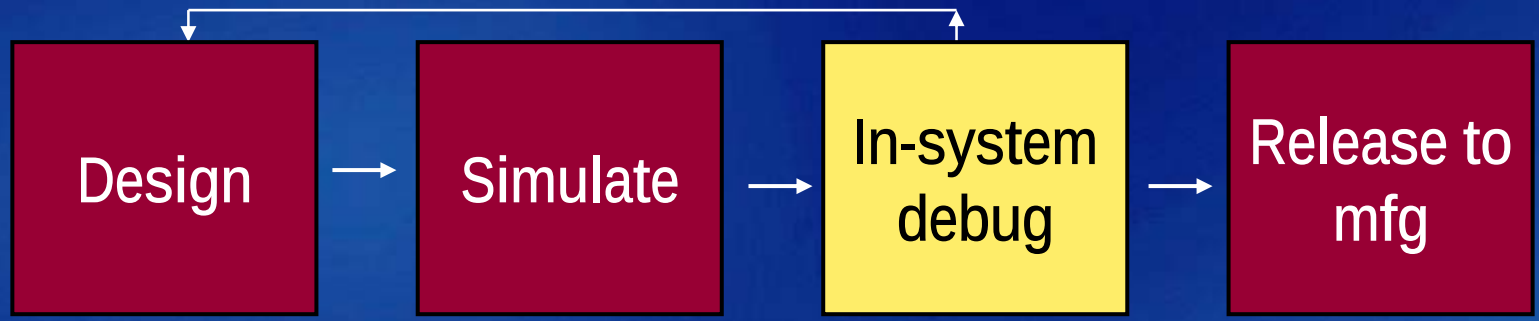
In-system Debug is a Critical Part of FPGA Development

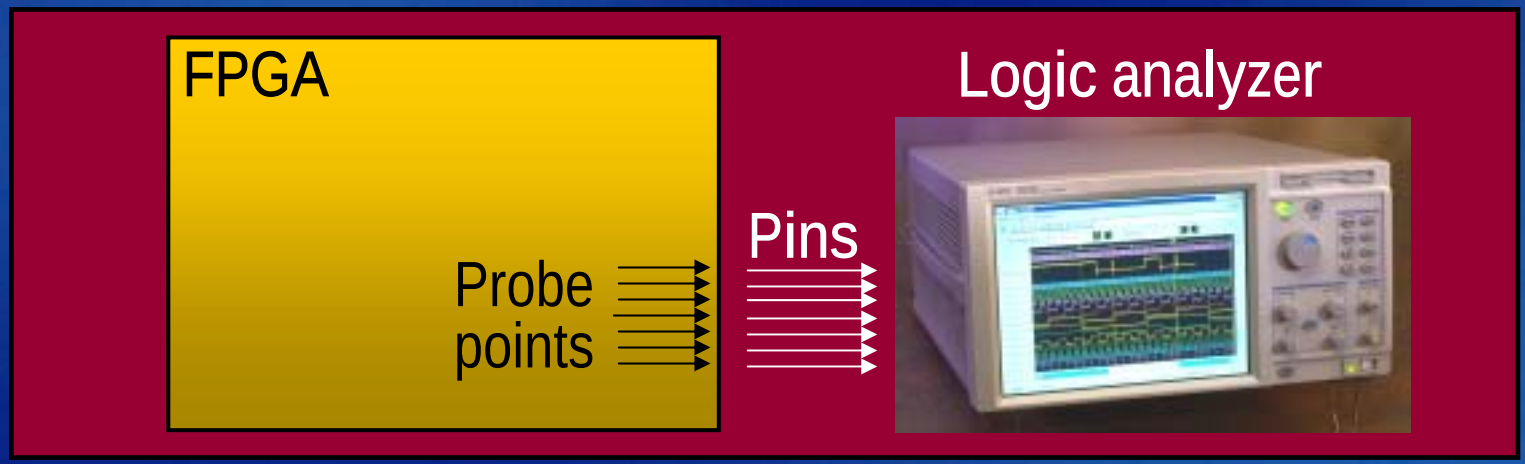


- FPGAs enable better & faster in-system debug and validation than exhaustive simulation
  - Faster: several seconds in-circuit = days of simulation
  - Uncovers problems difficult to simulate
    - Corner cases
    - Interaction with rest of the system
    - Signal integrity effects

What to Consider

- Where are the problems likely to be?
- What visibility will be needed to isolate problems?
- How will you gain access to these signals?
- How will you analyze what's going on?

Route Signals to External FPGA Pins



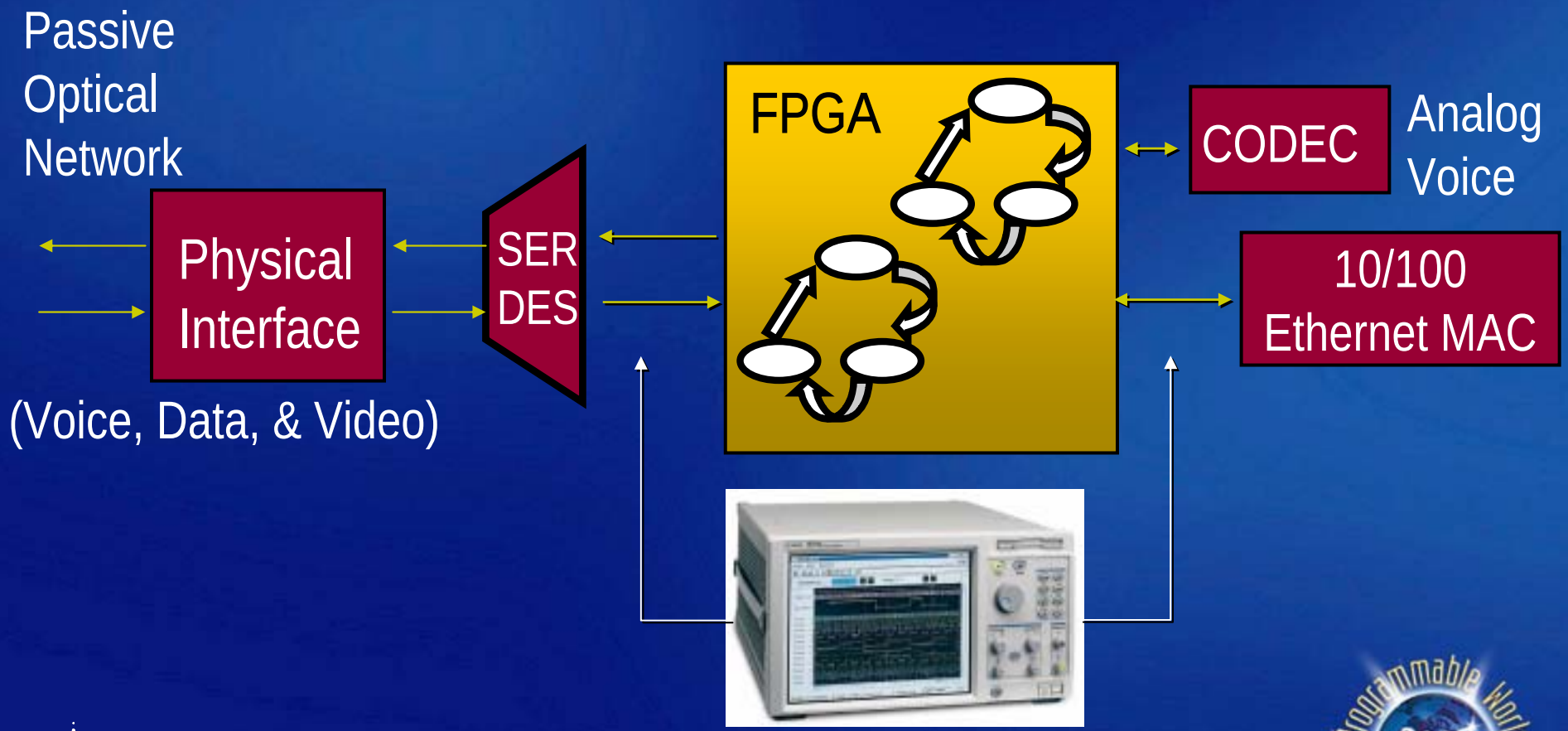
Advantages:

- Deep & wide trace
- Sophisticated triggering
- Synchronous/asynchronous
- System correlation

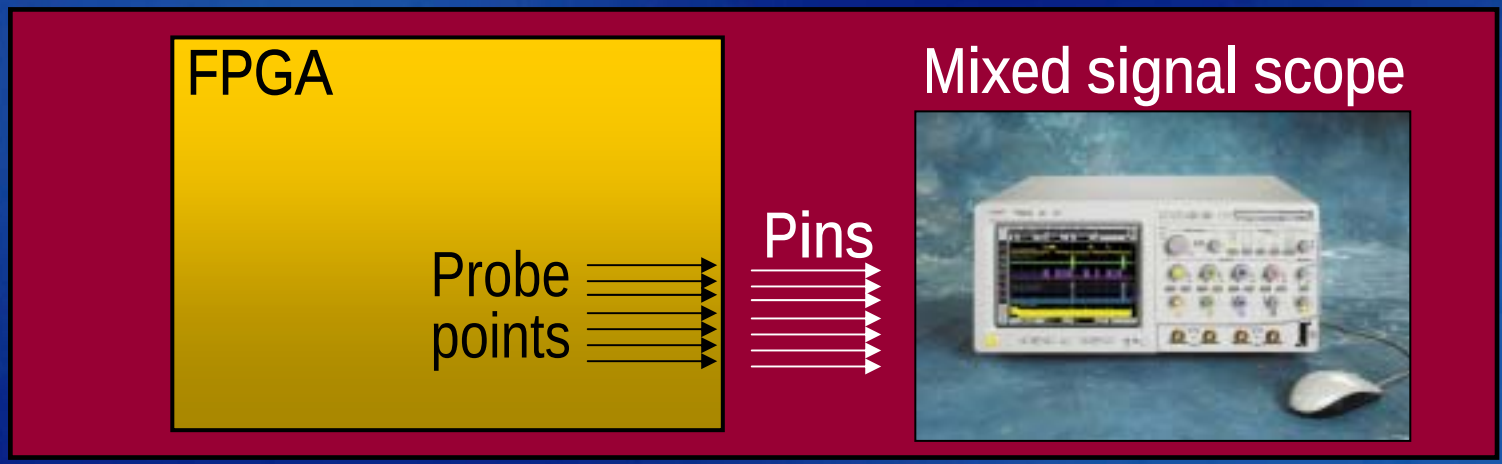
Tradeoffs:

- Consumes pins
- Requires probing planning
- May require re-compile

ATM Access Device Validation Example



Mixed Digital & Analog Analysis



Advantages:

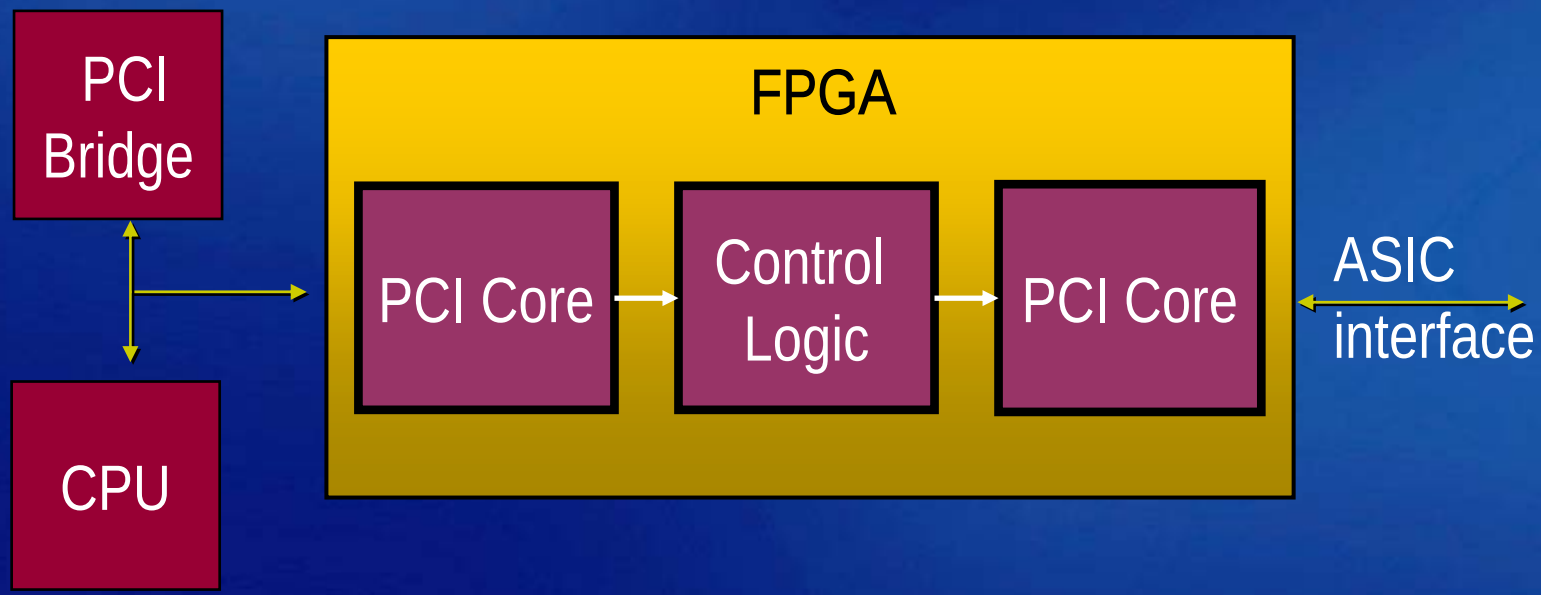
- Analog & digital triggering and capture
- Deep memory

Tradeoffs:

- Asynchronous capture only
- Limited to 20 probe points

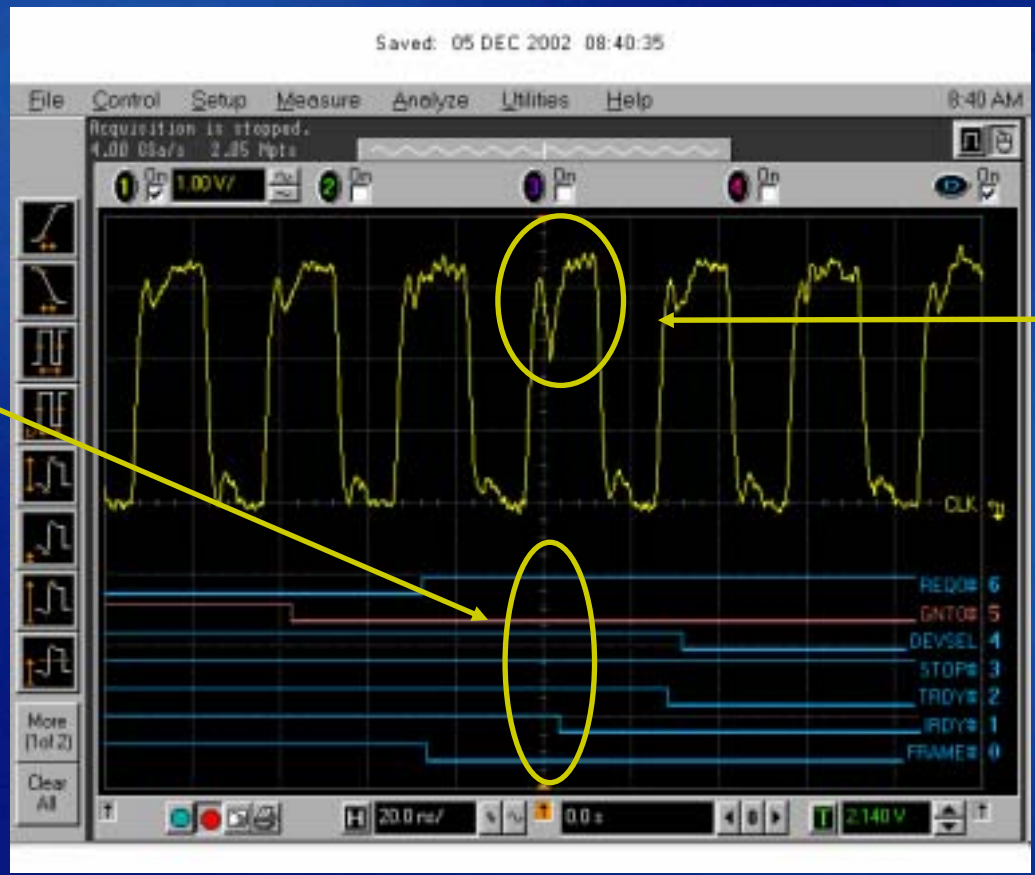
Instrumentation Validation Example

- PCI bus intermittently crashed during CPU writes
- Used SW to exercise numerous PCI modes



Signal Integrity Effects of the Real World

Digital channels provide state trigger



Analog channels see isolated clock coupling

Debug Using FPGA Resources

- Integrated Logic Analyzer (ILA)
- Integrated Bus Analyzer (IBA)
- Virtual IO core (VIO)
- Pin minimization technologies
  - Switching MUX for signal selection
  - Time division multiplexing for pin optimization
    - ILA with Agilent Trace Core (ATC)

Integrated Logic Analyzer

Advantages:

- No pins required
- Inexpensive

Tradeoffs:

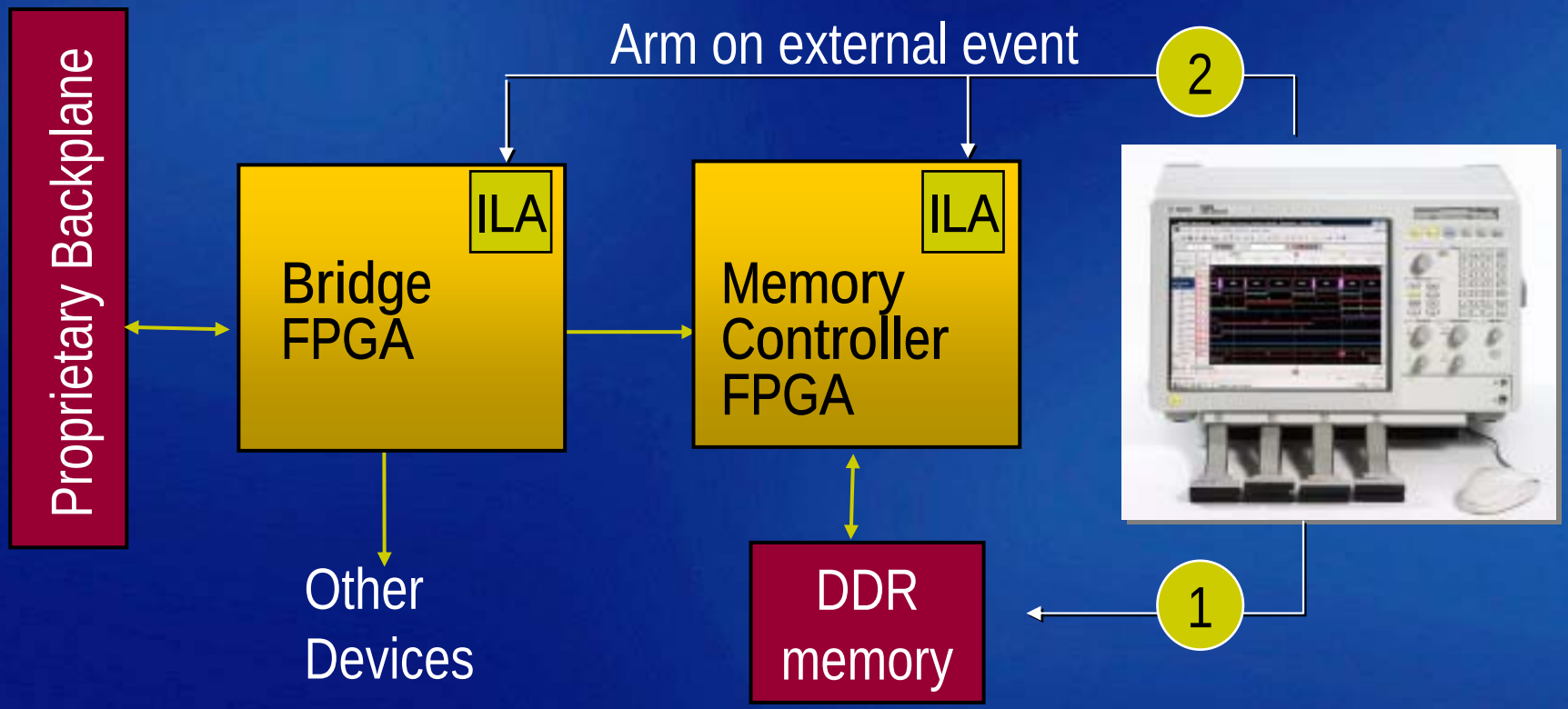
- Consumes FPGA resources
- Synchronous capture only

Deep Memory for ChipScope Pro

Time division multiplexing for greater visibility over a fixed number of pins

- 1x, 2x, and 4x data compression modes
  - e.g. monitor 75 probe points using only 20 pins

ChipScope + Logic Analyzer



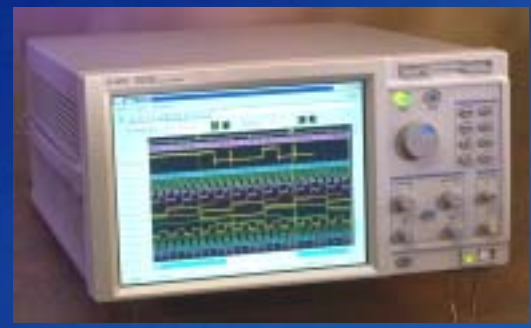
Summary

- Increasing FPGA capability presents new challenges and opportunities for in-system debug and validation
- Design-phase consideration for debug and validation is growing in importance
- Xilinx and Agilent are collaboratively bringing new integrated debug capabilities to market
- The future is bright…!

Useful Links for More Information

- www.xilinx.com/chipscopepro

- www.agilent.com/find/logic



- www.agilent.com/find/scope

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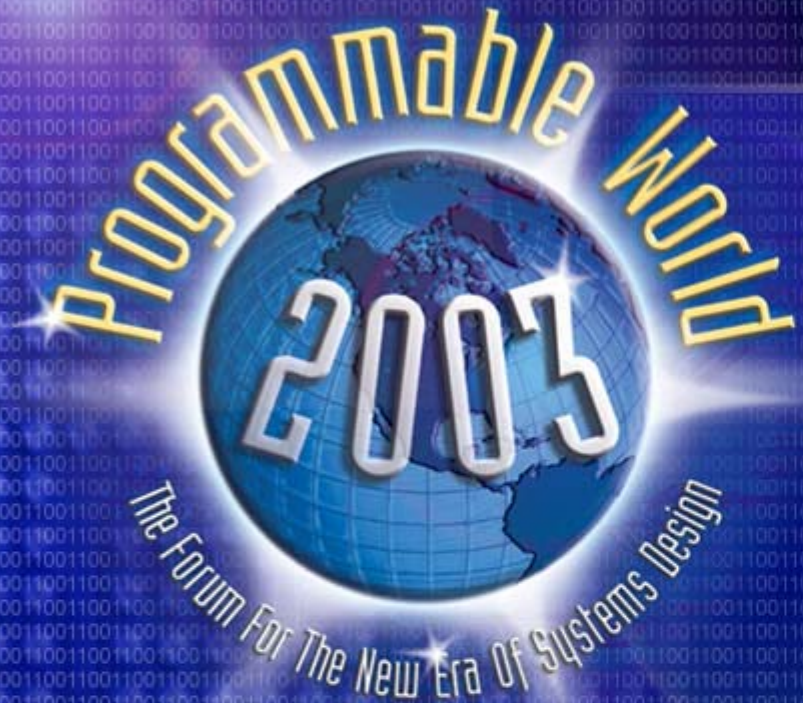

Thank You!

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