Challenges and Design Solutions to Upgrade Existing Systems for Higher Bandwidth (Part 1)

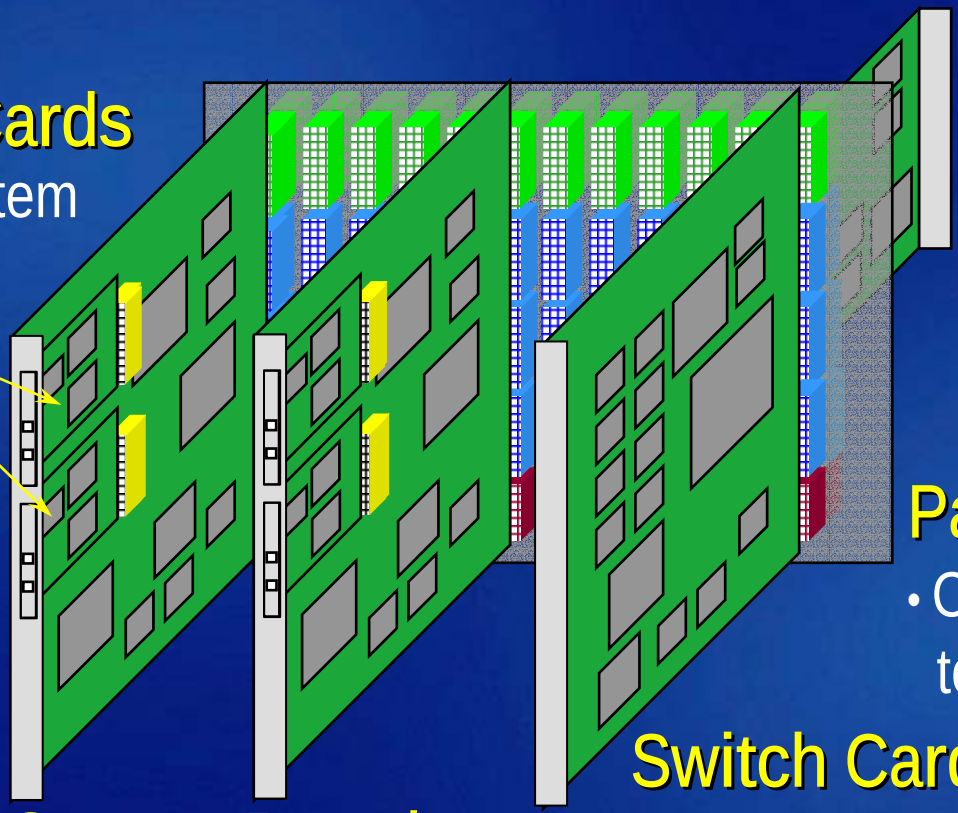
Upgrading vs Replacing

- Reuse Existing Infrastructure
- Shorter Schedule
- Lower Development Cost
- Higher Performance
- Feature Enhancements

Upgrading A System

- Many Aspects to Consider for System Upgrade
  - Power budget
  - Thermal environment
  - Other functional upgrades
- Focus on the System I/O to Improve Data Bandwidth
- Serial Backplane Case Study Example

A Typical Backplane System



Mezzanine Cards
- Configure System Boards for the user's application

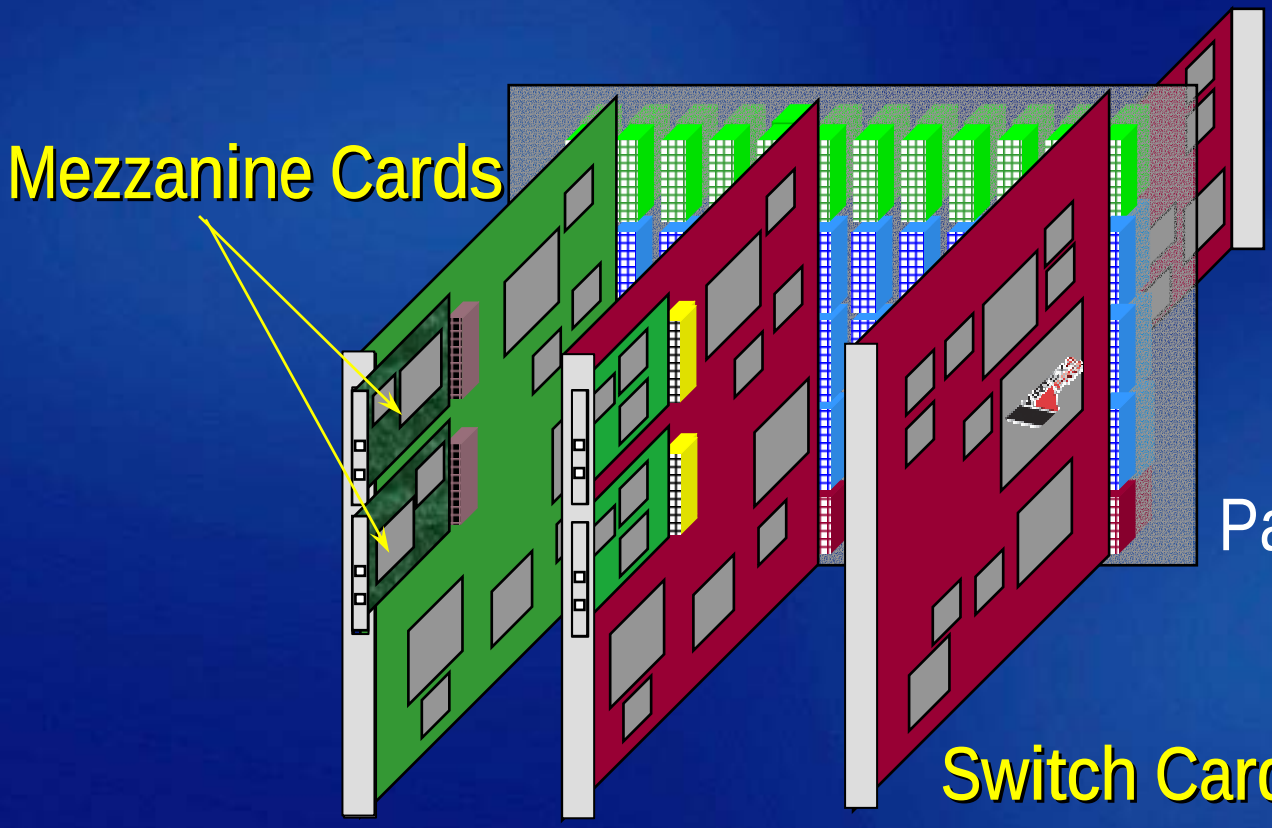
I/O Cards
- Configure system connections to the rest of the world

Passive Backplane
- Connect everything together

Switch Card

System Boards
- Configure the System for the user's application

What Can Be Upgraded?



Challenges

- New Silicon Technology with Existing Connectors and Backplanes
- Signal Integrity and Attenuation Issues
  - Jitter, skin effect, dielectric losses
- Diagnostic Testing and Characterization
  - Interoperability testing
  - Bit-error rate measurements
- Serial Protocol Selection

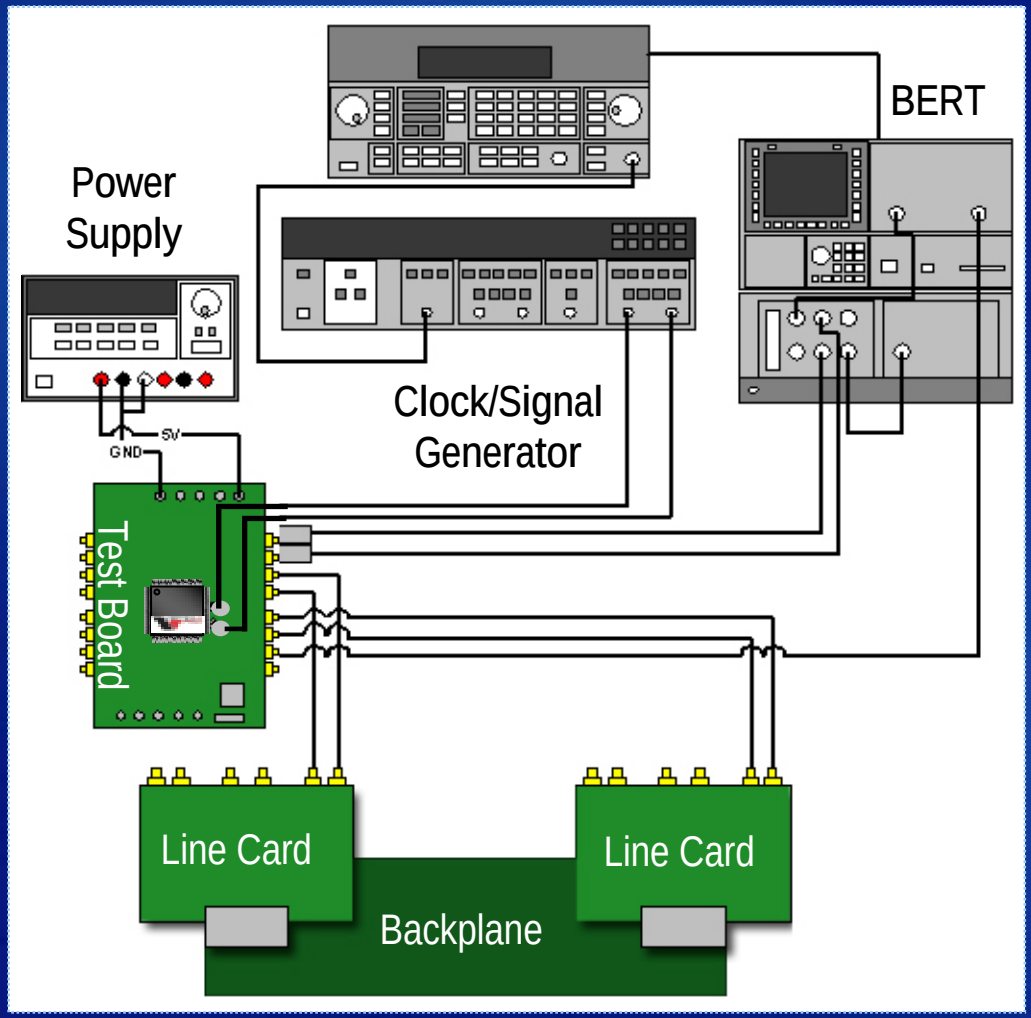
Solving the Challenges

- Characterization and Prototyping
  - Determine overall system signal integrity and margin
- System Design Aspects
  - I/O performance tuning
  - Serial Protocol Selection
- Simulation is Recommended
  - HSPICE, S-parameter simulation

Characterization & Prototyping

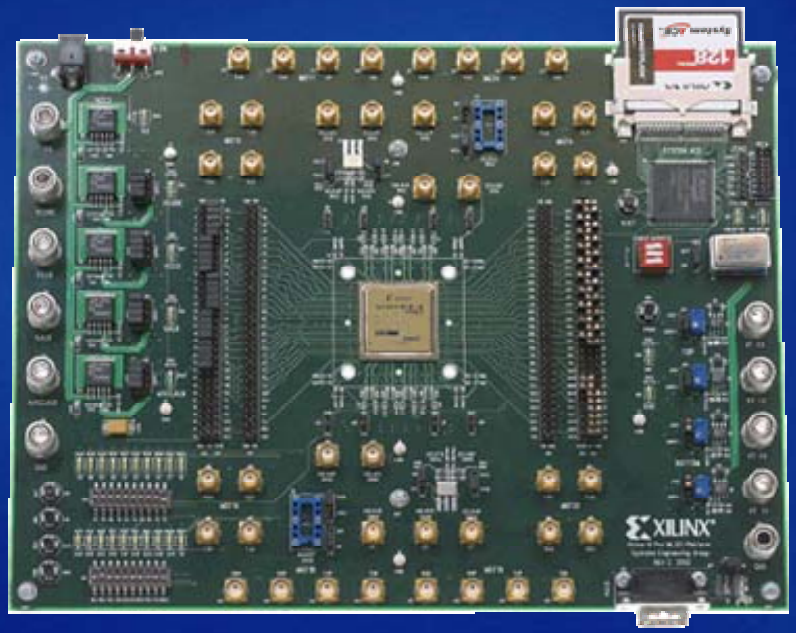
- Backplane Characterization Techniques
  - Eye diagrams - height and width
  - Deterministic and random jitter
  - Channel Bit Error Rate (BER)
  - Channel loss with S-parameters using a Vector Network Analyzer (VNA)
  - Channel discontinuities using a Time Domain Reflectometer (TDR)
- Validate Simulation with Hardware

Backplane Test Setup



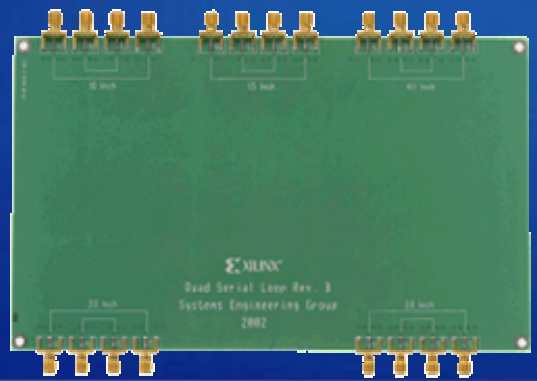
- Test Board Transmits and Receives Across Backplane
- Loopback within the Characterization Board

Example HW Characterization Platforms

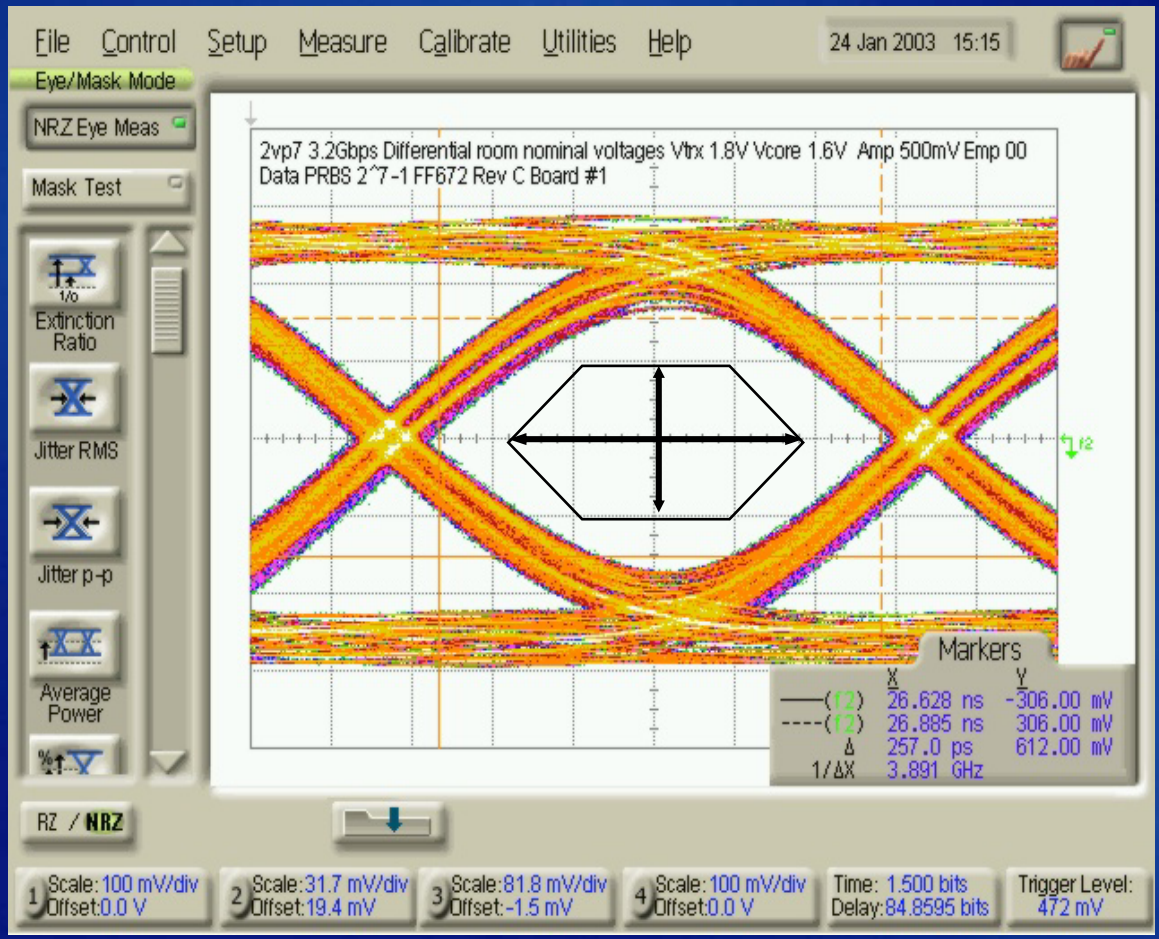


- ML321 Characterization Board
- Target device = XC2VP7 with 8 RocketIO™ Serial Transceivers
- On-board Oscillator or External Clock Source Options
- 8 mil Width / 10 mil Spacing Microstrip (Buried Trace) Lines
- 100 Ohms Differential Termination

- Microstrip Board
- Allows Additional FR4 Trace Length to Be Added to RocketIO Signals
- 10”, 15”, 20”, 30”, or 40” FR4 Microstrip Lines

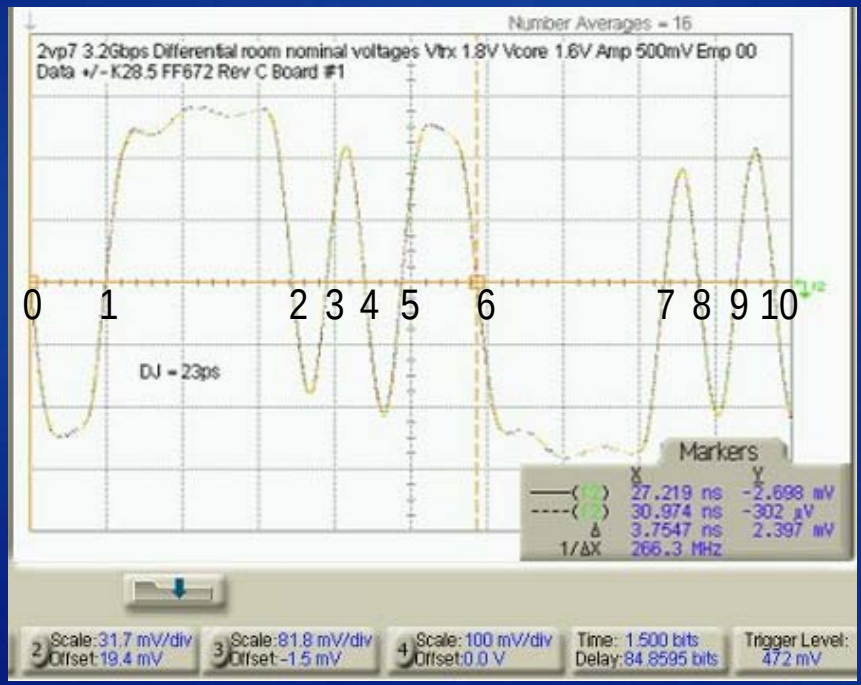


Eye Diagram with Mask

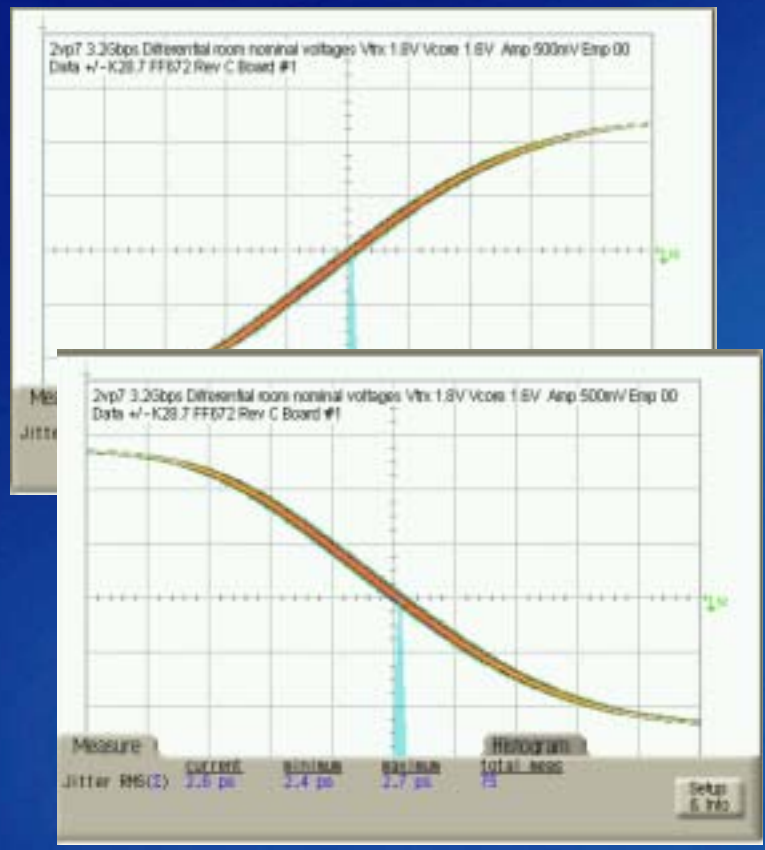


- Eye Width
  - Data valid time
- Eye Height
  - Differential voltage
- Eye Mask
  - Defined by specific standard

System Jitter



Deterministic Jitter



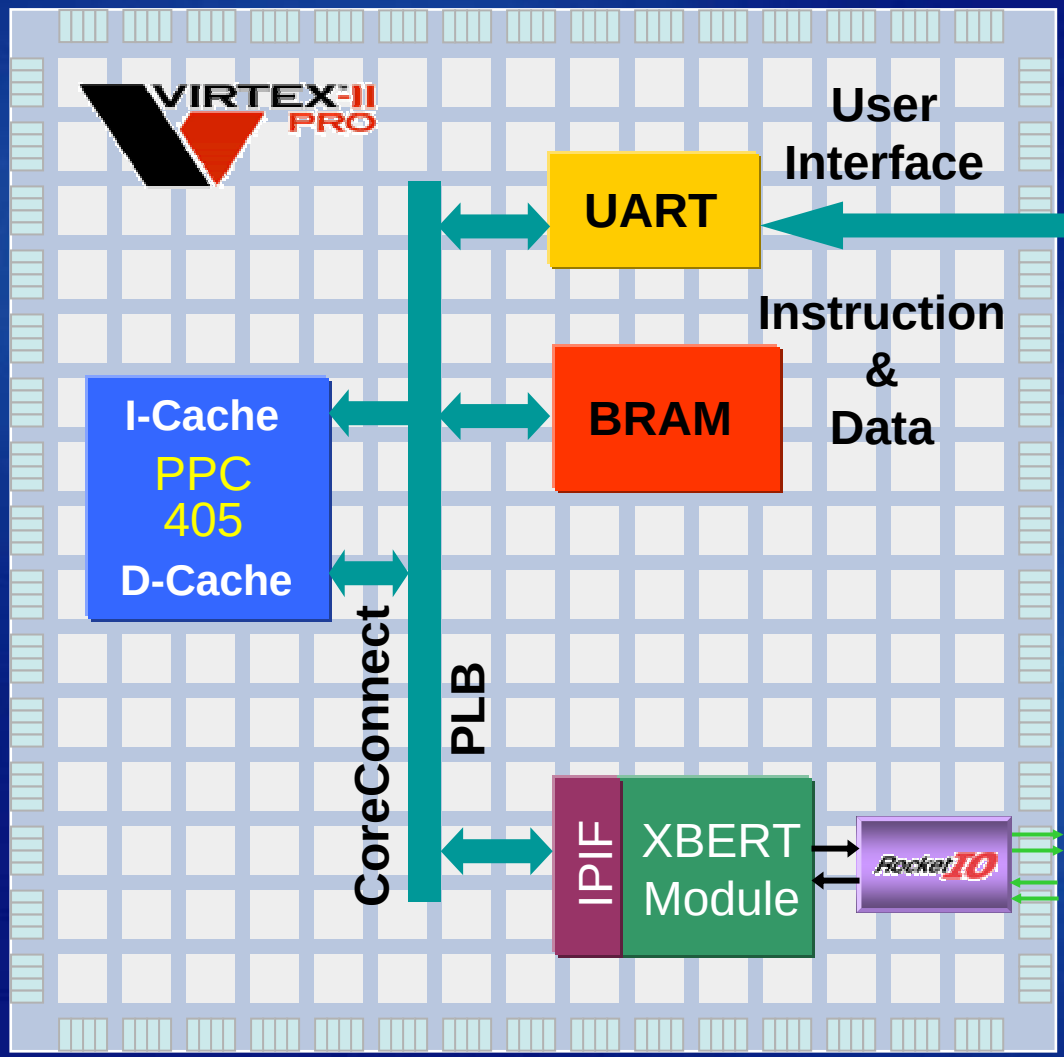
Random Jitter

- Characteristics of Your Physical System
  - K28.5 & K28.7 are common test patterns

Bit Error Rate Test (BERT)

- Used to Verify Serial Links Integrity and Compliance to Standard Specifications
- In Its Most Simplistic Form
  - BER = Dropped frames/ Total frames
- In the Real World, BER is Calculated as a Statistical Estimate of the True Bit Error Rate
- Pseudo Random Binary Sequence (PRBS)
  - Typically used as a test signal when making BER measurements

Xilinx On-Chip BERT Design



- PowerPC Controls BERT and PRBS Testing
- Simple Interface for Rapid Characterization & Interoperability Tests

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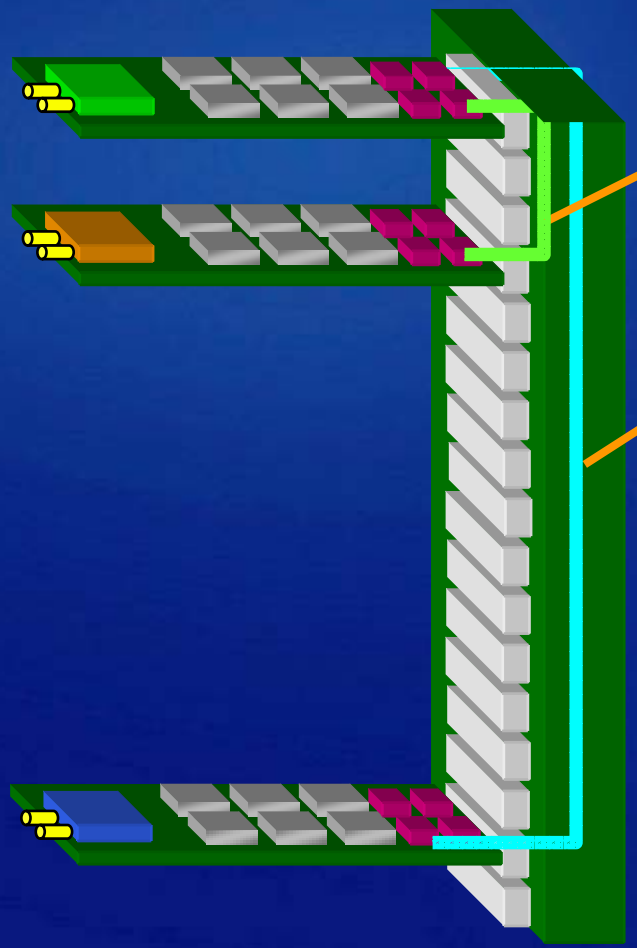
System Distance Dilemma



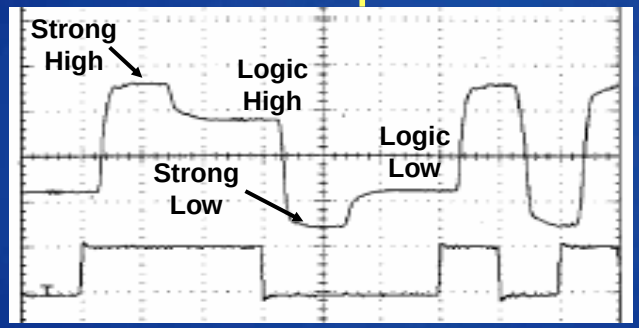
Example A: Short Trace

Example B: Long Trace

- Signal Attenuation & Jitter are Functions of Trace Length
- Transmitter Settings Can be Adjusted for Slot Location Within Backplane for Optimal Performance

Pre-emphasis for Signal Integrity

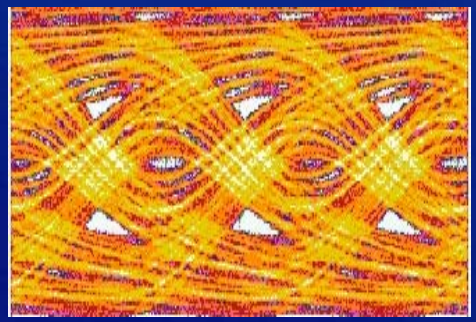
Pre-emphasis



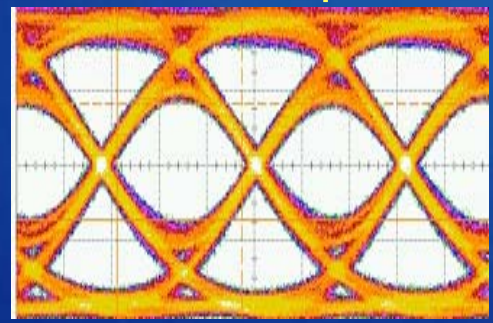
No Pre-emphasis

- Pre-emphasis Increases Drive of Transmitter Briefly
- Compensates for Frequency Dependent Loss in the Transmission Media
- Decreases Deterministic Jitter (DJ) at Receiver

10% Pre-emphasis



33% Pre-emphasis



After 44” of FR4 Backplane (3.125 Gbps)

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Xilinx Adaptive I/O Solution

- Enhanced Diagnostic Testing
  - Integrated with XBERT reference design
- Rapid Prototyping
  - Terminal interface for command line control of diagnostic testing and MGT transmitter settings without requiring FPGA reconfiguration
- In System RocketIO™ Attribute Setting
  - MGT attributes can be automatically set depending on backplane slot location, accommodating differences in transmission length

Serial Protocols Supported

LAN/MAN/WAN

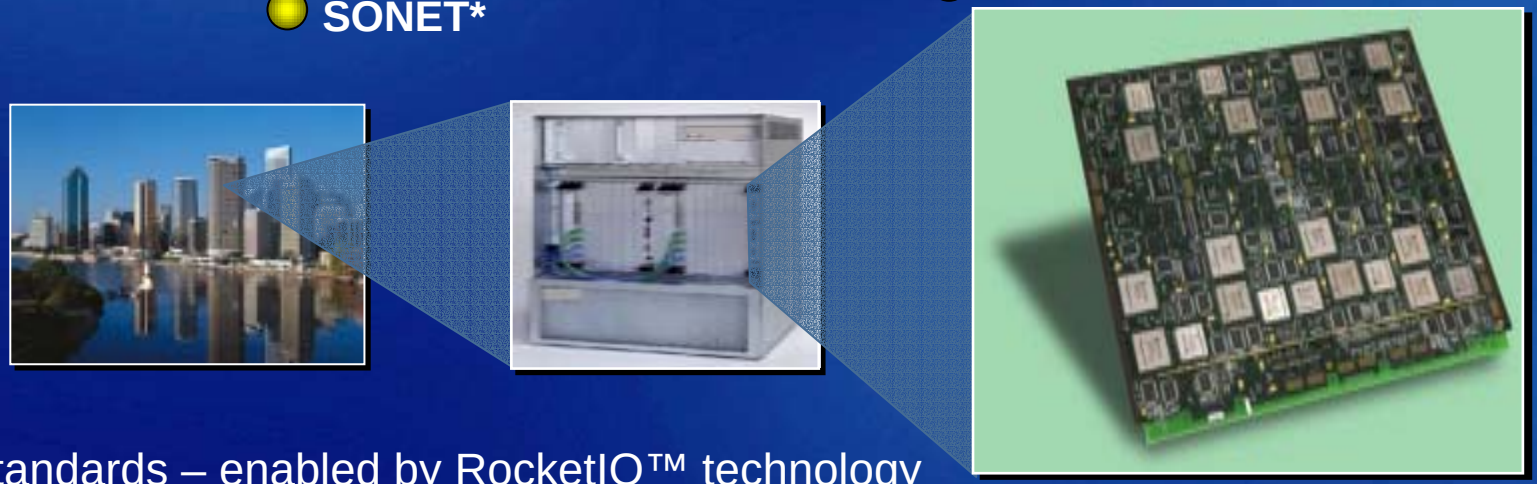
- 10/100 Ethernet (MII)
- 1Gb Ethernet(GMII)
- 10Gb Ethernet(XGMII)
- 1Gb Ethernet (1000 Base-X)
- 10Gb Ethernet (XAUI)
- OC48*
- OC192*
- OC768*

Board-to-Board/Backplane

- PCI 32/33
- PCI 64/66
- PCI-X 100
- **RapidIO Ser.**
- **Fibre chan.**
- **10GE(XAUI)**
- **SONET***
- RapidIO™
- CSIX
- HyperTransport
- **InfiniBand™**
- **PCI Express™**
- **Aurora**

Chip-to-Chip

- PCI 32/33
- PCI 64/66
- PCI-X 66&133
- RapidIO
- SFI-4
- 10GE (XAUI)
- SPI-3 & SPI-4.2
- SPI-4.1
- CSIX
- HyperTransport
- XSBI
- PCI Express



- Serial Standards – enabled by RocketIO™ technology
- Parallel Standards – enabled by SelectIO™-Ultra technology

* SONET compatible, supports data rate

http://www.xilinx.com/connectivity

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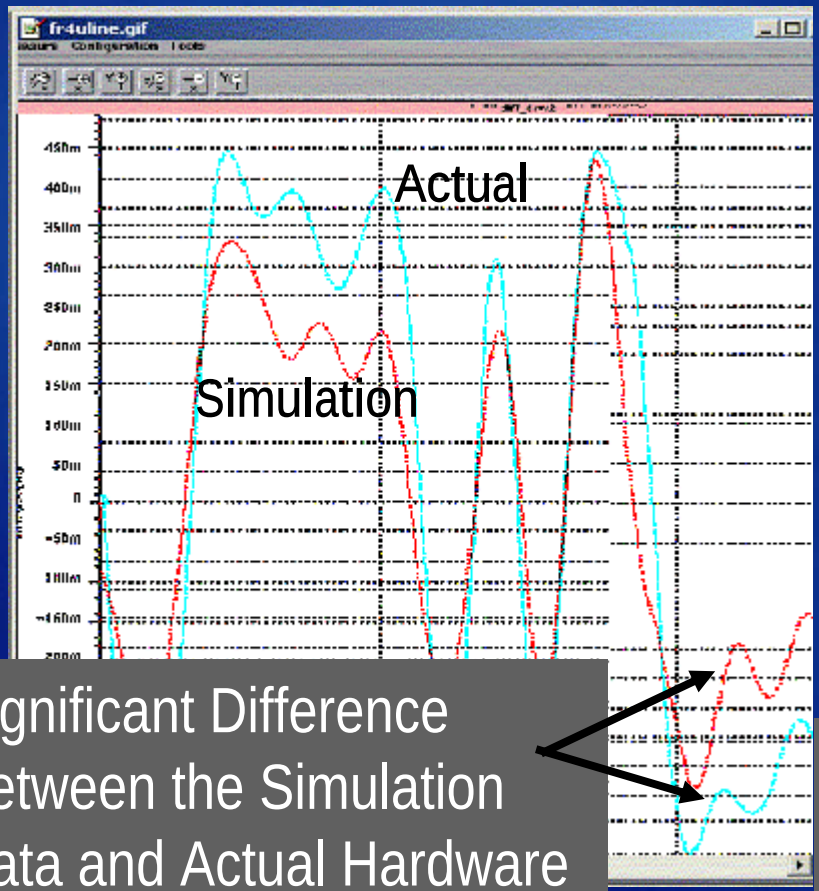
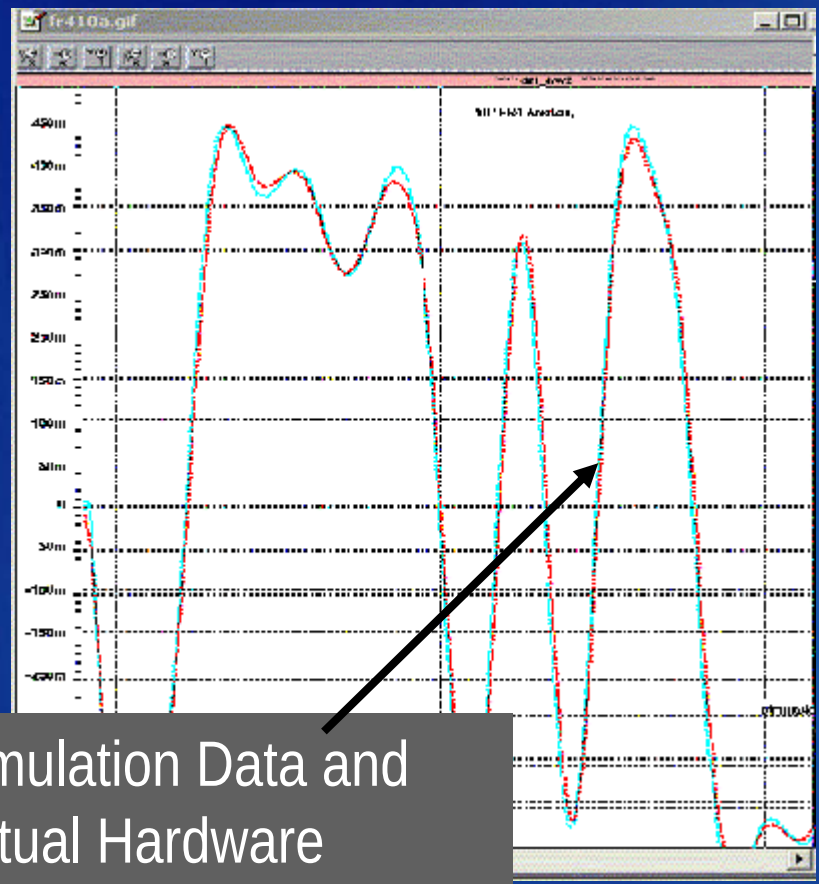
Simulation to H/W Correlation

- MGT SPICE Models are Provided by IC Vendors
- SPICE Connector Models Can be Difficult to Use
- Lossy Coupled Transmission Lines
  - Modeling requires the use of matrices generated by a field solver and a frequency-dependent simulation methodology
  - "W element" modeling is commonly used to simulate coupled transmission lines with loss
  - S-parameter modeling can be more accurate

W-Element vs S-Parameters Simulation



Significant Difference Between the Simulation Data and Actual Hardware Measurements



Simulation Data and Actual Hardware Measurements Match

Serial Design Resources

Dedicated Web Portal - http://www.xilinx.com/serialsolution

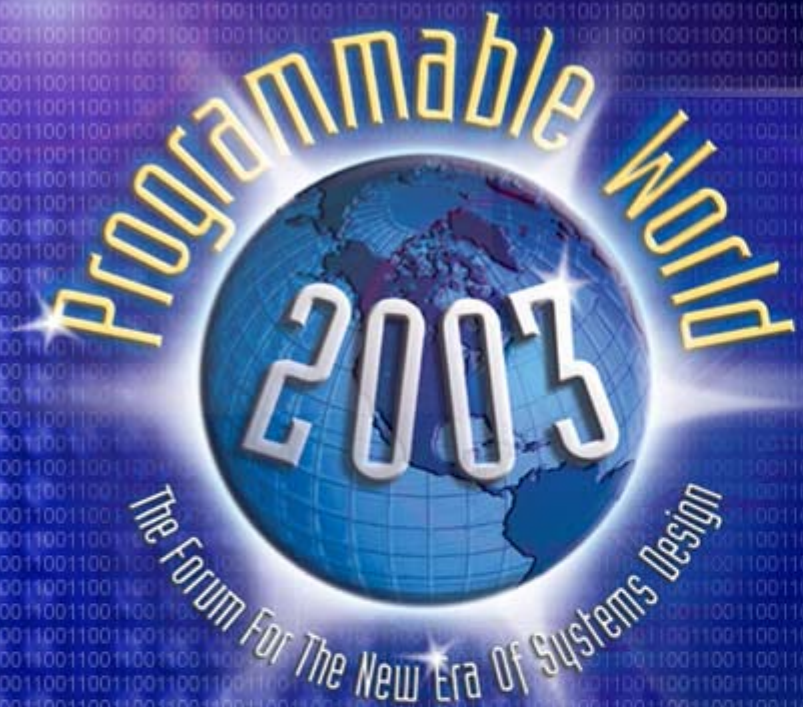
- IP/ Ref. Designs
- RocketIO Data
  - Characterization
  - User Guide
  - SPICE suite
- PCB Design/Signal Integrity Tools
- HW Evaluation Platforms
- Partner Solutions
- Technical Training
- Design Services

Conclusion

- Upgrading is Challenging but Achievable
- Upgrading Achieves Higher System Performance at Lower Cost in a Shorter Time
- FPGAs Offer Flexible and Cost Effective Solutions
- Xilinx Has Design Resources to Ensure Your Success

References

- Adaptive I/O Solution - Three Reference Designs
  - http://www.xilinx.com/xapps/xapp660.pdf
  - http://www.xilinx.com/xapps/xapp661.pdf
  - http://www.xilinx.com/xapps/xapp662.pdf
- Aurora Open Protocol
  - http://www.xilinx.com/aurora
- Serial Design Resources (http://www.xilinx.com/serialsolution)
  - RocketIO User Guide
  - RocketIO Characterization Report
  - RocketIO ML321 characterization board
  - Serial IP & reference designs
  - RocketIO training class



Thank You!