

Challenges and Design Solutions to Upgrade Existing Systems for Higher Bandwidth (Part 2)

Agenda

- Major design-in challenges
- Why simulate?
- Enabling design collaboration



Design-in of Complex IC's is Tougher than Ever

Silicon



Package



onto

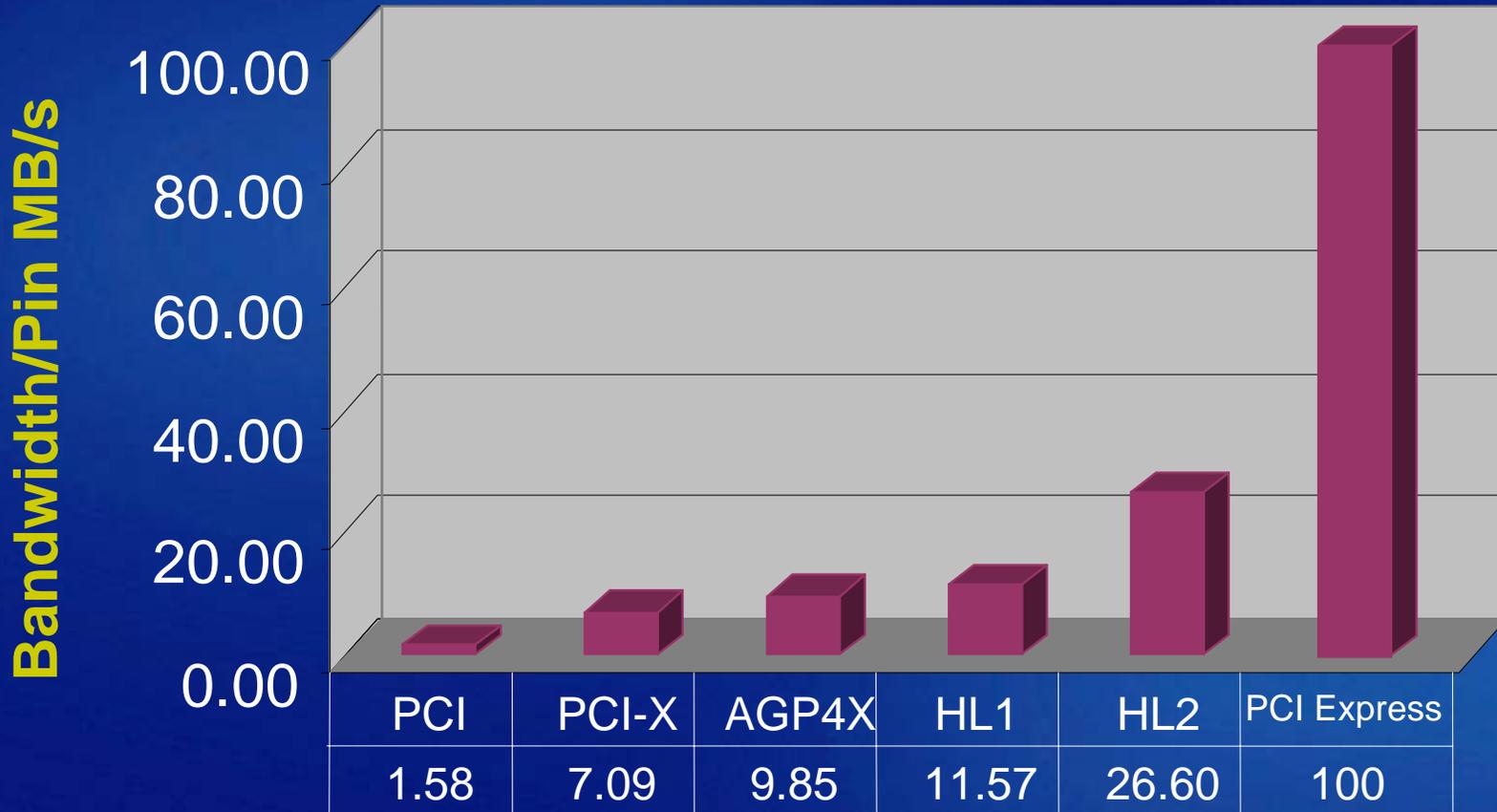
Board



into

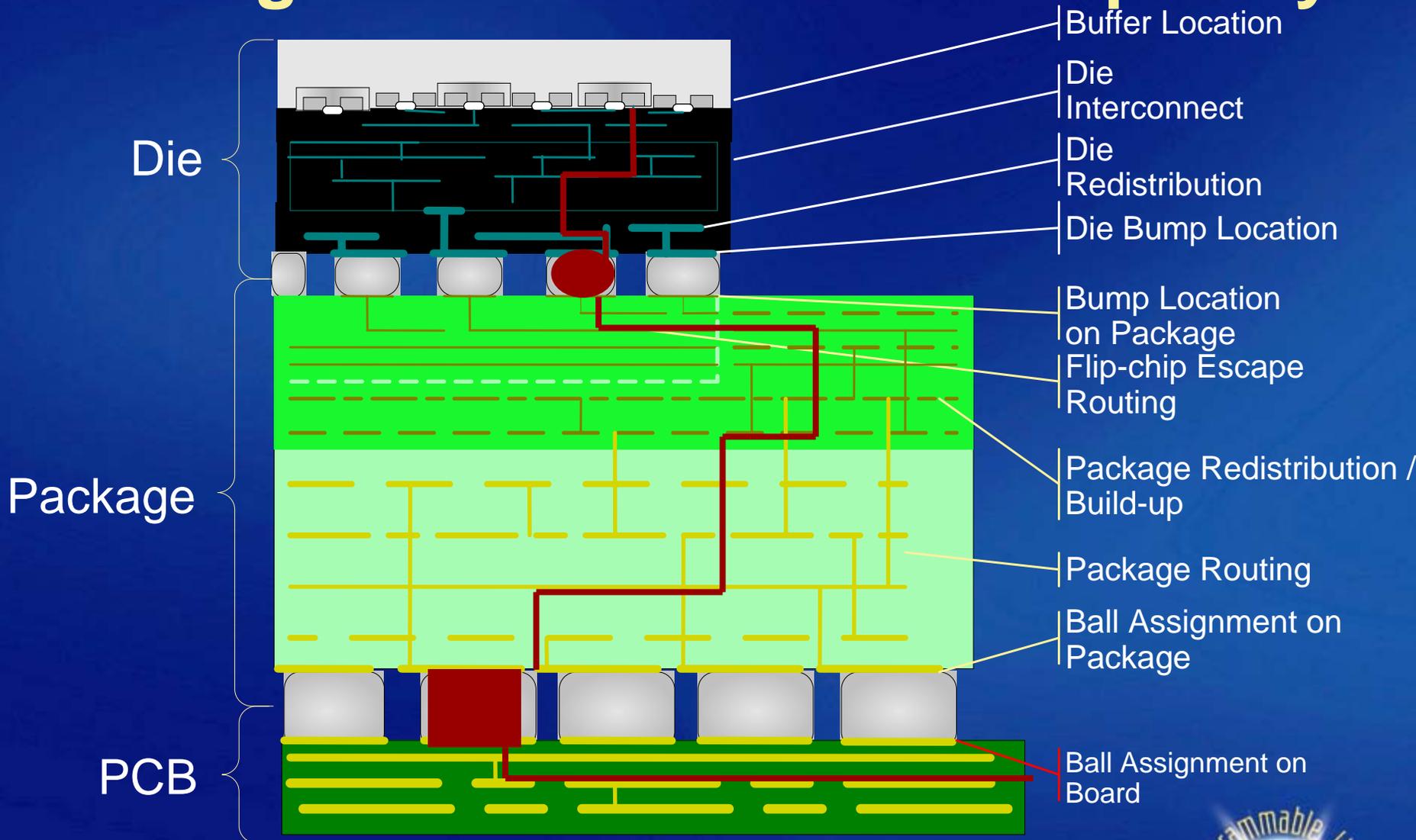
To
Volume

Increasing Bandwidth/pin Efficiency

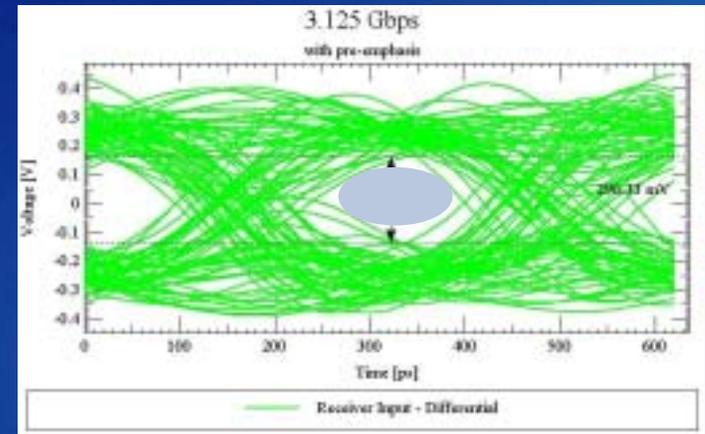
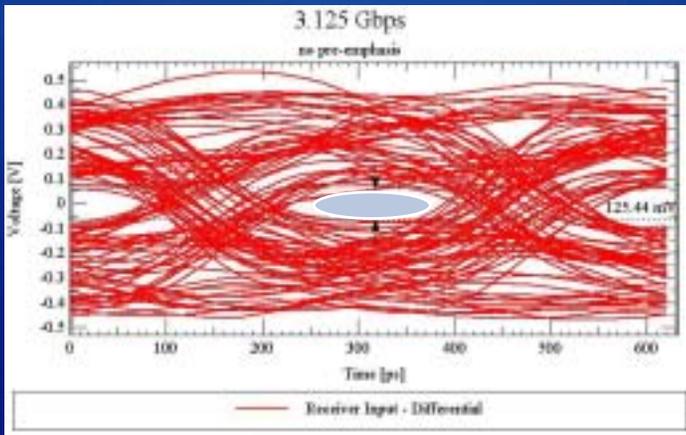
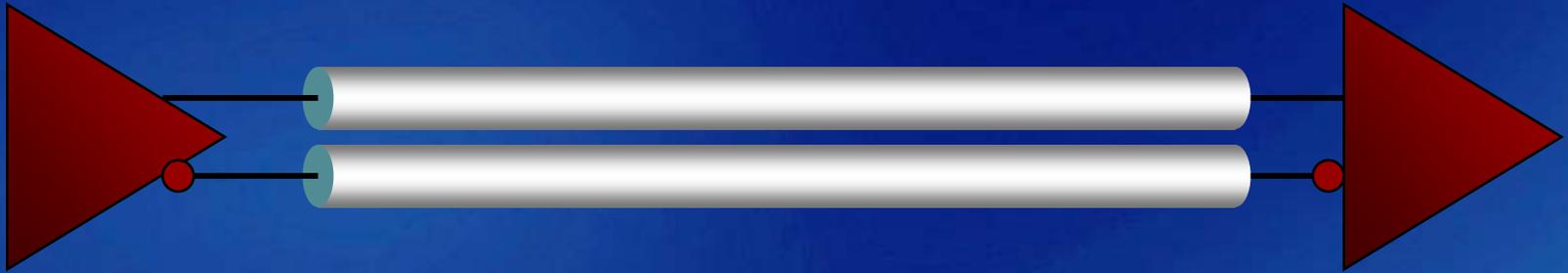


Source: Intel PCI Express Overview
Pins include all signals + VCC/GND

Dealing with Interconnect Complexity

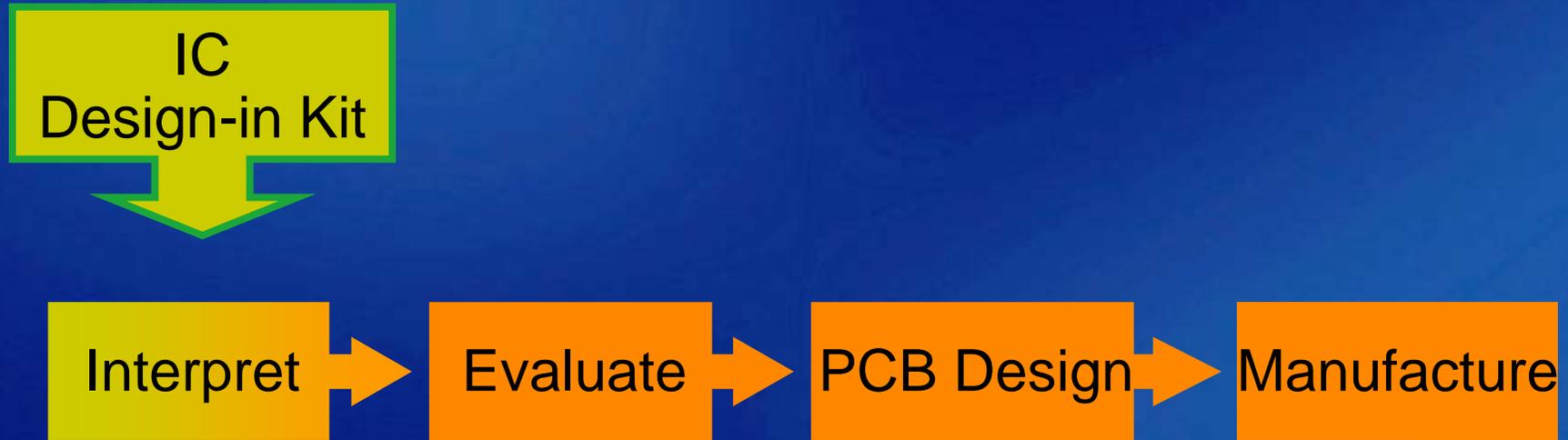


Simulation is Critical for High-Speed Design



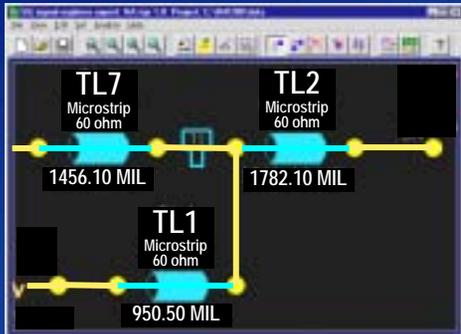
But setting up for simulation can be time consuming...

Design-in Kits Accelerate Design Start Time

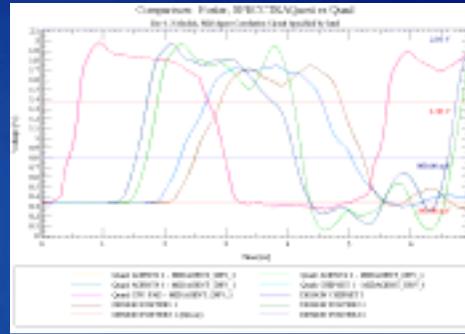


Save weeks or months off your design cycle

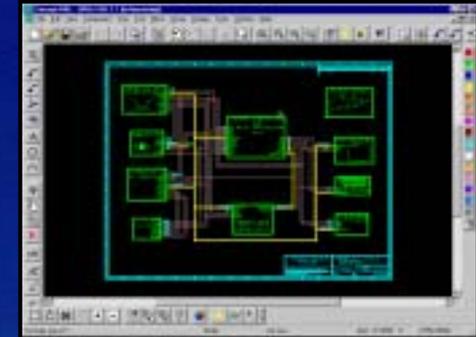
Design Kit Contents



Simulation Setup



Correlation Data



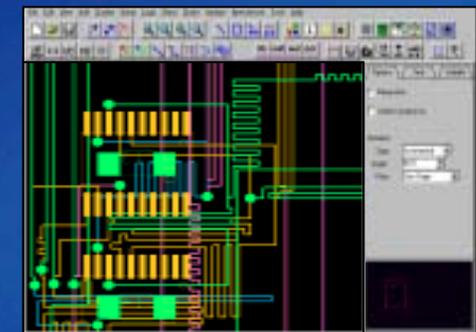
Schematics

| Constraint | Value | Unit | Min | Max |
|--------------|---------|------|-----|-----|
| TL1 Length | 950.50 | MIL | | |
| TL2 Length | 1782.10 | MIL | | |
| TL7 Length | 1456.10 | MIL | | |
| TL Impedance | 60 | ohm | | |

Constraints



**Tutorials
Utilities
Web page**



PCB Layout

Ready to simulate in minutes



High-speed PCB Systems Design

Design-in
Kit

EXPLORATION

CONSTRAIN &
FLOORPLAN

CONSTRAINT
DRIVEN LAYOUT

VERIFICATION



High-speed PCB Systems Design

Design-in Kit



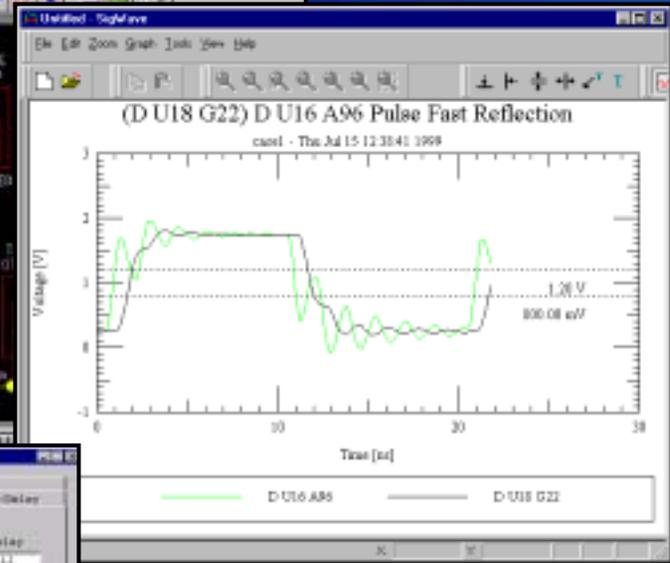
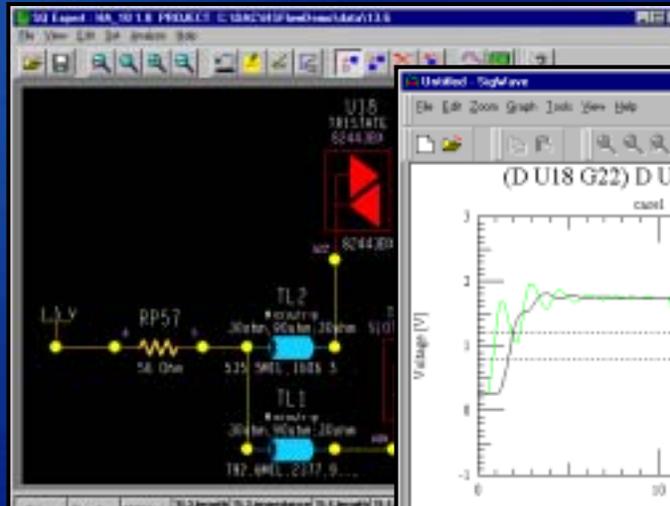
Models, topologies, stimulus,
Custom measurements

EXPLORATION

CONSTRAIN &
FLOORPLAN

CONSTRAINT
DRIVEN LAYOUT

VERIFICATION



| From | To | Rule Type | Min Delay | Max Delay |
|------|-----|-----------|-----------|-----------|
| TL1 | TL2 | EXP-78 | 500 nll | 800 nll |
| TL2 | TL1 | EXP-78 | 500 nll | 800 nll |
| TL1 | TL1 | EXP-78 | 500 nll | 800 nll |

Rule Name:

Rule Type:

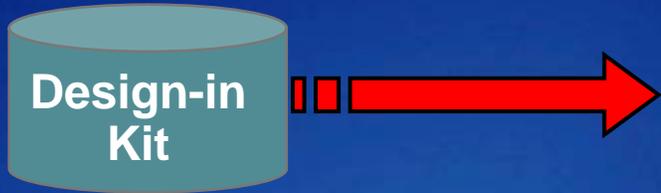
Min Delay:

Max Delay:

Buttons: Add, Delete, OK, Cancel, Help



High-speed PCB Systems Design



Pre-defined rules
Example schematic & layout

EXPLORATION

CONSTRAIN &
FLOORPLAN

CONSTRAINT
DRIVEN LAYOUT

VERIFICATION

The collage shows various stages of PCB design: a schematic diagram, a physical layout, a timing analysis table, and a signal integrity plot.

| Signals | Min | Actual | Margin | Max | Actual | Margin |
|--------------|---------|--------|--------|------|--------|---------|
| | | | | | | |
| System | | | | | | |
| MicroBoard # | | | | | | |
| SA_2 | | | | | | 0029... |
| U1E100P17.0 | 100 000 | | | 1000 | 0007.0 | 0010... |
| SA_4 | | | | | | 0013... |
| U1E1000P04.3 | 100 000 | | | 1000 | 0011.3 | 0013... |
| SA_5 | | | | | | 001400 |
| U1E100P17.7 | 100 000 | | | 1000 | 0040 | 001400 |
| SA_6 | | | | | | 0018... |
| U1E100P04.1 | 100 000 | | | 1000 | 0017.8 | 0018... |
| SA_7 | | | | | | 0016... |
| U1E100P17.0 | 100 000 | | | 1000 | 0016.3 | 0016... |
| SA_8 | | | | | | 0008... |
| U1E100P04.1 | 100 000 | | | 1000 | 0006.0 | 0008... |
| SA_9 | | | | | | 0018... |

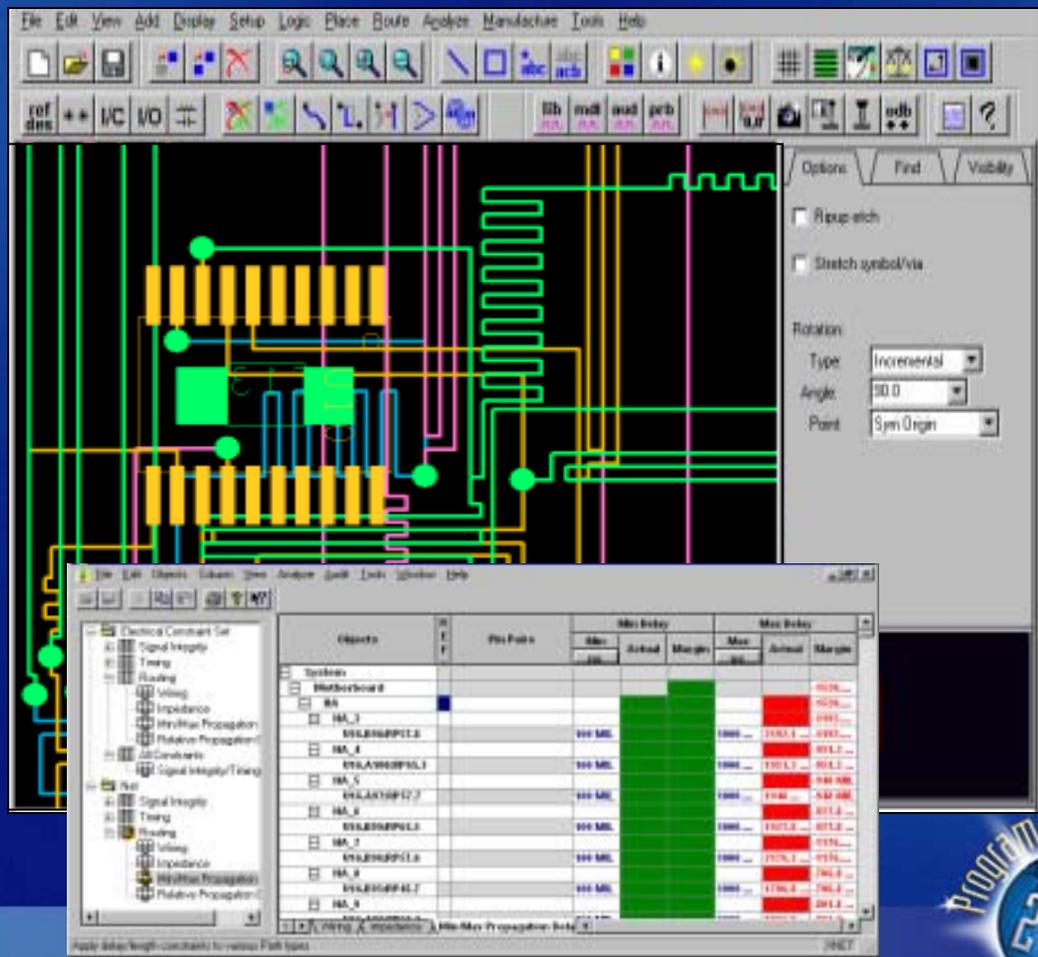


High-speed PCB Systems Design

Design-in Kit



Example PCB, footprints, Common constraints



EXPLORATION

CONSTRAIN & FLOORPLAN

CONSTRAINT DRIVEN LAYOUT

VERIFICATION



High-speed PCB Systems Design

Design-in Kit



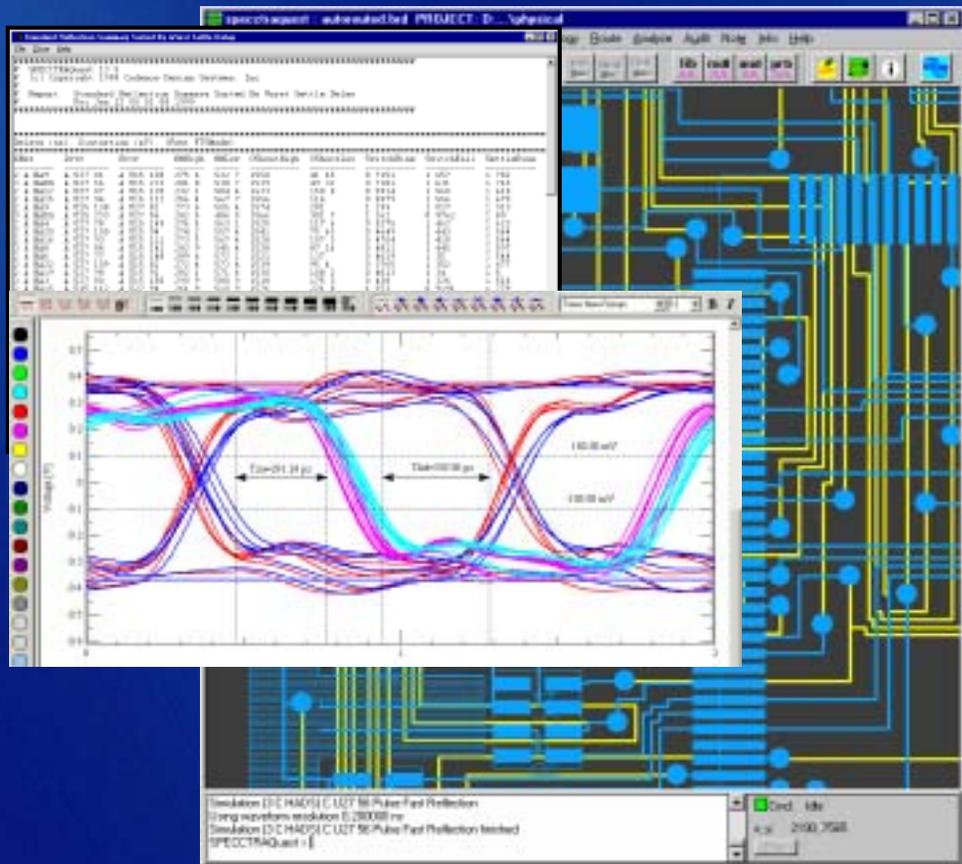
Component models
Post-processing utilities

EXPLORATION

CONSTRAIN & FLOORPLAN

CONSTRAINT DRIVEN LAYOUT

VERIFICATION



Design-in Kits Available Now

The screenshot shows the Xilinx website's 'Products' section. The Xilinx logo is in the top left. A navigation bar contains links for HOME, PRODUCTS, END MARKETS, SUPPORT, EDUCATION, ONLINE STORE, CONTACT, and SEARCH. Below this is a secondary navigation bar with links for Silicon Solutions, Design Resources, System Resources, and Literature. The main content area features a sidebar on the left with 'What's New Success Stories', 'Cadence SPECCTRAQuest™', and 'RocketIO Design Kit with Cadence SPECCTRAQuest'. The main text area includes a breadcrumb trail, a sub-header for the design kit, a paragraph about the goal of getting products to market, a paragraph about the importance of analyzing high-speed signal integrity, and a paragraph describing the design kit as an electronic blueprint. A 'Related Features' box on the right lists links to an alliance overview, a SPECCTRAQuest overview, a download link, and a journal article. A bulleted list at the bottom details the kit's contents, including system level topologies, IO buffer models, a large package model, test bench data, connector models, device-specific scripts, and a video.

XILINX® Products

HOME PRODUCTS END MARKETS SUPPORT EDUCATION ONLINE STORE CONTACT SEARCH

| Silicon Solutions | [Design Resources](#) | System Resources | Literature |

Home : [Products and Solutions](#) : [ISE Logic Design Tools](#) : [Alliance EDA Partners](#) : RocketIO Design Kit with Cadence SPECCTRAQuest

RocketIO Design Kit with Cadence SPECCTRAQuest

Now that you are considering the use of Xilinx RocketIO technology in your next product, getting it to market as soon as possible is a primary goal.

Properly analyzing and correcting potential high speed signal integrity problems BEFORE you fabricate your PCB will greatly help to insure that you do not have multiple board spins.

The RocketIO Design Kit for SPECCTRAQuest, an electronic blueprint for simulating and implementing Virtex-II Pro™ Rocket IO transceivers in a system, allows you to develop optimal constraints for your PCB systems. These constraints then drive PCB floorplanning, routing, and verification process.

The RocketIO Design Kit for SPECCTRAQuest includes the following:

- Ready-to-simulate system level topologies for typical use of the device on the board/system;
- Verified IO buffer models;
- Large Package Model;
- Test bench data, Correlation data;
- Connector models for backplane applications;
- Device specific scripts/tools to evaluate simulation results;
- A video that describes how to get started with the design kit in the end users environment.

Related Features

- ▶ [Cadence and Xilinx Alliance Overview](#)
- ▶ [SPECCTRAQuest Overview](#)
- ▶ [Download the Kit from the SPICE Suite](#)
- ▶ [Xcell Journal Article](#)

http://www.xilinx.com/ise/alliance/rocketio_kit.htm



Summary

- Interconnect complexity and increasing speed
- Signal integrity is a mainstream design problem
- Simulation is the only way to first time design success
- Design-in kits get you designing product faster
- What are your IC suppliers doing to enable your product design?

References

- SPECCTRAQuest high-speed design community
 - <http://www.specctraquest.com>
- Cadence Design Chain Optimization Initiative
 - http://www.cadence.com/feature/design_chain.html
- Articles & papers
 - <http://www.specctraquest.com/Contribute/Solutions.asp>
 - http://www.specctraquest.com/downloads/xc_speckit42.pdf
 - http://www.xilinx.com/publications/xcellonline/xcell_45/xc_cadence45.htm
- Webinars & movies
 - <http://www.cadencepcb.com/promotions/designchain/jump.asp>
 - <http://www.specctraquest.com/Optimize/DesignKits.asp>
 - http://www3.vcall.com/digitallava/cadence_alex_rm/audio_rm/main.htm



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Thank You!

Cadence across silicon-package-board

Market Leader

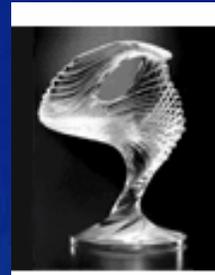
2001 Total Revenue: \$1.43B
2001 Product Revenue: \$830M

Global Business

North America 59%
Europe 21%
Japan/Asia 20%
>58 offices worldwide

Unmatched Resources

Total Employees: 5,600
Engineers: >3,600
2001 R&D investment: ~\$300M



*IEEE Corporate
Innovation Award
Recipient for 2002*



| Rank | Company | Rev. # Mil. |
|------|------------------|-------------|
| 1 | Microsoft | 25,296 |
| 2 | Oracle | 10,860 |
| 3 | Computer Assoc. | 4,198 |
| 4 | Peoplesoft | 2,073 |
| 5 | Siebel Systems | 2,048 |
| 6 | Compuware | 2,010 |
| 7 | BMC Software | 1,504 |
| 8 | Veritas Software | 1,492 |
| 9 | Cadence Design | 1,430 |
| 10 | Electronic Arts | 1,322 |

