Challenges and Design Solutions to Upgrade Existing Systems for Higher Bandwidth (Part 2)

Agenda

- Major design-in challenges
- Why simulate?
- Enabling design collaboration

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Design-in of Complex IC's is Tougher than Ever

Silicon

Package

onto

Board

To Volume

into

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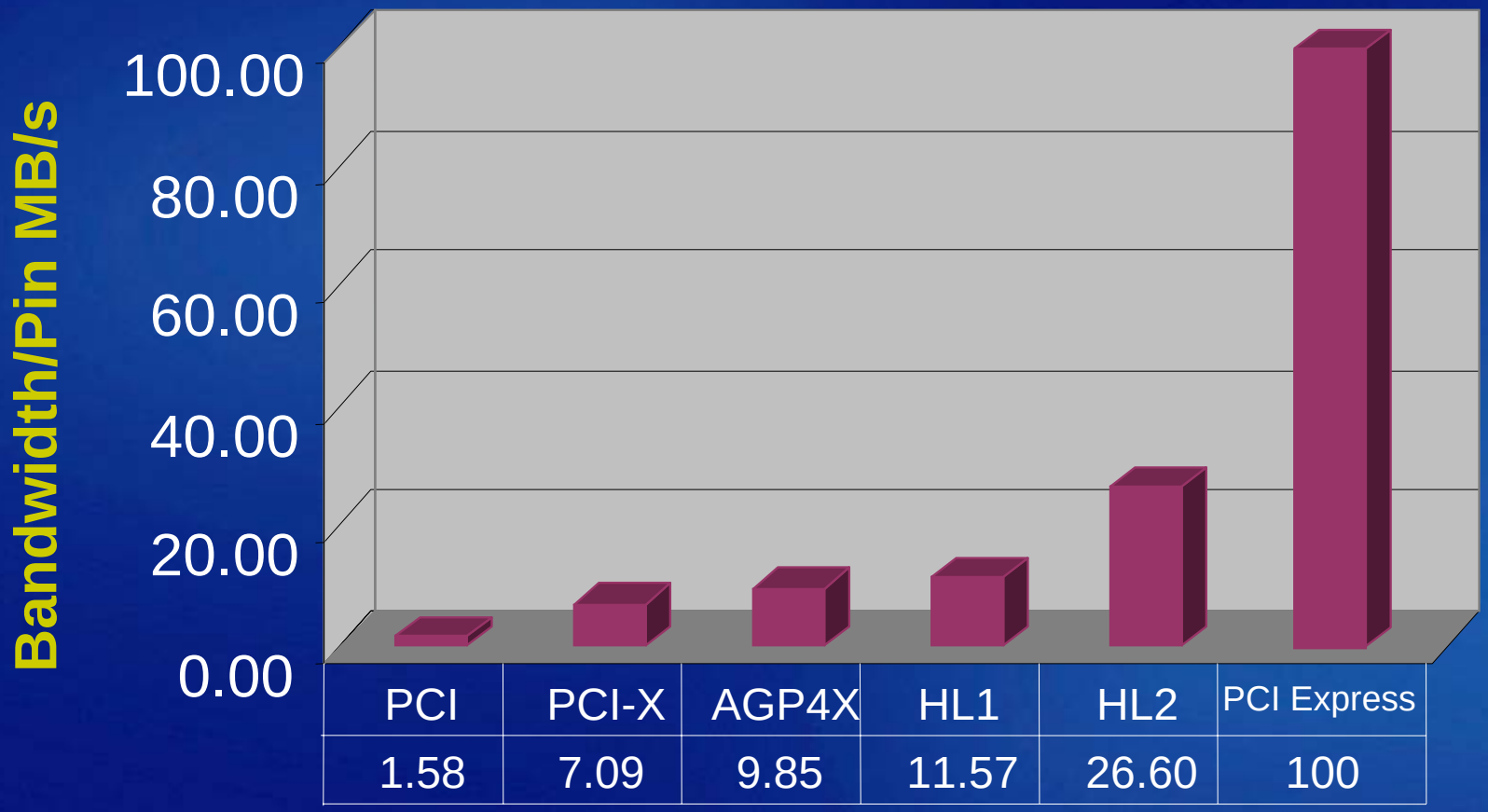
Increasing Bandwidth/pin Efficiency



Source: Intel PCI Express Overview
Pins include all signals + VCC/GND

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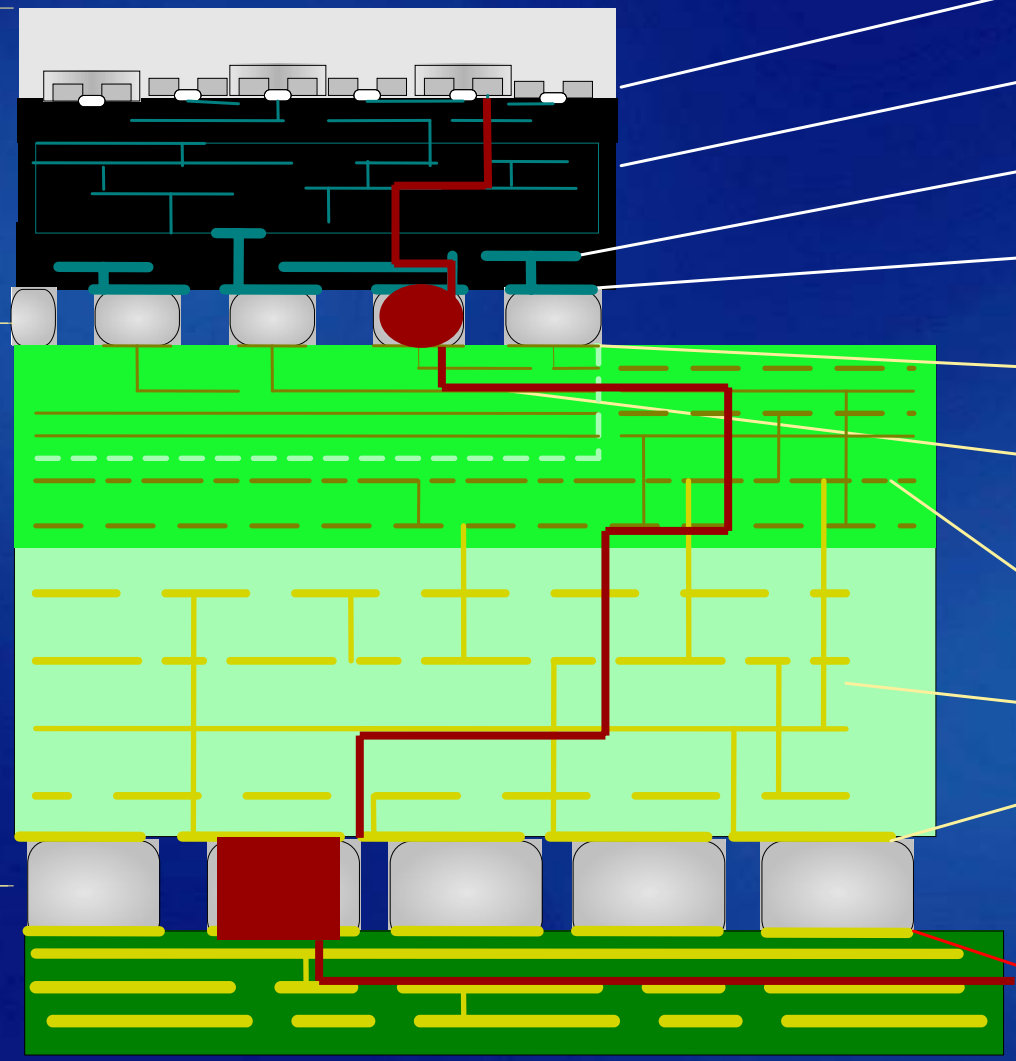
Dealing with Interconnect Complexity



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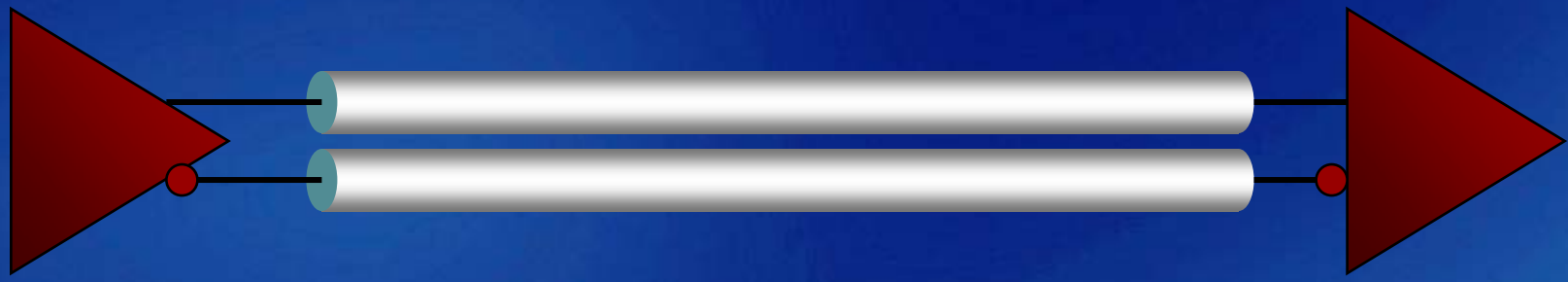
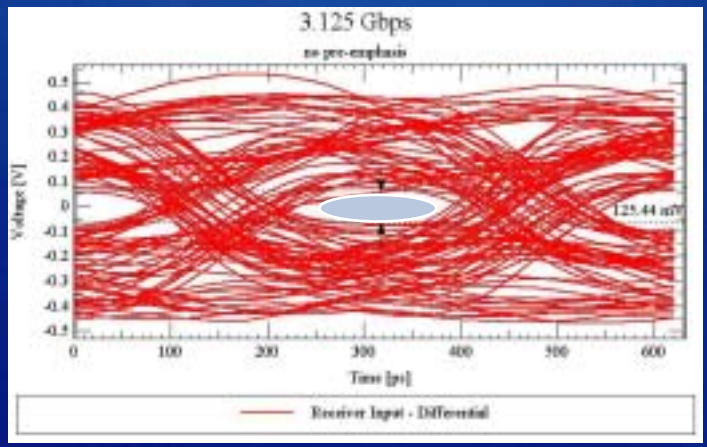
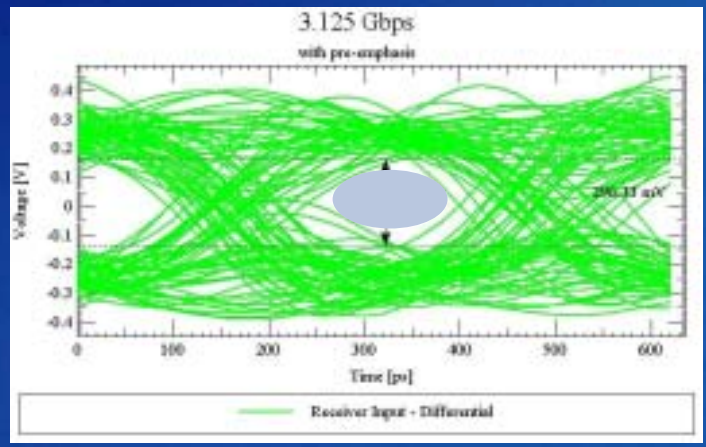
Simulation is Critical for High-Speed Design







But setting up for simulation can be time consuming…

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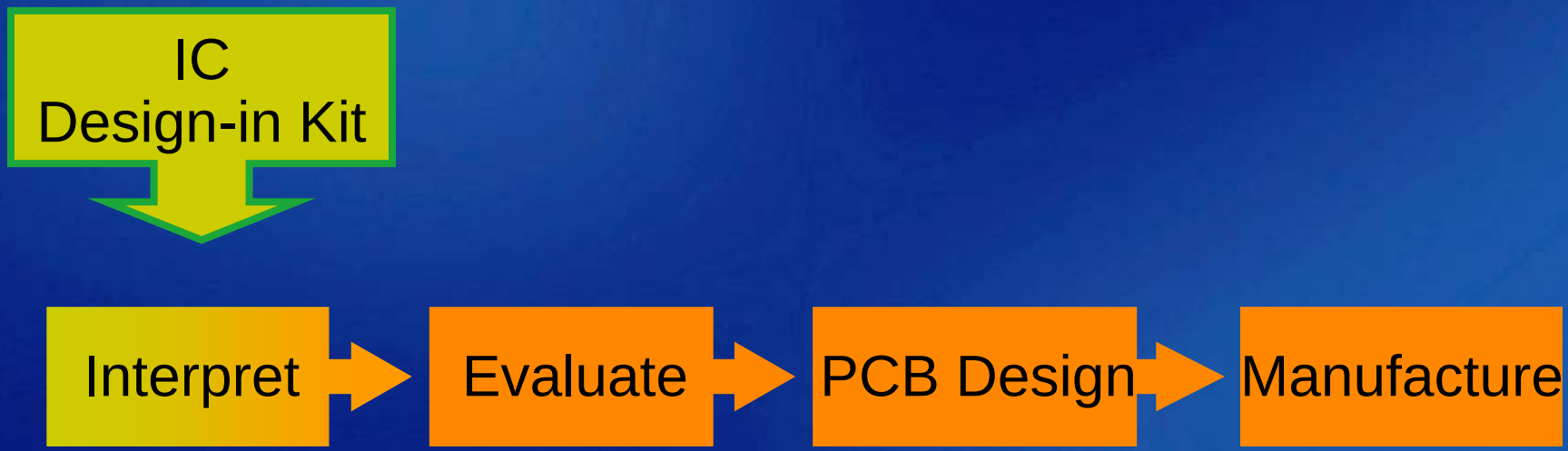
Design-in Kits Accelerate Design Start Time



Save weeks or months off your design cycle

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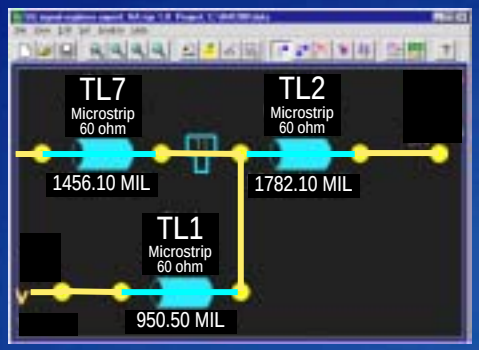
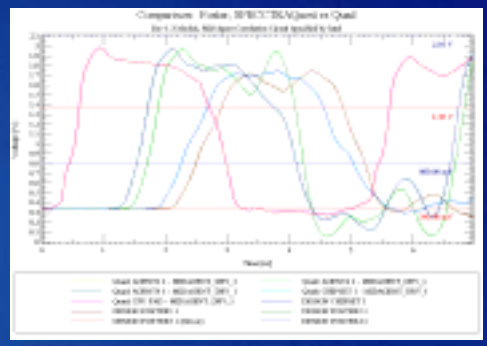
Design Kit Contents



Simulation Setup

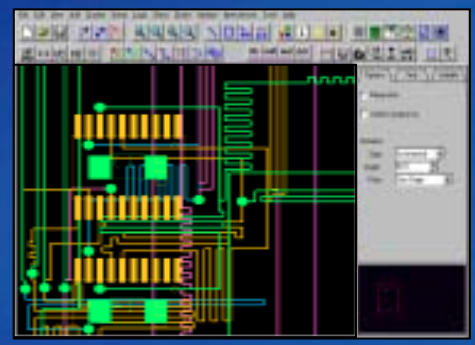


Correlation Data

Schematics

Constraints

Tutorials
Utilities
Web page



PCB Layout

Ready to simulate in minutes

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High-speed PCB Systems Design

EXPLORATION

CONSTRAIN &
FLOORPLAN

CONSTRAINT
DRIVEN LAYOUT

VERIFICATION

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High-speed PCB Systems Design

Design-in Kit

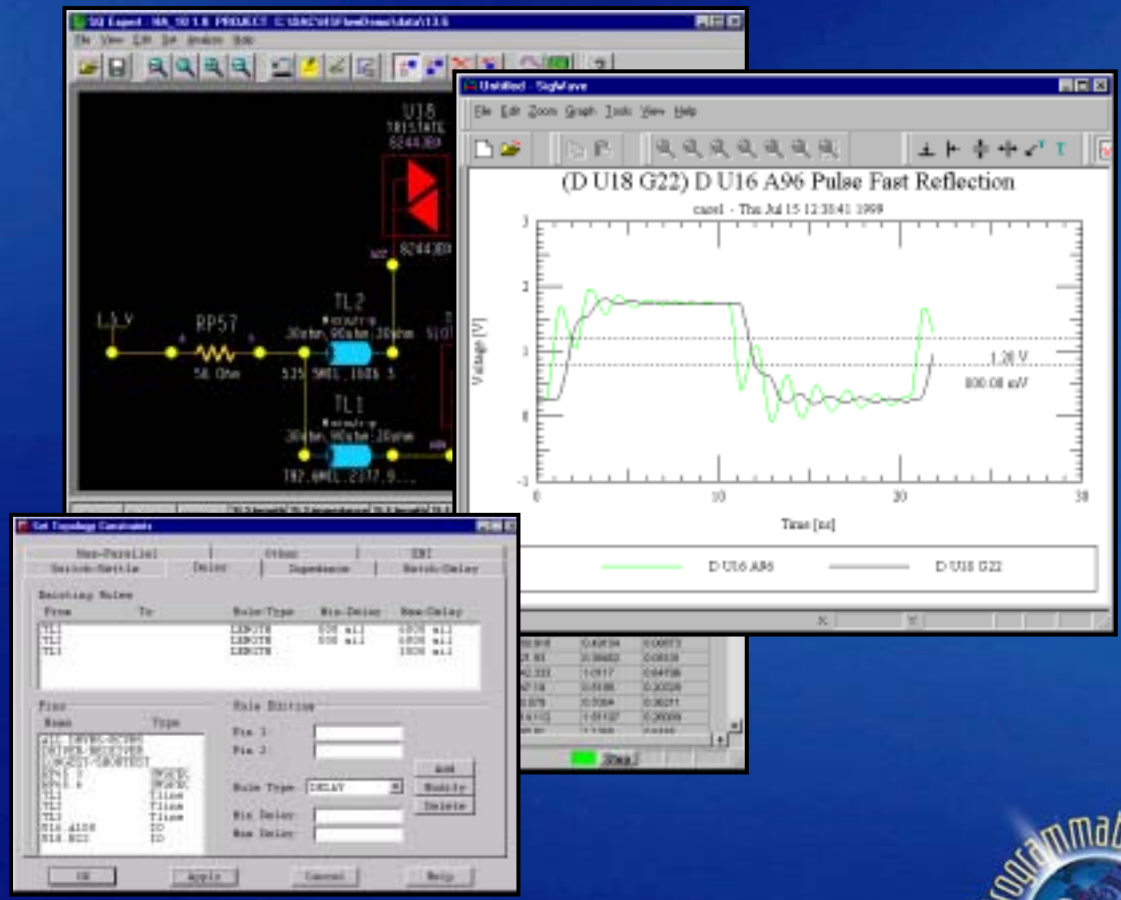
Models, topologies, stimulus,
Custom measurements

EXPLORATION

CONSTRAIN & FLOORPLAN

CONSTRAINT DRIVEN LAYOUT

VERIFICATION



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High-speed PCB Systems Design

Design-in Kit

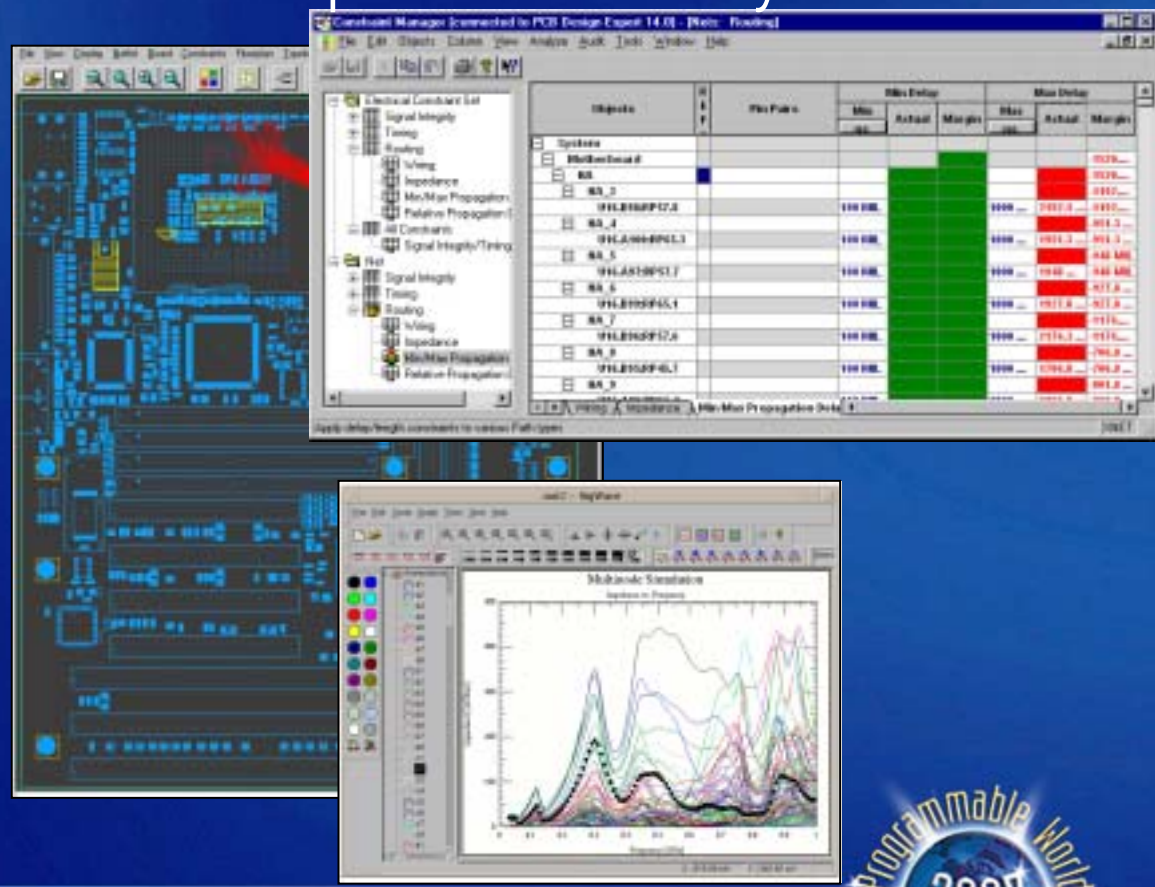
Pre-defined rules
Example schematic & layout

EXPLORATION

CONSTRAIN & FLOORPLAN

CONSTRAINT DRIVEN LAYOUT

VERIFICATION



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High-speed PCB Systems Design

Design-in Kit

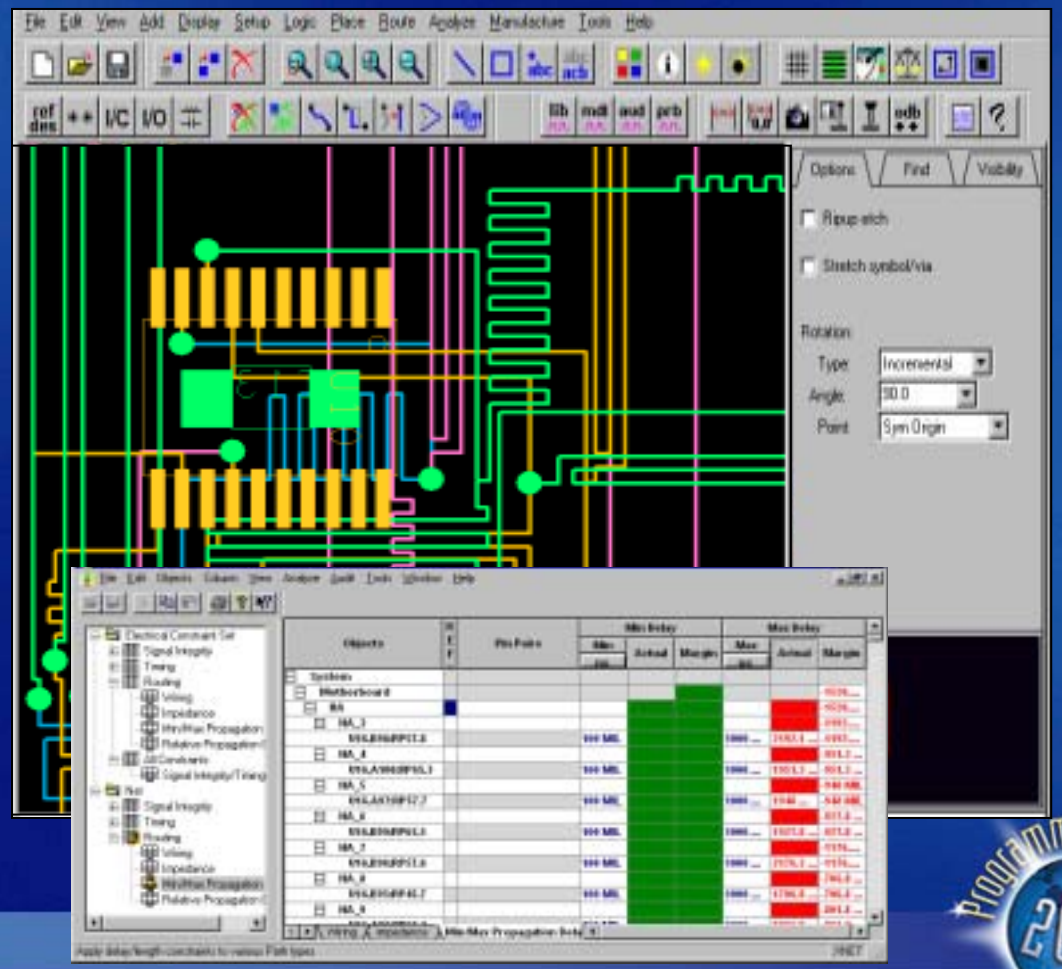
Example PCB, footprints, Common constraints

EXPLORATION

CONSTRAIN & FLOORPLAN

CONSTRAINT DRIVEN LAYOUT

VERIFICATION



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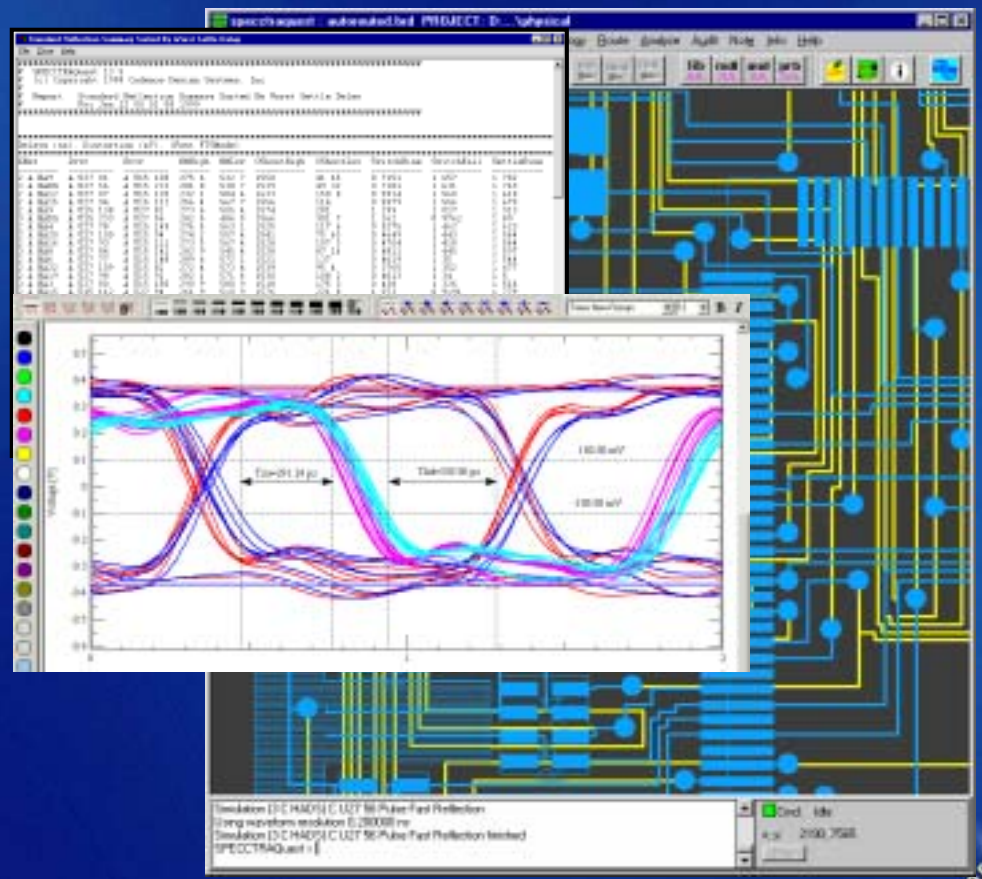
High-speed PCB Systems Design

Design-in Kit

Component models
Post-processing utilities



EXPLORATION

CONSTRAIN & FLOORPLAN

CONSTRAINT DRIVEN LAYOUT

VERIFICATION

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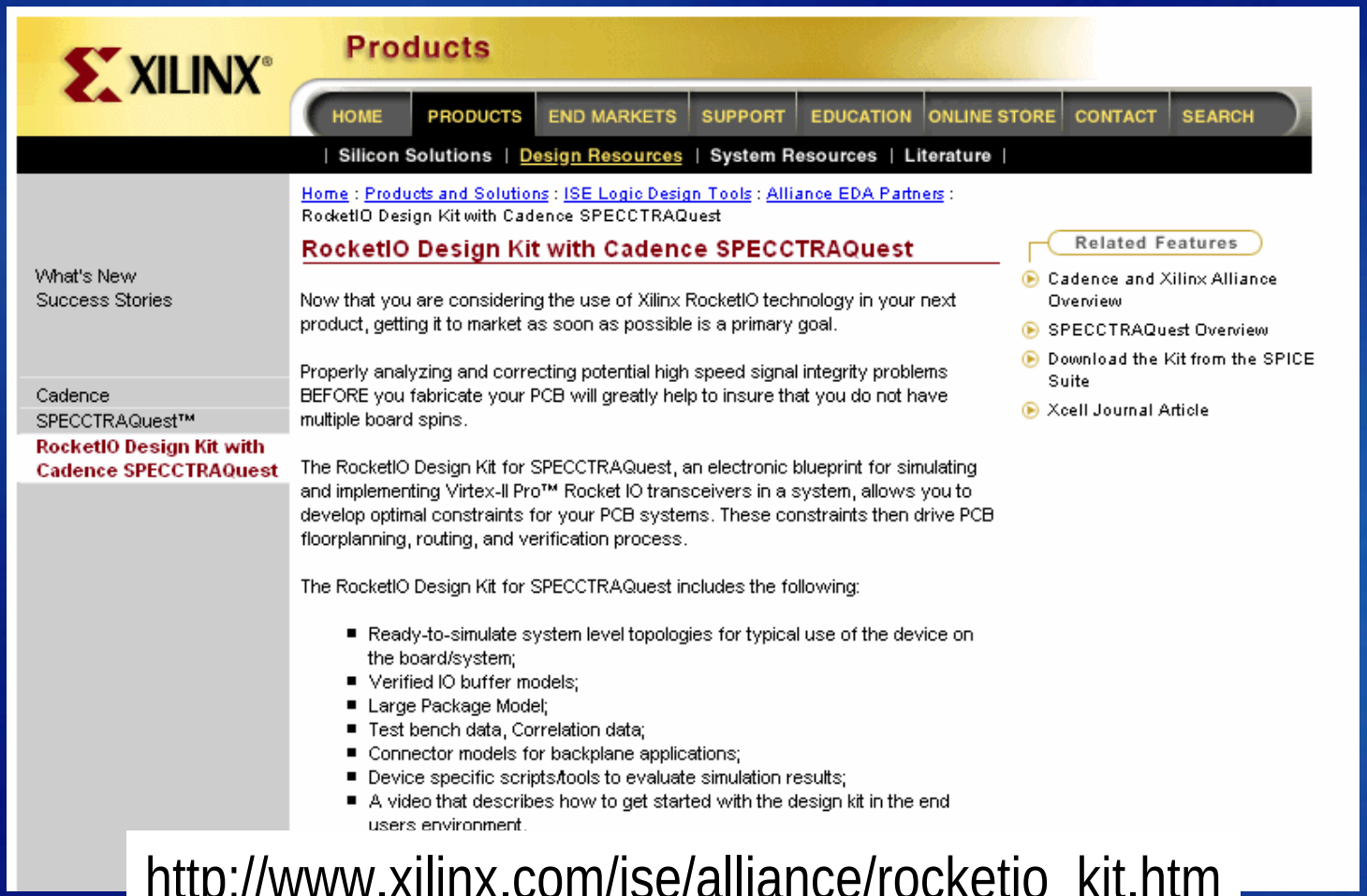
Design-in Kits Available Now



http://www.xilinx.com/ise/alliance/rocketio_kit.htm

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Summary

- Interconnect complexity and increasing speed
- Signal integrity is a mainstream design problem
- Simulation is the only way to first time design success
- Design-in kits get you designing product faster
- What are your IC suppliers doing to enable your product design?

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References

- SPECCTRAQuest high-speed design community
  - http://www.specctraquest.com
- Cadence Design Chain Optimization Initiative
  - http://www.cadence.com/feature/design_chain.html
- Articles & papers
  - http://www.specctraquest.com/Contribute/Solutions.asp
  - http://www.specctraquest.com/downloads/xc_speckit42.pdf
  - http://www.xilinx.com/publications/xcellonline/xcell_45/xc_cadence45.htm
- Webinars & movies
  - http://www.cadencepcb.com/promotions/designchain/jump.asp
  - http://www.specctraquest.com/Optimize/DesignKits.asp
  - http://www3.vcall.com/digitallava/cadence_alex_rm/audio_rm/main.htm

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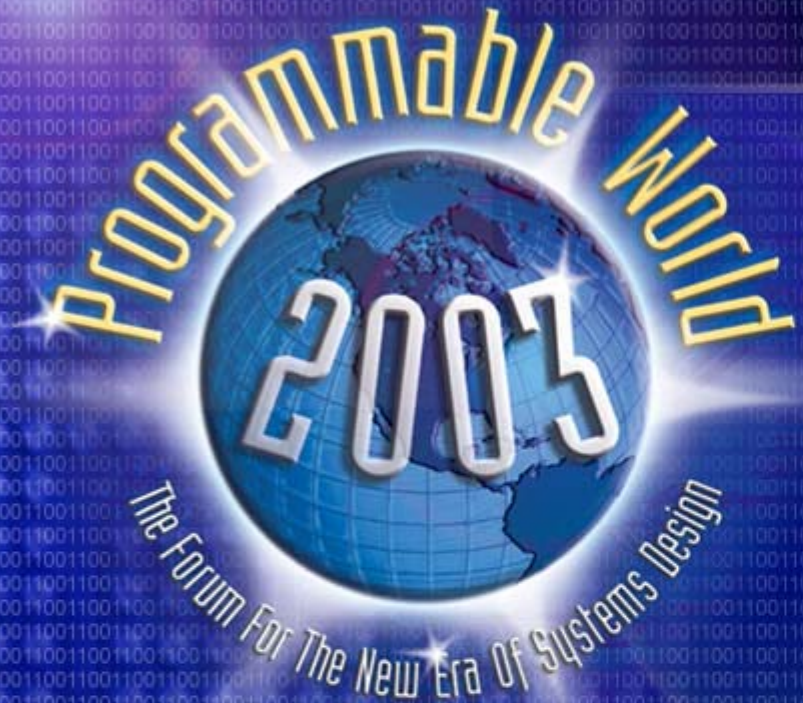


Thank You!

Cadence across silicon-package-board

Market Leader

2001 Total Revenue:	$1.43B
2001 Product Revenue:	$830M

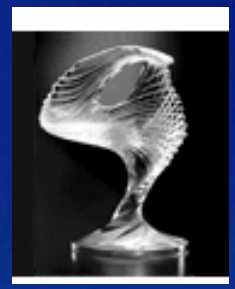
Global Business

North America	59%
Europe	21%
Japan/Asia	20%

>58 offices worldwide

Unmatched Resources

Total Employees:	5,600
Engineers:	>3,600
2001 R&D investment:	~$300M



IEEE Corporate Innovation Award Recipient for 2002

Rank	Company	Rev. # Mil.
1	Microsoft	25,296
2	Oracle	10,860
3	Computer Assoc.	4,198
4	Peoplesoft	2,073
5	Siebel Systems	2,048
6	Compuware	2,010
7	BMC Software	1,504
8	Veritas Software	1,492
9	Cadence Design	1,430
10	Electronic Arts	1,322

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