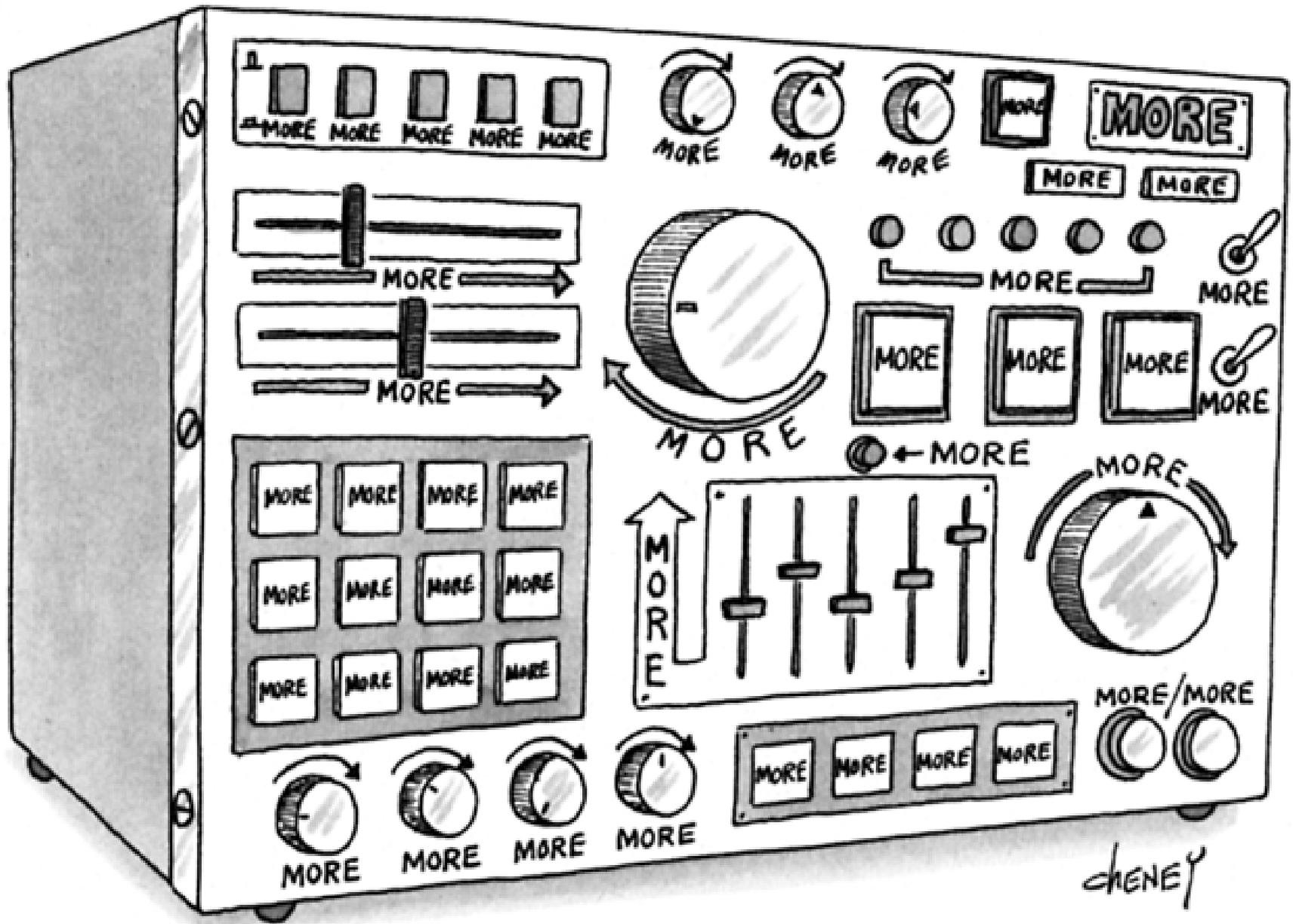


# New 10G Products from Xilinx

## 10 Gbps RocketPHY™ Family & Virtex-II Pro™ X Architecture



# Higher Bandwidth at Lower Cost

System Cost Requirements

Traditional I/O solutions unable to keep pace with core logic performance

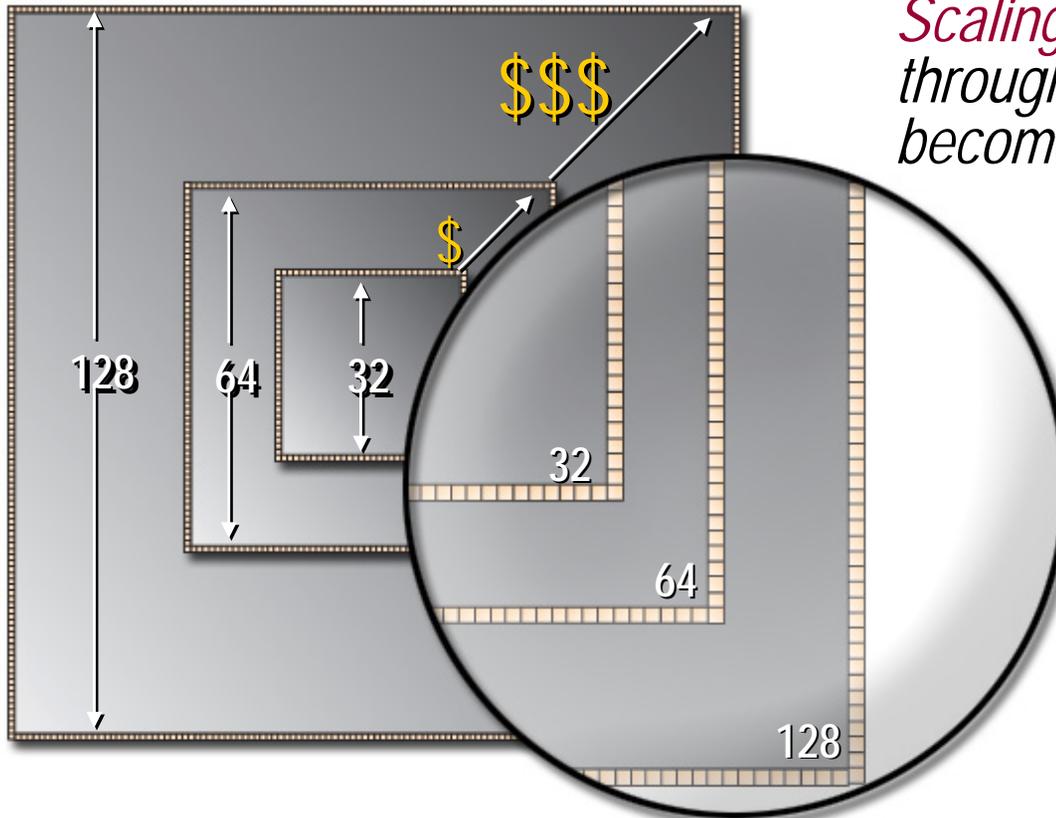
Bandwidth Requirements

Market pressures demand continued cost & bandwidth scaling

Time



# Traditional Scaling Reaches Limits



*Scaling bandwidth through increasing I/O becomes impractical*

# At 1 Gbps Parallel Signaling Hits a Brick Wall

- *Signal skew  $\ll 10\text{pS}$*
- *High Power Consumption*
- *Simultaneous Switching Noise*
- *Radiated EMI*

*The Solution is*  
**Serial...**



# The Benefits of Going Serial

- Significant pin-count consolidation
  - Component, PCB, and connector costs significantly reduced
- Reduced power consumption & EMI emissions
  - Low voltage differential signaling
- Simplified design
  - Integrated clock eliminates clock skew design challenges





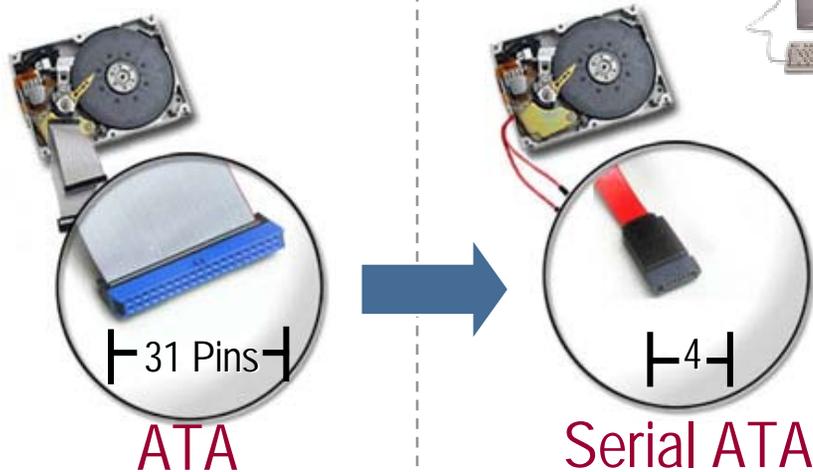
# The Serial Tsunami

- Benefits of serial technology driving a “Tsunami” of new connectivity standards...
- With multiple speeds, protocols, and connectors...
- Addressing multiple interconnect hierarchies...
  - Box-to-box, board-to-board, chip-to-chip, & chip-to-optics
- With rapid adoption across multiple markets.
  - Communications, Storage, Computing, Video, Industrial, Instrumentation, Consumer...

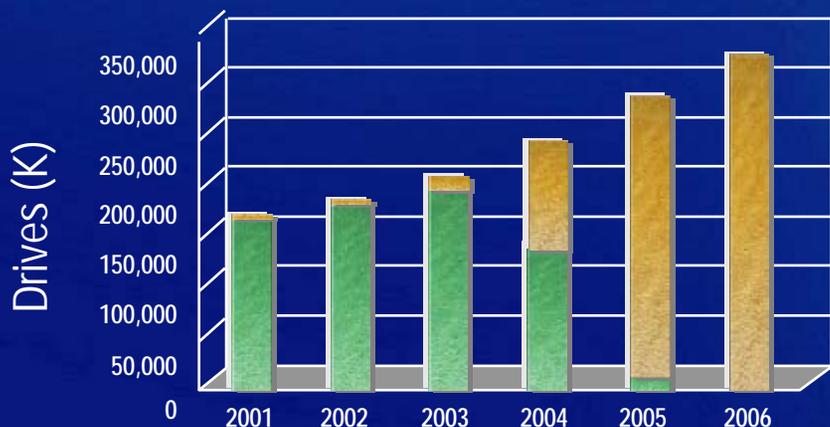
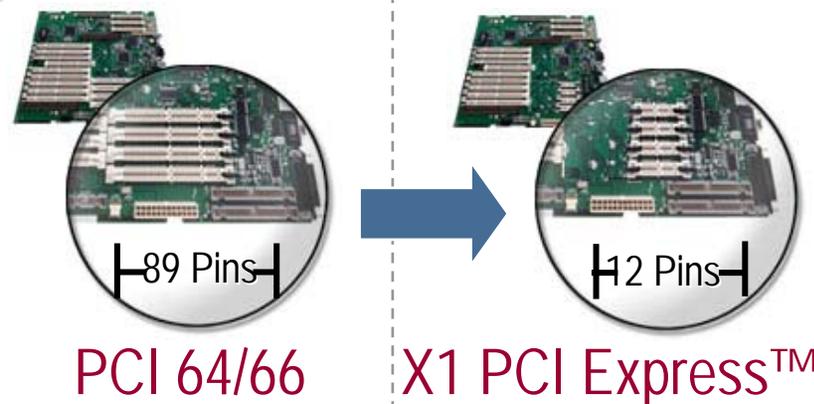


# Serial Signaling in Computers

## Hard Drives - ATA



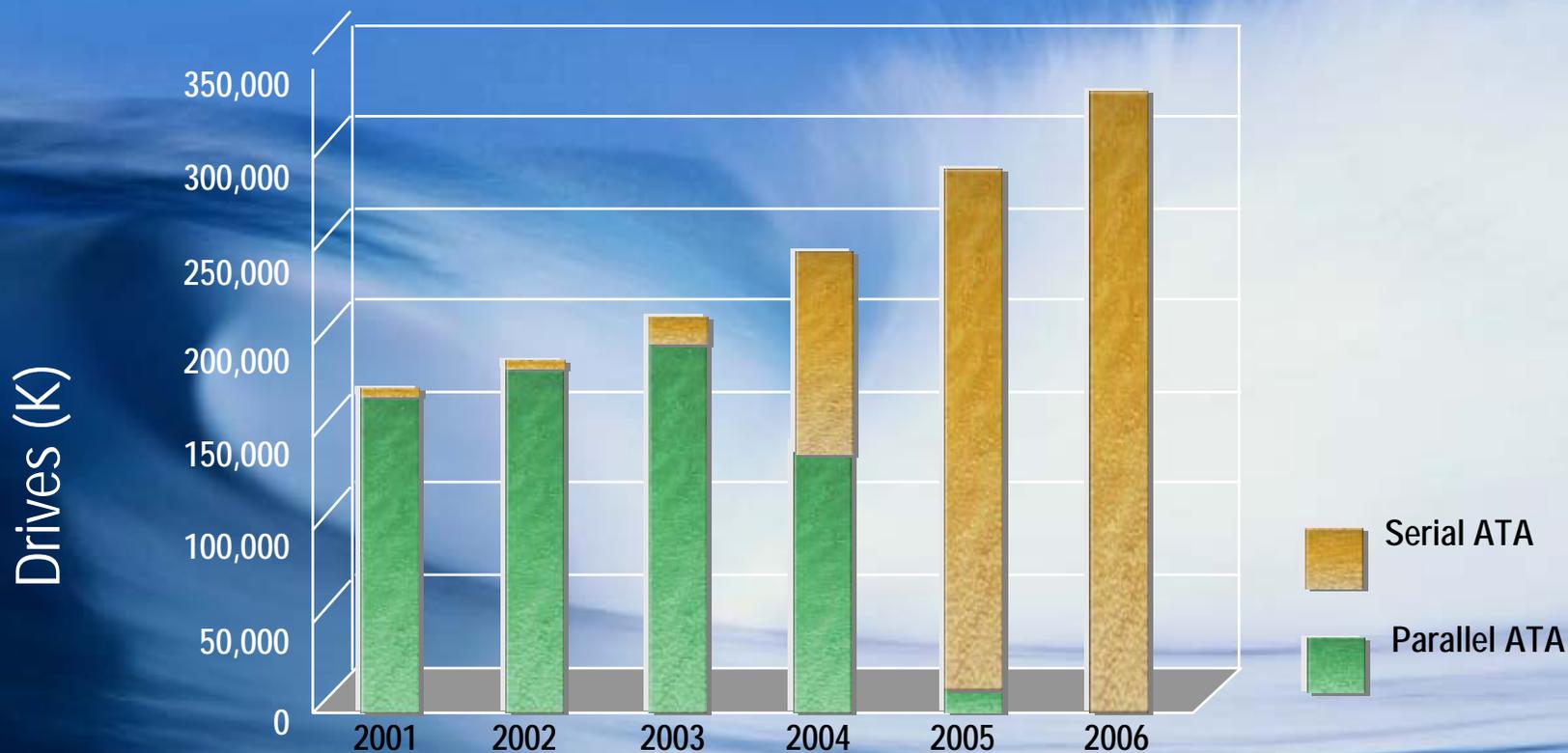
## Motherboards - PCI



Serial	0.0%	0.3%	7.3%	42.8%	95.6%	100.0%
Parallel	100.0%	99.7%	92.7%	57.2%	4.4%	0.0%



# Parallel → Serial ATA

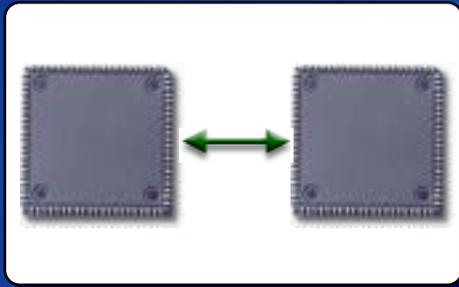


Serial	0.0%	0.3%	7.3%	42.8%	95.6%	100.0%
Parallel	100.0%	99.7%	92.7%	57.2%	4.4%	0.0%



# A Tsunami of Serial Standards

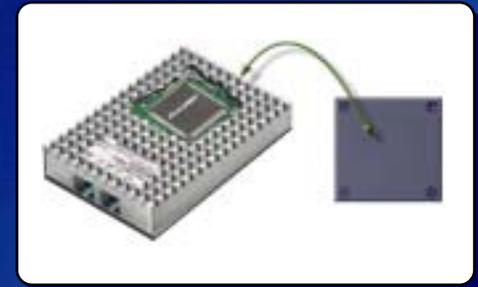
Chip-to-Chip



Board-to-Board



Chip-to-Optics

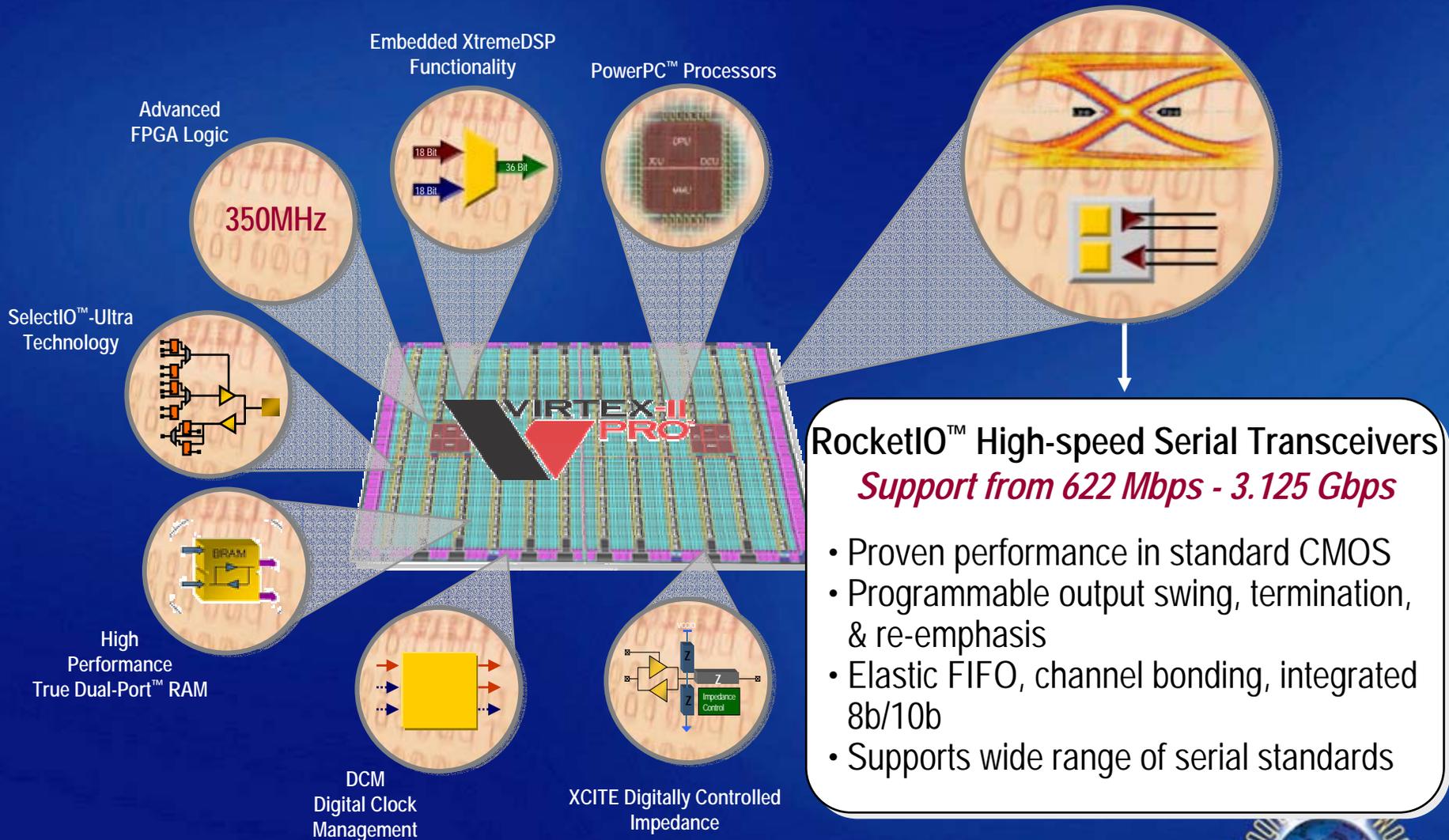


<b>SONET Backplane</b>	<b>2.488,</b>	<b>9.9532 Gbps</b>
<b>XAUI Backplane / Line Side</b>	<b>3.125 Gbps</b>	
<b>Ethernet Backplane</b>	<b>1.25,</b>	<b>10.3125 Gbps</b>
<b>Proprietary Backplane</b>	<b>1.25,</b>	<b>5.0, 6.25, 10 Gbps</b>
<b>InfiniBand™</b>	<b>2.5 Gbps</b>	
<b>Fibre Channel</b>	<b>1.0625,</b>	<b>2.125, 10 Gbps</b>
<b>Serial RapidIO™</b>	<b>1.25,</b>	<b>2.5, 3.125 Gbps</b>
<b>PCI Express™</b>	<b>2.5 Gbps</b>	
<b>SFI-5 / SPI-5</b>	<b>2.488 Gbps</b>	
<b>SFI- 4.2</b>	<b>2.5 Gbps</b>	

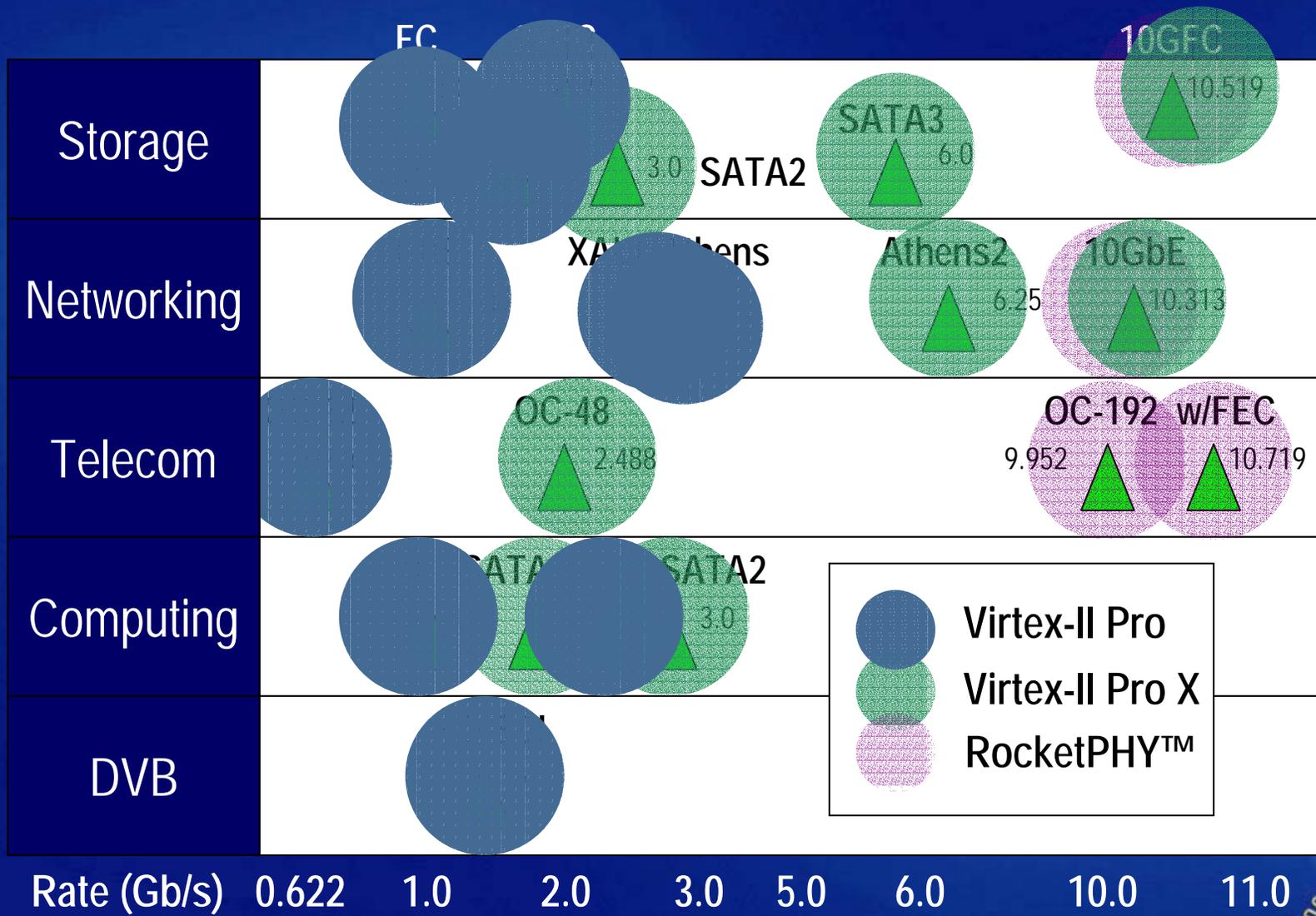


# The Virtex-II Pro Platform FPGA

Defining the Industry Standard for Cost, Performance, & Flexibility



# Multi-Gb Serial Terrain Map



# Extending Solutions Leadership to 10 Gbps

RocketPHY™

The logo for RocketPHY, featuring the word "Rocket" in a stylized, italicized font with a red-to-orange gradient, and "PHY" in a bold, red, sans-serif font. The text is set against a background of horizontal lines that create a sense of motion or speed.

SONET Compliant 10 Gbps  
CMOS Physical Layer  
Transceiver Family

Sampling  
NOW

Virtex-II Pro™ X

The logo for Virtex-II Pro X, featuring a large, stylized "V" composed of black and red geometric shapes. To the right of the "V" is the text "VIRTEX-II PRO" in a bold, sans-serif font, with "X" in a larger, red, stylized font below it.

Virtex-II Pro FPGA with  
integrated 10 Gbps

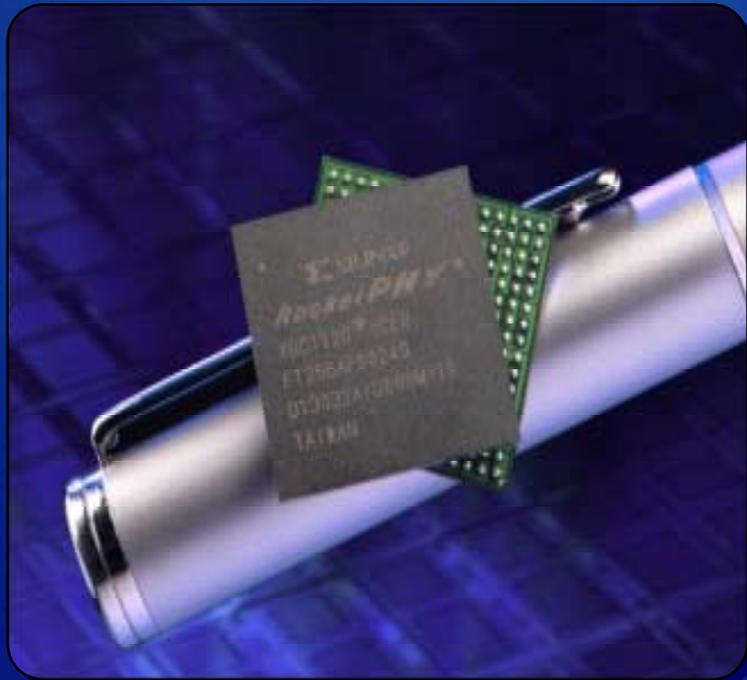
Sampling  
2H 03

Redefining the *Industry Standard* for  
*Programmable Solutions... Again*



# RocketPHY™ 10G

## Physical Layer Transceivers



- Single-Chip CMOS PHY Devices
- Ultra-low jitter ( $< 1.0$  ps RMS)
- **9.953 – 10.709** Gbps data rates
- Markets: WAN, MAN, LAN & SAN
  - SONET OC-192 (SDH STM-64) + FEC
  - 10GbE
  - 10G Fibre Channel
- 16-bit LVDS parallel interface
  - OIF SFI-4
  - XSBI IEEE 802.3ae compliant
    - DDR-XSBI Option
- FT256 BGA package



# RocketPHY™ Family

## RocketPHY™ 10G Ultra MSA



Multi-Rate OC-192+FEC/10GbE/10G FC with SFI-4/XSBI Interfaces

## RocketPHY™ 10G SONET / SDH



OC-192 SONET (STM-64 SDH) with SFI-4 Interface

## RocketPHY™ 10G Ethernet / Fibre Channel



10GE/10G FC Transceiver w/ 16-bit LVDS Interface (XSBI)

*Unparalleled solutions for 10 Gbps applications*



# The 10G Optical Revolution

## 300-pin MSA



RocketPHY supports  
both MSA & XFP  
applications

*RocketPHY*

## XFP MSA



- Traditional 10G MSA optical modules
  - 200 – 300 Pins, fixed wavelength, CWDM & Tunable Laser
  - Relatively high cost - \$1800 ++

- Driving lower cost through XFP
  - XFP – 10G Forum Factor Pluggable
  - Protocol agnostic – LAN, WAN, SAN
  - **1/5 of the space, 1/2 of the power, 1/3 of the cost**



# 300 MSA vs. XFP Cost Comparison

*Cost Benefits & Density will Drive Rapid XFP Adoption*

*2004 estimated pricing*

300-Pin MSA

**\$1800**



SFI-4 /  
XSBI



XFP

**\$700**

~ \$600



XFI

< \$100



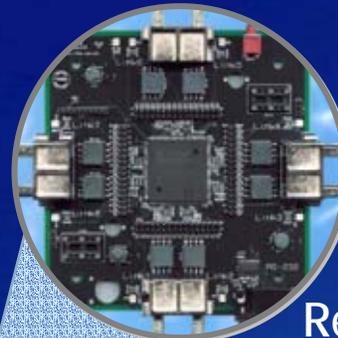
SFI-4 /  
XSBI



Save Over  
\$1000/Port

# Comprehensive Serial Solutions

Serial Specialist  
FAEs



Reference Designs  
& Eval Boards

**Comprehensive Solutions**  
to accelerate design time  
and tame the Serial Tsunami



Interoperability  
Certification



Comprehensive  
Characterization  
Reports

Advanced Serial  
I/O IC Design Team

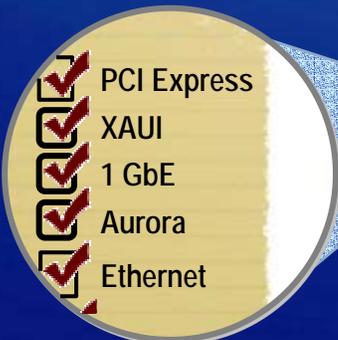


Serial Standards  
Signalling Support



PCI Express  
S. RapidIO  
XAUI  
1 GbE  
BackPlane  
1 G F/C

Serial Standards  
Protocol & IP



PCI Express  
XAUI  
1 GbE  
Aurora  
Ethernet



# CTD Video



# Extending Solutions Leadership to 10 Gbps

RocketPHY™

The logo for RocketPHY, featuring the word "Rocket" in a stylized, italicized font with a red-to-orange gradient, and "PHY" in a bold, red, sans-serif font. The text is set against a background of horizontal lines that create a sense of motion or speed.

SONET Compliant 10 Gbps  
CMOS Physical Layer  
Transceiver Family

Sampling  
NOW

Virtex-II Pro™ X

The logo for Virtex-II Pro X, featuring a large, stylized "V" composed of black and red geometric shapes. To the right of the "V" is the text "VIRTEX-II PRO" in a bold, sans-serif font, with "X" in a larger, red, stylized font below it.

Virtex-II Pro FPGA with  
integrated 10 Gbps

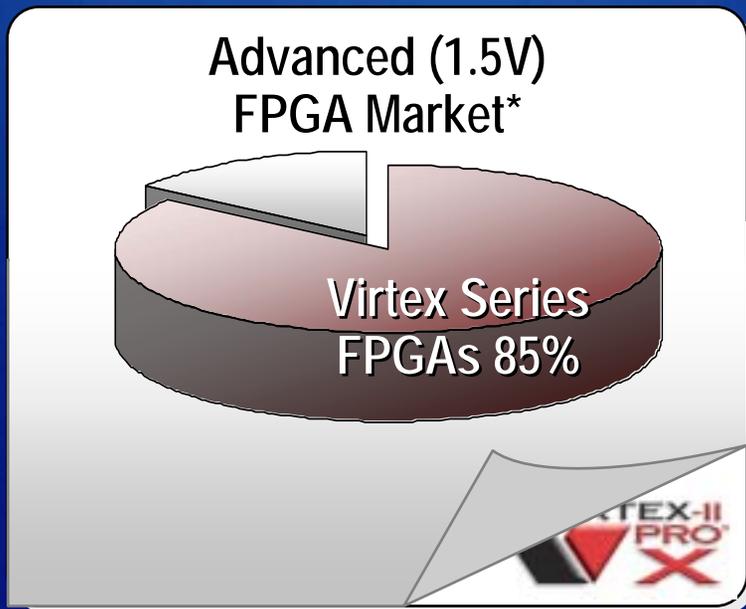
Sampling  
2H 03

Redefining the *Industry Standard* for  
*Programmable Solutions... Again*



# Virtex-II Pro X Architecture

Virtex Series  
Industry's most popular  
Platform FPGA solution

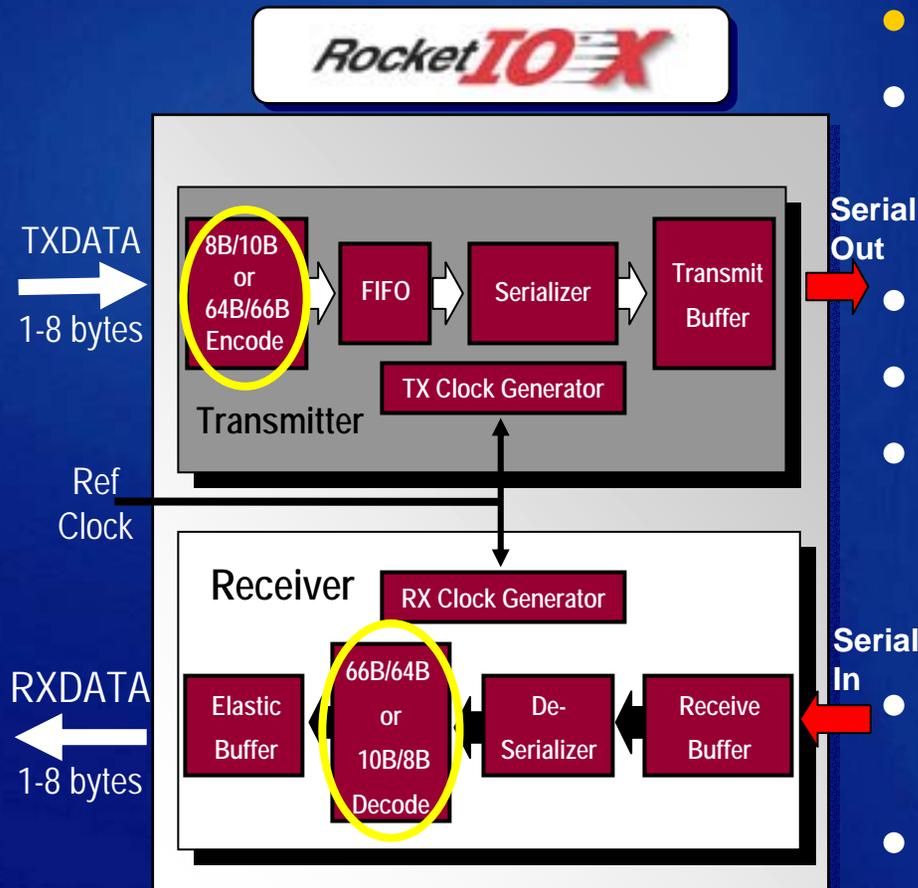


- Extends most popular Platform FPGA family to 10Gbps serial
- Fully compatible with Virtex-II Pro
  - Same architecture
  - PowerPC processors cores
  - Pin-compatible
- Virtex-II Pro & Virtex-II Pro X = complete solutions from 622 Mbps to 10 Gbps
  - Chip-chip, board-board, chip-optics
  - New architecture ideally suited for 5/6/10 Gbps backplanes, 10G Base-R, and OC-48 compliant systems

\*Source: Company Reports, Xilinx Estimates Q1-Q4 CY '02 market data for 1.5 V FPGAs  
Note: Share base estimates based on Top 2 vendors only: Altera and Xilinx (represent >90% of market)



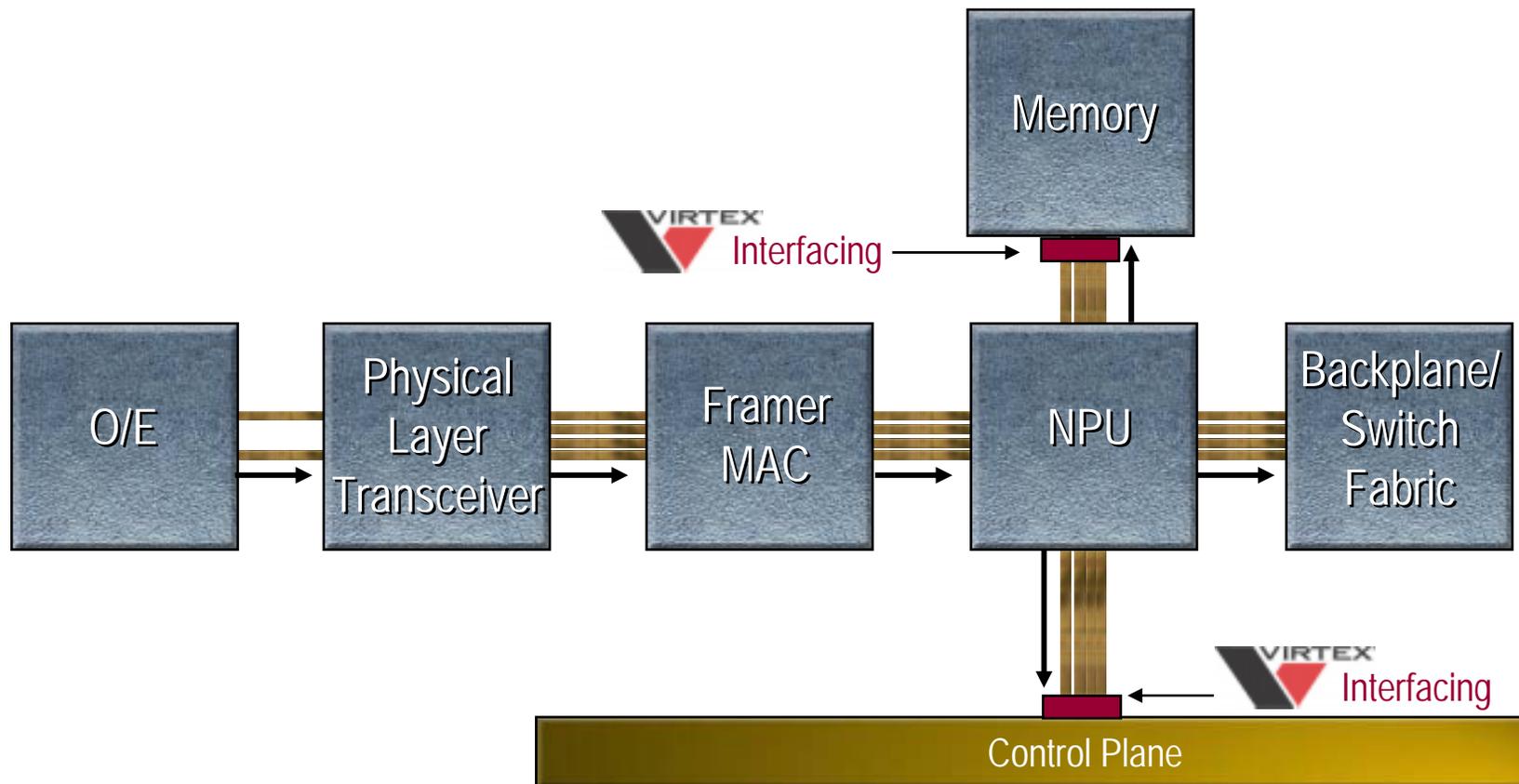
# RocketIO™ X Transceiver



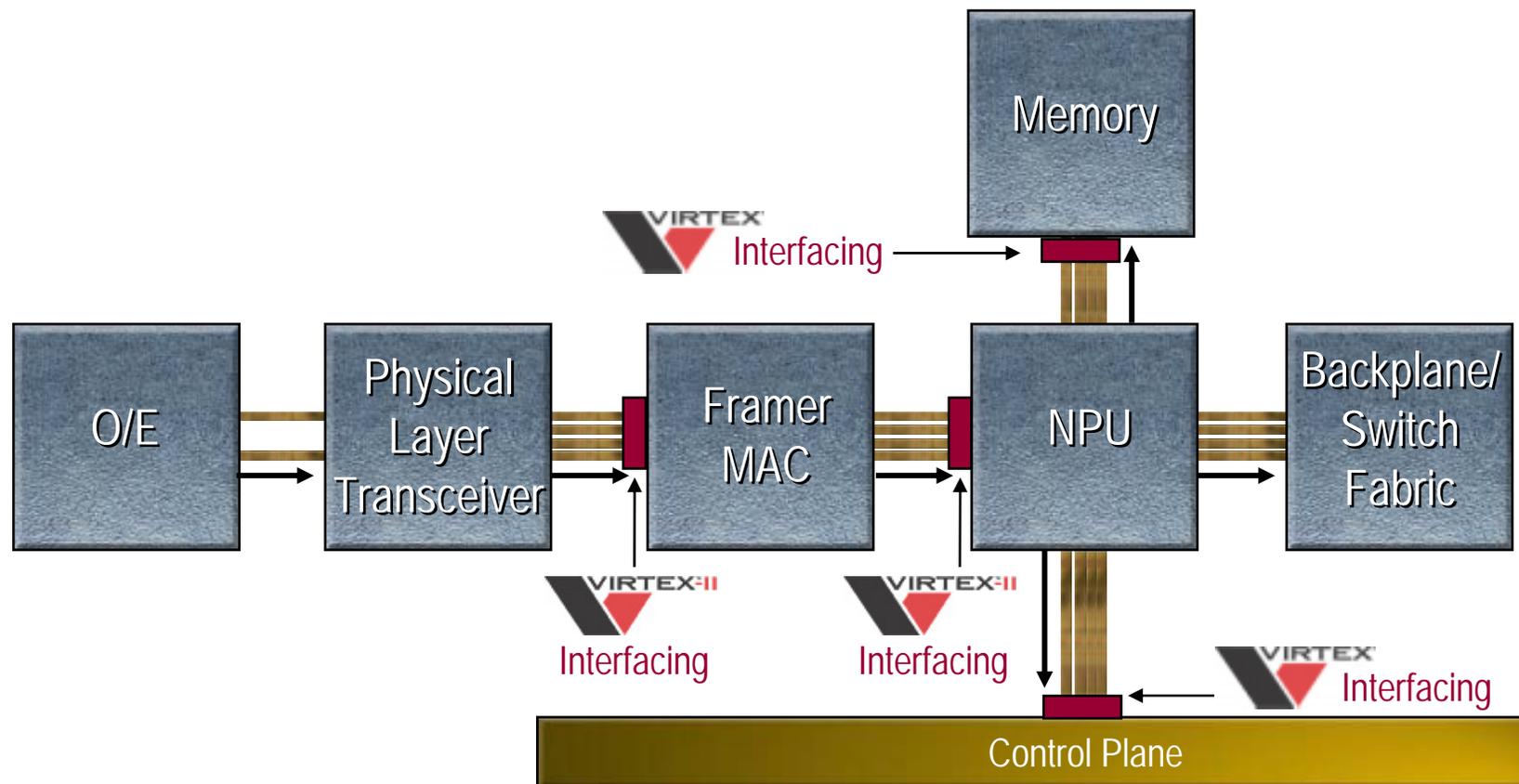
- 2.488 - 10.3125 Gbps per channel
- Enhanced SONET support
  - 8B/10B or 64B/66B encoding
  - x16 or x20 clock and data path
- Channel bonding
- Comma detect
- Programmable features for performance tuning and enhanced signal integrity
  - Pre-emphasis, receive equalization, output swing, and on-chip termination
- Bypass for encoding, FIFO, elastic buffer
- Built-in 10G Base-R circuitry
- Transceiver configuration port



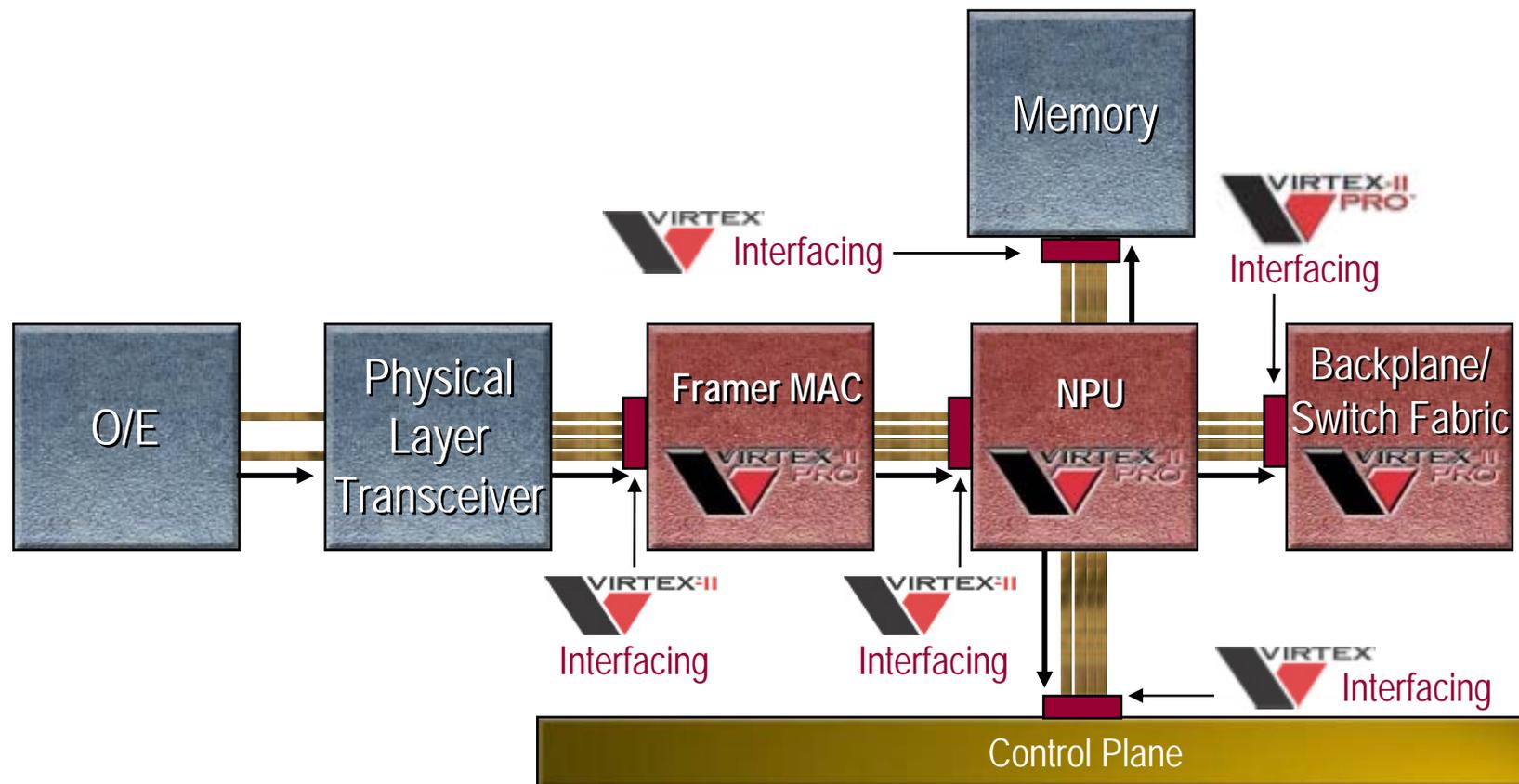
# A Continued Commitment to Delivering Solutions



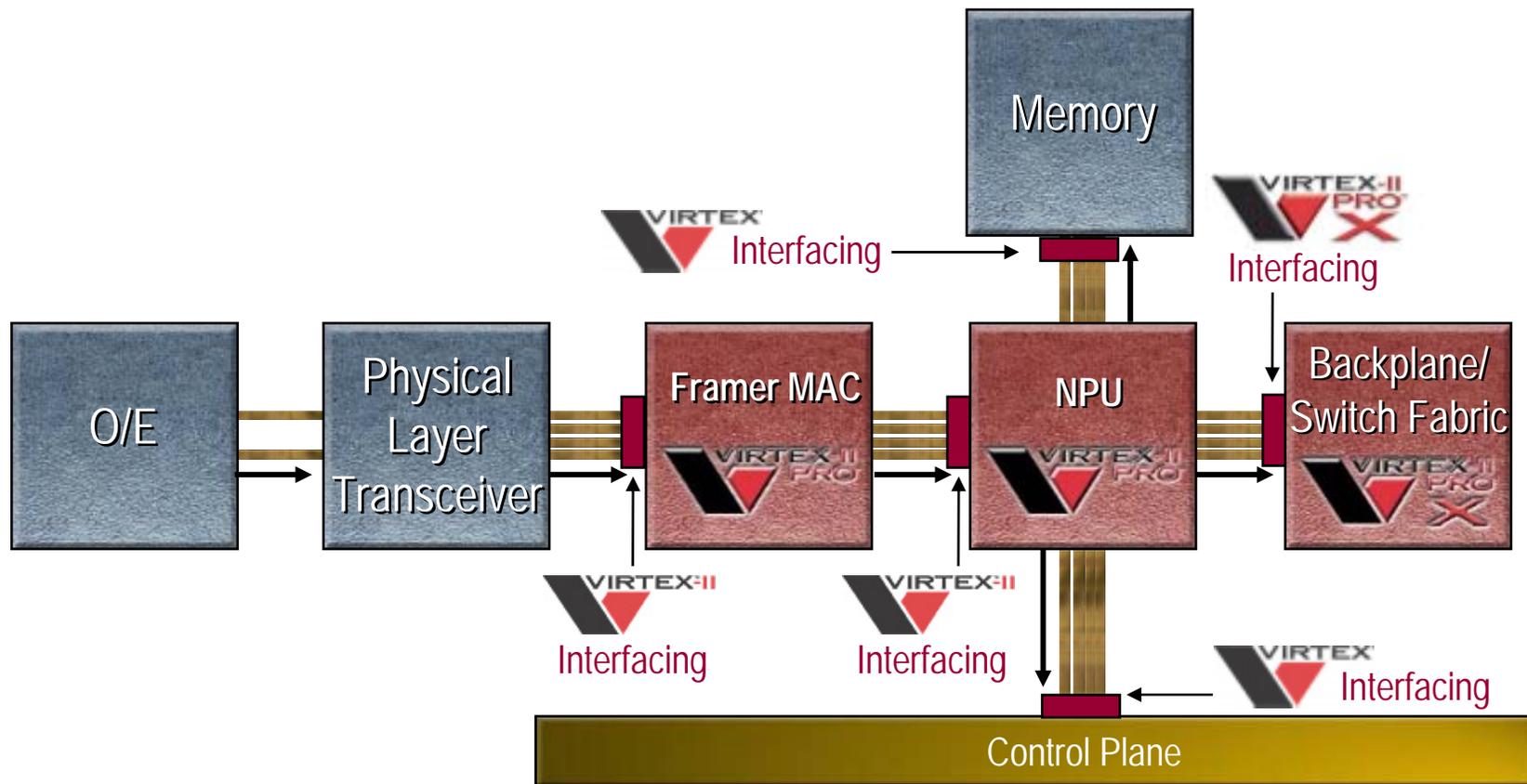
# A Continued Commitment to Delivering Solutions



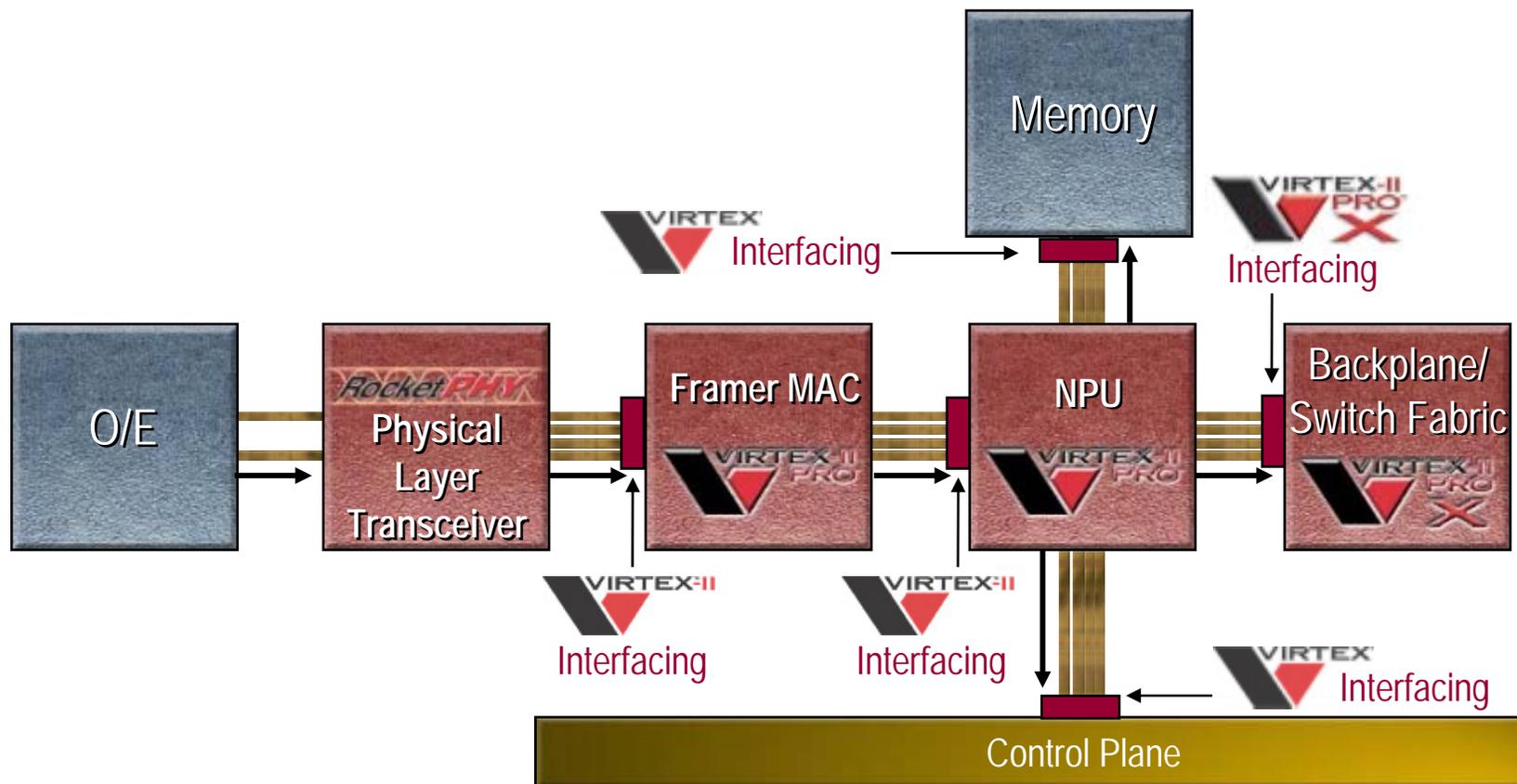
# A Continued Commitment to Delivering Solutions



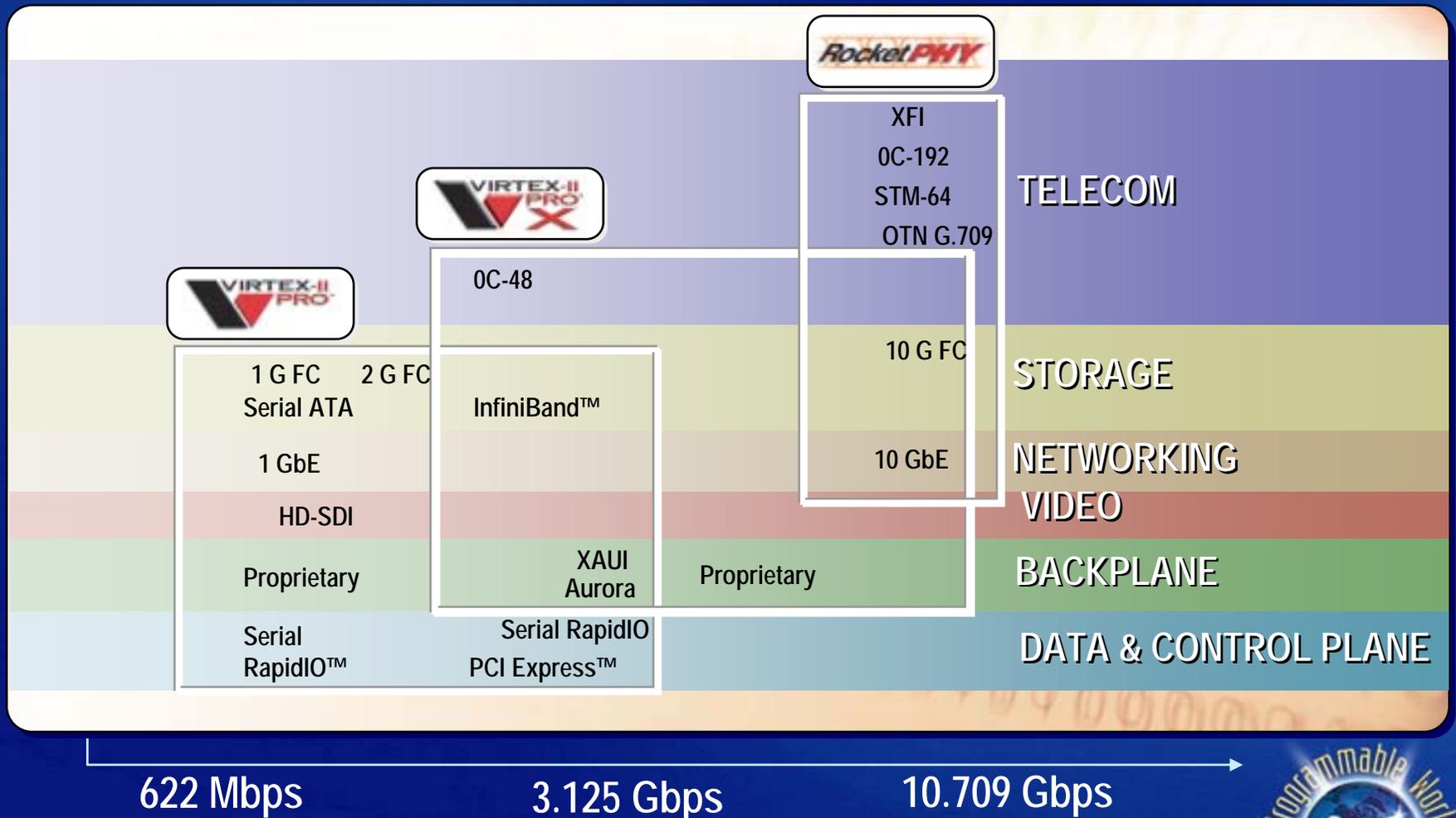
# A Continued Commitment to Delivering Solutions



# A Continued Commitment to Delivering Solutions



# Seamless Serial Solutions from 622 Mbps to 10 Gbps





# Summary

- Serial delivers higher bandwidth at lower cost
  - Driving Factor of the “Serial Tsunami”
  - Computing, Networking, Telecom, Storage, Video, Industrial, Military
- Xilinx committed to providing complete serial solutions
  - Silicon, Software, IP, Boards, Technical Support, Design Services
  - Covering speeds from 622 Mbps to 10 Gbps
  - Support for 14 connectivity standards
- Complete Range of Devices
  - Virtex-II Pro (9 Devices)
  - RocketPHY™ Family (3 Devices)
  - Virtex-II Pro X (coming in 2H03)

