



# Virtex-E Package Compatibility Guide

*This package compatibility guide describes the Virtex-E pin-outs and establishes guidelines for package compatibility between Virtex and Virtex-E devices.*

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The 1.8V Virtex-E FPGA family combines 0.18 mm technology with a synthesis-friendly silicon architecture to provide a new level of FPGA performance and density. Virtex-E FPGA availability in packages compatible with Virtex FPGAs allows systems to migrate from using Virtex family devices to Virtex-E family devices. Package pinout and pin functionality differences between Virtex-E and Virtex FPGAs are covered in this article.

## Power Supplies

As with the Virtex family, the Virtex-E positive supply is divided into two separate power supplies: VCCO and VCCINT. VCCO powers output pins and LVTTTL, LVCMOS, and PCI output and input pins. VCCINT powers internal logic and all input pins except LVTTTL, LVCMOS, and PCI inputs.

The Virtex-E VCCINT is 1.8V (while the Virtex VCCINT is 2.5V). This is a result of more advanced processing and 0.18 mm design rules, which also offer reduced die size, reduced power consumption, and increased speed. VCCO is adjustable, up to 3.3V, depending on the I/O standard used.

Voltage regulator modules with programmable output voltages can be used to power the VCCO and VCCINT inputs and accommodate the lower 1.8V VCCINT in the Virtex-E family.

## I/O Standards

Virtex-E devices can be used with 20 high-performance interface standards, including the LVDS and LVPECL differential signalling standards. A new LVCMOS I/O standard based on 1.8V VCCO is also supported. All I/O pins are 3V tolerant, and can be 5V tolerant with an appropriate external resistor. PCI 5V is not supported. Table 1 shows a complete listing of the supported I/O standards.

## I/O Banking

There are eight I/O banks in the Virtex-E family, as in the Virtex family, and each bank has multiple VCCO pins. All of the VCCO pins in one bank must be connected to the same voltage level, as determined by the I/O standard in use.

In Virtex-E devices the banking rules are different because the input buffers with LVTTTL, LVCMOS, and PCI standards are powered by VCCO instead of VCCINT. For these standards, only input and output buffers that have the same VCCO can be mixed together in the same bank.

## Low Voltage Differential Signals

The Virtex-E family incorporates differential signalling (LVDS and LVPECL). Two pins are utilized for these signals to be connected to a Virtex-E device. These are known as differential pin pairs. Each differential pin pair has a Positive

I/O Standard	Output VCCO	Input VCCO	Input VREF	Board Termination Voltage (VTT)
LVTTL	3.3	3.3	N/A	N/A
LVC MOS2	2.5	2.5	N/A	N/A
LVC MOS18	1.8	1.8	N/A	N/A
SSTL3 I & II	3.3	N/A	1.50	1.50
SSTL2 I & II	2.5	N/A	1.25	1.25
GTL	N/A	N/A	0.80	1.20
GTL+	N/A	N/A	1.0	1.50
HSTL I	1.5	N/A	0.75	0.75
HSTL III & IV	1.5	N/A	0.90	1.50
CTT	3.3	N/A	1.50	1.50
AGP-2X	3.3	N/A	1.32	N/A
PCI33_3	3.3	3.3	N/A	N/A
PCI66_3	3.3	3.3	N/A	N/A
BLVDS/LVDS	2.5	N/A	N/A	N/A
LVPECL	3.3	N/A	N/A	N/A

Table 1 - Supported I/O Standards

(P) and a Negative (N) pin. These pairs are labeled in the following manner:

I/O\_L#[P/N]

where L = LVDS or LVPECL pin

# = Pin Pair Number

P = Positive

N = Negative

I/O pins for differential signals can either be synchronous or asynchronous, input or output. The pin pairs can be used for synchronous input and output signals as well as asynchronous input signals. However, only some of the differential pairs can be used for asynchronous output signals.

Differential signals require the pins of a pair to switch almost simultaneously. If the signals driving the pins are from IOB flip-flops, they are synchronous. If the signals driving the pins are from internal logic, they are

asynchronous. Table 2 defines the names and function of the different types of differential pin pairs in the Virtex-E family.

Pin Name	Description
IO_L#[P/N] Example: IO_L22N	Represents a general I/O or a synchronous input/output differential signal. When used as a differential signal, N means Negative I/O and P means Positive I/O.
IO_L#[P/N]_Y Example: IO_L22N_Y	Represents a general I/O or a synchronous input/output differential signal, or a part-dependent asynchronous output differential signal.
IO_L#[P/N]_YY Example: O_L22N_YY	Represents a general I/O or a synchronous input/output differential signal, or an asynchronous output differential signal (for all devices within the same package.)
IO_LVDS_DLL_L#[P/N] Example: IO_LVDS_DLL_L16N	Represents a general I/O or a synchronous input/output differential signal, or a differential clock input signal or a DLL input. When used as a differential clock input, this pin is paired with the adjacent GCK pin. The GCK pin is always the positive input in the differential clock input configuration.

Table 2 - Differential Pin Pairs

Part	Package	Pins	Virtex	Virtex-E
XCV200	FG456	E11, U11	I/O	No Connect
		B11, AA11	No Connect	IO_LVDS_DLL
XCV300	BG432	B26, C7, F1, F30, AE29, AF1, AH8, and AH24	No Connect	VCCINT
XCV400	FG676	D13, Y13	I/O	No Connect
		B13, AF13	No Connect	IO_LVDS_DLL
XCV400/600	PQ240/HQ240	P215, P87	IO_VREF	IO_LVDS_DLL
		P216, P86	I/O	IO_VREF
All	PQ240/HQ240	P232, P207, P176, P146, P116, P85, P55, and P25	I/O	VCCO
		P231	I/O	IO_VREF

Table 3 - Virtex Family Compared to Virtex-E Pin-out Differences

## Differential Clock Pins

In addition to the four GCLKs in the Virtex family, the Virtex-E family has four IO\_LVDS\_DLL pins that can be paired with GCLKs to support up to four differential clocks. A differential clock input pair always includes one GCLK and the adjacent IO\_LVDS\_DLL pin. The GCLK pin is always the positive input in differential clock input configurations.

When differential clocks are not in use, these IO\_LVDS\_DLL pins can be used as single-ended I/Os or as DLL input pins.

## DLL Input Pins

Four additional DLL input pins (IO\_LVDS\_DLL) can be used as inputs to the DLLs, for a total of eight usable inputs for DLLs in the Virtex-E family. This is very useful in clock mirroring applications.

## Pinout Differences

The Virtex-E and Virtex families are pin-compatible with some minor exceptions as shown in Table 3. Some of the exceptions are described below:

- XCV200E Device, FG456 Package - The Virtex-E XCV200E has two I/O pins swapped with the Virtex XCV200 to accommodate differential clock pairing.
- XCV300E Device, BG432 Package - The Virtex-E XCV300E has eight pins (B26, C7, F1,

F30, AE29, AF1, AH8, and AH24) connected to VCCINT that are no-connect in the Virtex XCV300.

- XCV400E Device, FG676 Package - The Virtex-E XCV400E has two I/O pins swapped with the Virtex XCV400 to accommodate differential clock pairing.
- All Devices, PQ240 and HQ240 Packages - The Virtex devices in PQ240 and HQ240 packages do not have VCCO banking, but Virtex-E devices do. To achieve this, eight Virtex I/O pins (P232, P207, P176, P146, P116, P85, P55, and P25) are now VCCO pins in the Virtex-E family. This change also requires one Virtex IO\_VREF pin to be swapped with a standard I/O pin.

Additionally, accommodating differential clock input pairs in Virtex-E caused some IO\_VREF differences in the XCV400E and XCV600E devices only. Virtex IO\_VREF pins P215 and P87 are Virtex-E IO\_VREF pins P216 and P86, respectively. Virtex-E pins P215 and P87 are now IO\_LVDS\_DLL.

## Conclusion

Though the new Virtex-E family has many enhancements, it can easily be interchanged with the Virtex family, with only minor considerations. ☒

This information is subject to change. For the latest information, see the Xilinx web site at <http://www.xilinx.com>.