XH3 HardWire ASIC
Industry's First "FpgASIC"

March 1998 | Product Description

Features

- 0.5µ CMOS Gate Array
- Two Metal Routing Options
- Maximum of 140,000 Gates
- Maximum Total Pads: 352
- 5 V Operation
- Input Modes: CMOS, TTL, PCI
- Output Modes: Normal, 3-state, Bi-directional, Meets PCI Spec
- Output Drive FPGA Compatible
- Average Gate Delay 0.16 ns (typ) for 2 Input NAND (fanout = 2)
- Input Buffer 1.5 ns (max) Commercial
- Output Buffer 3.6 ns (max) Commercial
- RAM Single: Synchronous and Asynchronous, Dual Port: Synchronous
- Full Scan Test >95% Fault Coverage Most Devices
- Built-in JTAG Capacity
- Built-in POR, Oscillator, Global Buffering
- Built-in Configurable Control Logic
- Exact FPGA-Compatible I/O Cells
- Speed Grades to -09
- Pre-Verified LogiCOREs
- Drop-in Configuration Emulation
- Package Change Flexibility

FPGA Support

- XC4000E
- XC4000EX
- Flexible Packaging Options

Product Overview

The Xilinx HardWire™ XH3 products represent the first true FPGA specific ASIC, or "FpgASIC" family. These devices are state-of-the-art 0.5µ (5V) optimized gate arrays specifically designed to support ASIC versions of Xilinx XC4000E and XC4000EX product lines. Each XH3 device contains ASIC versions of critical FPGA features actually built into the base gate array silicon. Because of the exact match in feature set, Xilinx can guarantee form, fit and function equivalence from the FPGA to the XH3 HardWire ASIC.

System designers can now take advantage of FPGA flexibility for system design, debug, and pre-production, and then achieve lowest total system cost for volume production by converting the FPGA to a HardWire ASIC, using the Xilinx turnkey conversion service. FPGA features and density have reached a point where FPGAs can be considered for complex system level design and integration. The Xilinx HardWire family backs that up with advanced technology and a no-risk conversion. In addition, The XH3 HardWire ASICs are tuned to support Xilinx LogiCORE technology, including the PCI core.

Table 1 describes the six devices in the XH3 ASIC family. Each device has been optimized to support popular Xilinx FPGA packages through the appropriate maximum pad count. Packages from the PC84 to BG432 are supported. Pinouts and packages are the same as their FPGA counterparts.

Gate counts support the latest FPGA devices, even those configured with large amounts of on-chip RAM and high CLB utilization.

For device pinouts, package drawings, and other technical specifications, see the Xilinx Programmable Logic Data Book.

Design Flow

Because Xilinx starts the conversion process with a complete, placed and routed FPGA, the process is completely turnkey. Unlike traditional ASIC flows, Xilinx does not require simulation and test vectors, back annotation or rigorous customer verification of translated, re-routed net lists.

Traditional post-route timing data (Back-annotated SDF) data is not needed or available.

XH3 ASIC Architecture

The XH3 family is a 0.5µ gate array architecture using Xilinx design rules and Xilinx qualified process technology. The core devices use an enhanced ASIC architecture that optimizes both logic and routing density with highly-tuned drive and logic cells. All Xilinx XC4000E/EX I/O characteristics can be exactly replicated in the FpgASIC HardWire device. Crucial Xilinx features are actually built into the base array layers of the XH3 devices, as shown in Figure 1. The Xilinx-specific JTAG ring is built into the silicon, which allows for flawless conversion from the programmable JTAG implementation to the HardWire ASIC version. It eliminates the silicon overhead penalty usually associated with traditional JTAG gate array implementations.

Table 1: XH3 FpgASIC Family Chart

	Device					
	XH302	**XH304**	**XH306**	**XH308**	**XH310**	**XH312**
Usable Gates - DLM	14,000	25,000	45,000	70,000	90,000	140,000
Pads (Max)	136	172	204	240	292	352
Packages Supported	PC84 PQ100 TQ100 VQ100	PC84 PQ100 TQ100 VQ100 TQ144 PQ160	TQ144 PQ160 PQ208	PQ208 PQ240 BG225	PQ240 BG225 BG256	PQ240 PQ304 BG352 BG432
FPGAs Supported (Example)	XC4005 XC4008 XC4010 XC4013	XC4013 XC4020 XC4025 XC4028	XC4020 XC4025 XC4028	XC4028 XC4036	XC4028 XC4036	XC4036

The XH3 die also contains some of the key FPGA features built into the corners of the die itself. Global buffers, power-on-reset (POR) circuitry and configuration control are designed into the actual uncommitted base array. This minimizes any mismatch between FPGA and HardWire ASIC features, and reduces the need to "add on" features that are not required on every FPGA device. Overall, conversion time is optimized, and the potential for FPGA to HardWire ASIC mismatches in technology or implementation are virtually eliminated.

Xilinx uses a patented Universal Configuration Emulation megafunction (UCE) to reproduce any Xilinx supported configuration mode in the HardWire ASIC. A similar Universal I/O function (UIO) is also implemented in each XH3 device to act as a completely compatible I/O controller. The UCE and UIO functions are fully automatic and help to reduce both functional mismatches and design conversion time.

Timing in a HardWire ASIC will be equal to or faster than that of its programmable equivalent. When the SRAM based elements, long lines and routing are replaced with the metal via's of a gate array, the timing improvements can be dramatic. Xilinx guarantees that every HardWire conversion will be a form, fit, and functional equivalent to the corresponding FPGA device. It is important to make sure that from a chip level, board level, and system level perspective, the potential increase in speed will not cause unwanted race conditions or SSO (simultaneously switching outputs) problems.

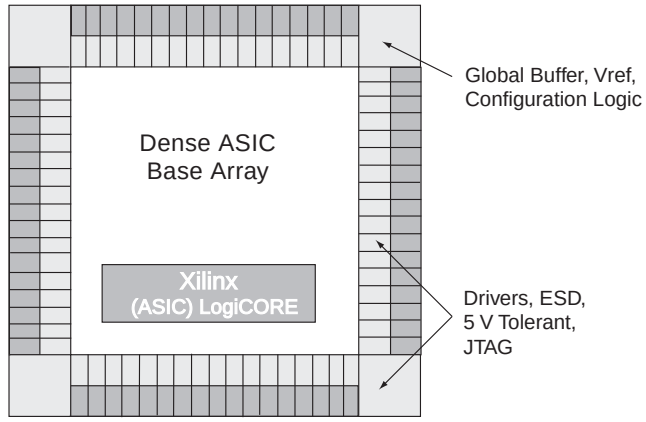

Figure 1: XH3 HardWire FpgASIC Architecture

XH3 Power Estimation

Xilinx HardWire ASIC devices usually require far less power than their programmable equivalent. In many cases, packages can be switched from a high performance heat-sinked version to the less expensive plastic equivalent. Exact power estimation can only be determined after the FPGA to ASIC conversion has been completed. Power consumption can be estimated however, using the formula in Table 2. Parameter definitions are found in Table 3.

Table 2: Power Estimation

$P_m = 1.40 \times N_m \times Ps_m \times [1/2 \times C_m \times VDD^2 \times F]$

$P_O = 1.25 \times N_O \times Ps_O \times [1/2 \times C_O \times VDD^2 \times F]$

$P_i = 1.40 \times N_i \times Ps_i \times [1/2 \times C_i \times VDD^2 \times F] = [N_i \times (0.5\ mA) \times VDD$

$P_c = 1.25 \times N_c \times [C_c \times VDD^2 \times F]$

$P_t = P_m + P_o + P_i + P_c$

Table 3: Parameter Definitions

P_m	Power consumption due to core (Watts)
P_o	Power consumption due to output buffers (Watts)
P_i	Power consumption due to input buffers (Watts)
P_c	Power consumption due to clock buffers (Watts)
P_t	Total power consumption (Watts)
F	The clock frequency (MHz)
N_m	Number of CLB's x 15
C_m	.54 x 10^{-12} (FARAD)
Ps_m	The percentage of core macros switching in a clock cycle (default 10%)
N_o	Total number of output buffers in the design
C_o	50 x 10^{-9} (FARAD)
Ps_o	The percentage of output buffers switching in a clock cycle (default 40%)
N_i	Total number of input buffers in the design
C_i	.54 x 10^{-12} (FARAD)
Ps_i	The percentage of input buffers switching in a clock cycle (default 40%)
N_c	Total number of clock buffers in the design
C_c	Number of FF's on the clock net x 0.54 x 10^{-12} (FARAD)
VDD	Power supply (Volts)

Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, Tj = -0°C to +85°C	Commercial	4.75	5.25	V
	Supply voltage relative to GND, Tj = -40°C to +100°C	Industrial	4.5	5.5	V
V_{IH}	High-level input voltage	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}

Note: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.

DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0 mA, V_{CC} min	TTL outputs	2.4		V
	High-level output voltage @ I_{OH} = -8.0 mA, V_{CC} min (note 4)	TTL outputs	2.4		V
	High-level output voltage @ I_{OH} = -1.0 mA, V_{CC} min	CMOS outputs	V_{CC} -0.5		V
V_{OL}	Low-level output voltage @ I_{OL} = 4.0 mA, V_{CC} min (notes 1 & 3)	TTL outputs		0.4	V
		CMOS outputs		0.4	V
	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} min (notes 1 & 3)	TTL outputs		0.4	V
		CMOS outputs		0.4	V
	Low-level output voltage @ I_{OL} = 24.0 mA, V_{CC} min (notes 1 & 3)	TTL outputs		0.4	V
		CMOS outputs		0.4	V
RPU	Pull-up resistor at VCC = 5V		20	250	kΩ
RPD	Pull-down resistor at VCC = 5 V		20	250	kΩ

Symbol	Description		Min	Max	Units
I_{CCO}	Quiescent supply current (note 2)	CMOS		10	µA
		TTL		10	ma
I_L	Input of output leakage current		-10	+10	µA
CIN	Input capacitance (sample tested)	Plastic packages		10	pF
		Ceramic packages		16	pF

Notes: 1. With up to a maximum of 64 output pins sinking current simultaneously.
2. With no output current loads, no ac, all package pins at V_{CC} or GND level.
3. I/O combination options
Category I: XC4000, XC4000E, and XC4000XE Series compatible:
VOH sourcing 4 mA, and VOL sinking 12mA.

Operation Features

Input Modes	CMOS, TTL, PCI
Output Modes	Normal, 3-state, Bidirectional Meets PCI Spec
Output Drive	FPGA Compatible
Average Gate Delay	0.16ns (TYP) for 2 input NAND (fanout = 2)
Input Buffer	1.5ns (max) Commercial
Output Buffer	3.6ns (max) Commercial
RAM	Single: Synchronous and Asynchronous Dual Port: Synchronous

Absolute Maximum Ratings

Symbol	Description			Units
V_{CC}	Supply voltage relative to GND		-0.5 to +7.0	V
V_{IN}	Input voltage relative to GND (note 1)		-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output (note 1)		-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic	+150	°C
		Plastic packages	+125	°C

Notes: 1. Maximum DC overshoot or undershoot above V_{CC} or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to V_{CC} +2.0 V, provided this overshoot or undershoot lasts less than 20 ns.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.