Virtex-E High Performance Differential Solutions: Low Voltage Differential Signalling (LVDS)

Introduction

As the need for higher bandwidth accelerates, system designers are choosing differential signaling to satisfy high bandwidth requirements while reducing power, increasing noise immunity, and decreasing EMI emissions. LVDS is a low swing, differential signaling technology providing very fast data transmission, common-mode noise rejection, and low power consumption over a broad frequency range. The Virtex-E family delivers the programmable industry's highest bandwidth and most flexible differential signaling solution for direct interfacing to industry-standard LVDS devices.

With up to 36 I/O pairs operating at 622 Megabits per second (Mb/s) or up to 344 I/O pairs operating at over 311 Mb/s, the Virtex-E family supports multiple 10 Gb/s ports while maintaining high signal integrity with low power consumption. Unlike other PLD solutions, all Virtex-E LVDS I/Os support input, output, and I/O signaling, providing a system designer unparalleled flexibility in board layout. Table 1 summarizes the LVDS support in the Virtex-E family.

Table 1: Virtex-E High-Bandwidth LVDS Support Summary

LVDS Configuration	Bandwidth
Point-to-Point	36 pairs @ 622 Mb/s or 344 pairs @ 311 Mb/s
Multi-Drop	344 pairs @ 311 Mb/s

The LVDS Standard

LVDS is defined by two industry standards: ANSI/TIA/EIA-644 and IEEE 1596.3 SCI-LVDS.

- The ANSI/TIA/EIA-644 standard defines LVDS electrical specs including driver output and receiver input electrical characteristics. It does not cover functional specifications, protocols, or transmission medium characteristics since these are application dependent. The ANSI/TIA/EIA-644 is the more generic of the two standards, and is intended for multiple applications.
- The IEEE 1596.3 SCI-LVDS standard is a subset of SCI (Scalable Coherent Interface). The SCI-LVDS standard defines electrical specifications for the physical layer interface of SCI. It is similar to the ANSI/TIA/EIA-644 standard but differs in the intended usage of the interface. The IEEE committee created the SCI-LVDS standard for communication between SCI nodes.

The Virtex-E LVDS solution conforms to the ANSI/TIA/EIA-644 standard. Table 2 summarizes the pertinent Virtex-E LVDS DC specifications.

Table 2: LVDS DC Specifications

DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}		2.375	2.5	2.625	V
Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.25	1.425	1.6	V
Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.9	1.075	1.25	V
Differential Output Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	250	350	450	mV
Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.25	1.375	V
Differential Input Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25 V	100	350	NA	mV
Input Common-Mode Voltage	Differential input voltage = ± 350 mV	0.2	1.25	2.2	V

Advantages

- LVDS is specified to be technology and process independent.
- LVDS is EMI tolerant. Common-mode noise is equally removed by two conductors and rejected by the receiver.
- No transmission medium is defined in the standard. The medium can be tailored to meet the specific application requirements.
- The typical LVDS voltage swing is 350 mV, resulting in a higher transfer rate and lower power consumption.

Configurations

There are two configurations that are used in LVDS applications, point-to-point and multi-drop. The Virtex-E family supports both LVDS configurations.

Point-to-Point

In point-to-point configuration, there is one transmitter and one receiver. The LVDS driver is a current source that drives a differential pair of lines. The typical current drive is 3.5 mA. The receiver has high DC impedance. The majority of the driver current flows across the termination resistor generating about 350 mV at the receiver inputs (Figure 1).

Multi-Drop

A multi-drop LVDS configuration has one transmitter and multiple receivers. The differential termination resistor is placed close to the last receiver (Figure 3).

Applications

Applications for LVDS include:

- Switches
- Repeaters
- Hubs
- Routers
- Wireless base stations
- Flat panel displays
- Digital cameras
- Printers
- Copiers

- Multimedia peripherals
- Backplane applications

Terminations

LVDS is widely used for high-speed point-to-point interface as well as multi-drop applications. Depending on the exact interconnect topology, precision resistors are required to match specific impedance characteristics to minimize reflection and ensure high signal integrity. The Virtex-E family supports the most flexible LVDS high-speed interface by supporting a flexible external termination scheme. This enables system designers select resistor values most appropriate for maximum performance.

Point-to-Point

Figure 1 shows the schematic of a standard LVDS driver driving the Virtex-E receiver. An LVDS driver drives the two 50 Ω transmission lines into a Virtex-E LVDS receiver. The two 50 Ω single-ended transmission lines can be micro-strip, strip-line, a 100 Ω differential twisted pair, or a similar balanced differential transmission line.

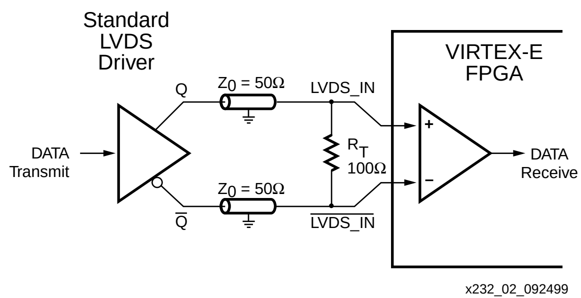

Figure 1: A Standard LVDS Driver Driving a Virtex-E LVDS Receiver

Figure 2 shows the complete schematic of the Virtex-E LVDS line driver and receiver. The standard LVDS 100 Ω termination resistor is connected across the LVDS_OUT and $\overline{\text{LVDS\_OUT}}$ outputs at the end of the transmission line. The resistors R_S and R_{DIV} attenuate signals from the Virtex-E LVDS drivers and provide a matched source impedance (series termination) to the transmission lines. Standard termination packs are available from **Bourns**. Other resistor vendors provide termination networks with up to 16-pins per pack.

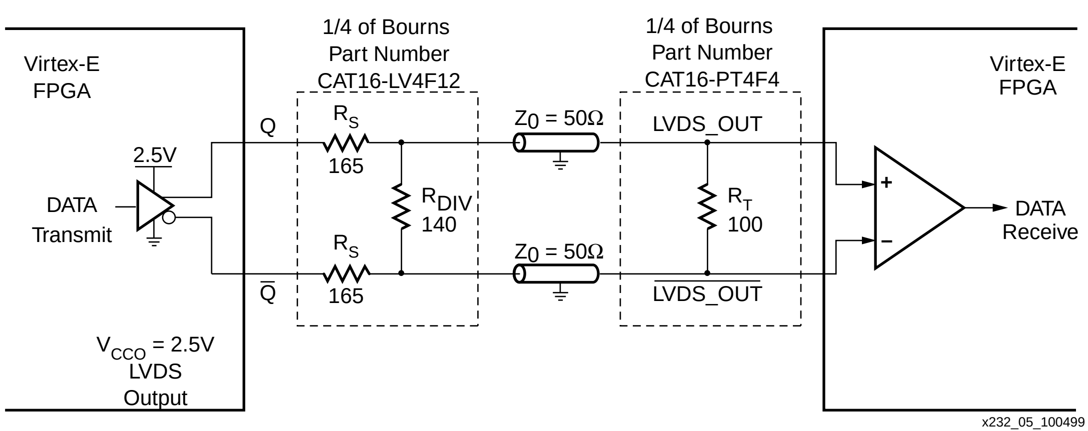

Figure 2: Virtex-E LVDS Line Driver and Receiver Schematic

Virtex-E LVDS driver meets ANSI/TIA/EIA-644 LVDS DC specifications. The matched source impedance of the Virtex-E LVDS driver absorbs nearly all differential reflections from the capacitive load at the LVDS destination, reducing standing waves, undershoot, and signal swing on data bursts or clocks.

Data and clocks can be transmitted over cables longer than 5 ns electrical length, limited only by the quality of the cable (the cable attenuation caused by skin effect losses at high frequencies).

The 622 Mb/s data rate, or 311 MHz clock is achievable with a Virtex-E -7 speed grade devices. See "**XAPP233: LVDS Transceivers at 622 Mb/s using General-Purpose I/O**" for details of the reference design.

Multi-Drop

Multi-drop LVDS configuration allows many receivers to be driven by one Virtex-E LVDS driver. With simple source and differential termination, Virtex-E LVDS driver can drive lines with fan-outs of 20 to 1, making Virtex-E LVDS I/Os suitable for a broad variety of high-load applications.

Figure 3 illustrates a Virtex-E LVDS driver driving 20 LVDS receivers in a multi-drop configuration. The receivers can be either Virtex-E receivers or other off-the-shelf LVDS receivers. The LVDS signal is driven from a Virtex-E LVDS driver, and is daisy-chained with two 29 Ω transmission lines and stubs to all 20 LVDS receivers. Each LVDS receiver is connected to the main multi-drop lines every 2.5" for a multi-drop line length of 50". Each LVDS receiver tap line has a 1" maximum stub length with a 50 Ω transmission line impedance to ground, or a differential impedance of 100 Ω between the two stubs. A 44 Ω termination resistor R_T is placed across the differential lines close to the last LVDS receiver. Resistors R_S and R_{DIV} attenuate the signals from the Virtex-E drivers and provide a 22 Ω source impedance (series termination) to the 29 Ω transmission lines. The 22 Ω source impedance is used because the added load of the LVDS receivers brings the 29 Ω line down to an effective average impedance of 22 Ω. The capacitor C_{SLEW} reduces the slew rate from the Virtex-E LVDS driver, resulting in smaller reflections and less ringing at the receivers.

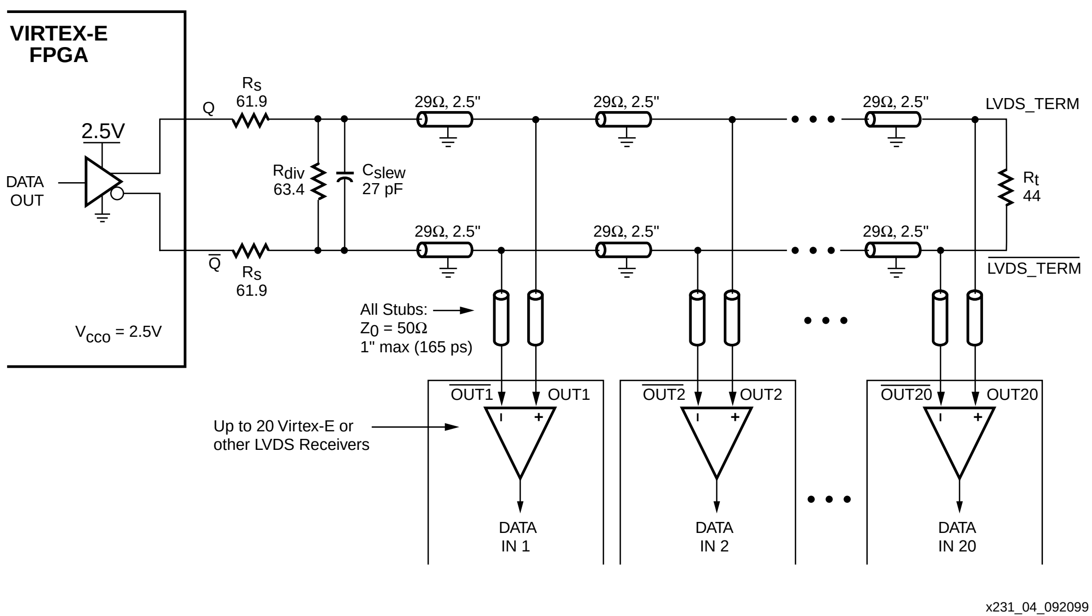

Figure 3: Virtex-E 20-load Multi-Drop LVDS Schematic

The two 29 Ω single-ended transmission lines can be micro-strip, strip-line, the single-ended equivalent of a 58 Ω twisted pair, or a similar balanced differential transmission line. The resistors R_S and R_{DIV} should be placed close to the Virtex-E driver outputs. The parallel termination resistor R_T should be placed close to the last LVDS receiver inputs at the far end of the multi-drop line. The capacitor C_{SLEW} should be placed close to the resistors R_S and R_{DIV}.

The Virtex-E multi-drop LVDS driver adheres to all the ANSI/TIA/EIA-644 LVDS standard DC input level specifications, and is fully compatible with LVDS receivers from National Semiconductor and other companies.

The maximum data rate is 311 Mb/s or a clock of 155.5 MHz for a Virtex-E -7 speed grade device. Reliable data transmission is possible for up to 20 LVDS receivers over a multi-drop line length of 50 inches, limited only by skin effect losses in the PCB trace.

Waveform

A typical LVDS output waveform for Virtex-E devices is shown in Figure 4.

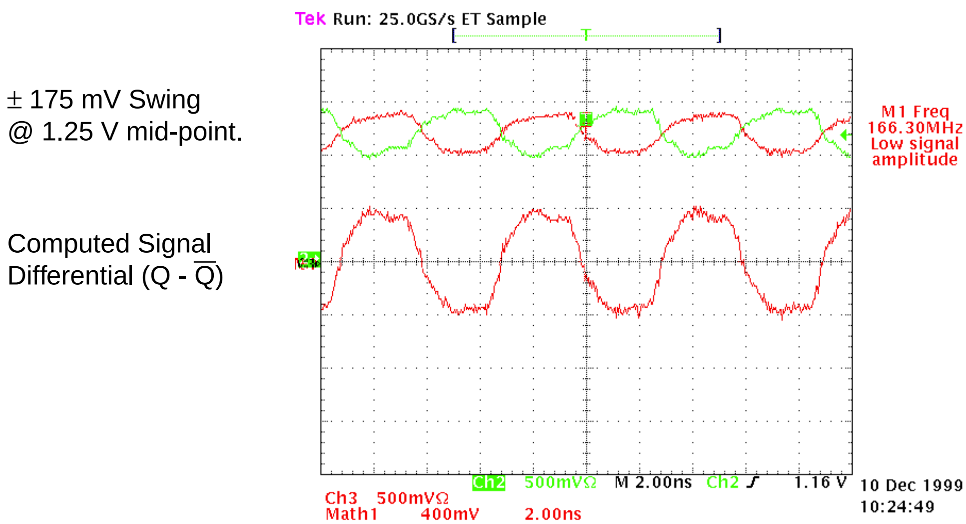

Figure 4: LVDS Output Waveform

Virtex Advantages

The Virtex-E devices are the first programmable logic devices available in the market incorporating advanced LVDS I/O capability with support for other differential standards (Bus LVDS and LVPECL). Unlike other announced architectures (for example, APEX E), the Virtex-E LVDS capability provides an abundance of LVDS-capable user I/O and clock pins, and the architectural flexibility shown in Table 3 to address true high-speed system issues. This capability works in concert with a robust delay locked loop (DLL) technology enabling designers to achieve maximum performance in their LVDS applications.

Table 3: Virtex-E High-Bandwidth LVDS Solution Summary

Feature	Virtex-E	APEX E
Offer LVDS as a standard feature	Yes, in all devices, packages, and speeds	Large "X" device only, fast speed only (More $$)
LVDS	Y	Y
Bus LVDS	Y	N
LVPECL	Y	N
LVDS Configurations	Point-to-point, Multi-drop, and Multi-point	Point-to-point and Multi-drop [1]
Maximum I/O Bandwidth	22 Gb/s (622 Mb/s/pair x 36 pairs) or 107 Gb/s (311 Mb/s/pair x 344 pairs)	10 Gb/s (622 Mb/s x 16 pairs)
Termination	Flexible External Termination	Inflexible Internal Termination on Outputs
High-Speed Differential Clock Pairs	4	1
Maximum # of differential pairs	344 In/Out	Dedicated 16 input and 16 output pairs. Not layout friendly.
Maximum Speed	622 Mb/s	622 Mb/s
Serializer/Deserializer	Flexible in CLB	Dedicated 8:1
Clock Recovery	N	N

1. APEX E has internal termination on the outputs and cannot guarantee high signal integrity due to an inability to impedance match.

Unlike other PLD solutions that only offer LVDS capability in the most expensive and highest speed grade options, the Virtex-E DLL and LVDS I/O capabilities are standard features available in all Virtex-E device/package combinations. The Virtex-E family offers the option to use up to 36 LVDS I/O pairs operating at 622 Mb/s or up to 344 LVDS I/O pairs operating at over 311 Mb/s to achieve over 100 Gb/s aggregate bandwidth. This enables system designers to support multiple 10 Gb/s ports architecture for high-performance DSP and data communication systems. Table 4 demonstrates the high-bandwidth LVDS solution provided by the Virtex-E family. In addition to offering a high-performance and highly flexible LVDS solution, Xilinx also works closely with other component vendors (e.g., Bourn for the resistor pack) to ensure inter-operability and help system designers further reduce the overall design complexity and system cost.

Table 4: Virtex-E High-Bandwidth LVDS Solution Summary

I/O Standard	Type	1	2	32	72	688
Virtex-E LVDS	Differential	NA	622 Mb/s	10 Gb/s	22 Gb/s	107 Gb/s
APEX E LVDS	Differential	NA	622 Mb/s	10 Gb/s	NA	NA

References

Standards

ANSI/TIA/EIA-644 **http://www.eia.org/eng**
IEEE1596.3 **http://www.ieee.org**

Related Xilinx Documents

XAPP230: "The LVDS I/O Standard" at: **http://www.xilinx.com/xapp/xapp230.pdf**
XAPP231: "Multi-drop LVDS" at: **http://www.xilinx.com/xapp/xapp231.pdf**
XAPP232: "The LVDS Drivers and Receivers: Interface Guidelines" at:
http://www.xilinx.com/xapp/xapp232.pdf

XAPP233: "LVDS Transceivers at 622 Mb/s using General Purpose I/O" at:
http://www.xilinx.com/xapp/xapp233.pdf