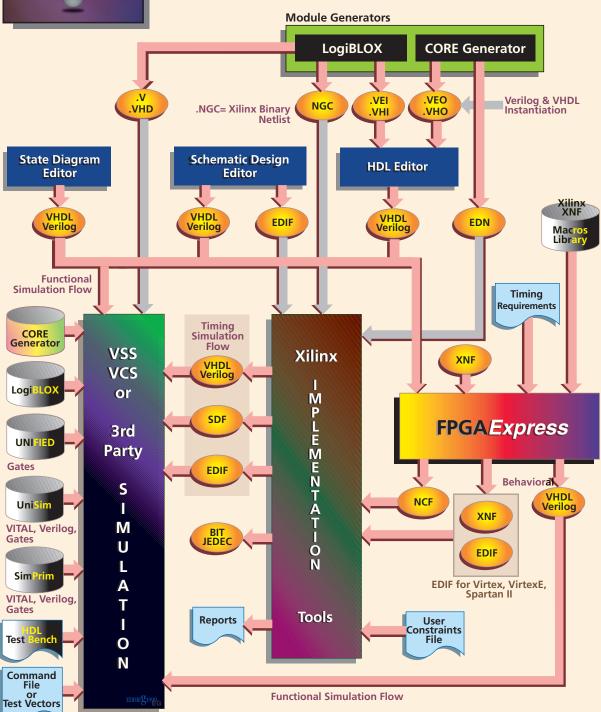




Synopsys FPGA Express Implementation Flow







Synopsys FPGA Express Information

Guide Overview

Device Architecture Support

FPGA Product Family

Spartan Virtex XC4000X

CPLD Product Family

XC9500

Xilinx Contacts and Technical Support

World Wide Web: http://www.xilinx.com

North America 1-800-255-7778 hotline@xilinx.com United Kingdom 44 1932-820821

ukhelp@xilinx.com

France

33 1-3463-0100 frhelp@xilinx.com

Japan

81 3-3297-9163 jhotline@xilinx.com

Synopsys Contacts and Technical Support

World Wide Web: http://www.synopsys.com

United States 1-800-245-8005

support_center@synopsys.com

Create a project

Go to menu File → New and define a new project. All HDL files processed by FPGA Express must be done through a project.

Add HDL files to project and analyze HDL files

After creating project, HDL design files can be added to the project. After adding the HDL design files, FPGA *Express* will automatically analyze the HDL files.

Implement the design

Select the top-level module/entity in the Design Sources window and the implement button will be highlighted.

Click on the implement button and specify the target die, speed grade and package. Strategies for synthesis can be specified during implementation.

Enter constraints

In the Chips window, select the implementation. Right-click on the selected implementation and select Edit Constraints. A window will appear where various constraints can be edited. After entering constraints, save constraints by closing the constraints window.

Optimize the design

Click on the **optimize** button located next to the implement button to synthesize the design OR select the menu **Synthesis** → **Optimize** Chip

Place & Route XNF or EDIF file with A2.1i

After optimization, write out the XNF or EDIF file by clicking on the Export Netlist button next to the implement button. Place and Route the XNF or EDIF file using A2.1i implementation tools with the Design Manager GUI or DOS shell based commands.