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July 1, 2000 (v1.0)

The Website is Always Current

Whenever Xilinx updates technical data on its products, the first place that information goes is to the Xilinx website. To find the absolutely latest technical product data from Xilinx, simply go to the following Web address:

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Aerospace and Defense CD-ROM

The Aerospace and Defense CD-ROM contains the complete Aerospace and Defense data book in PDF format (AD_databook.pdf) as well as the complete Data Book 2000 PDF version (databook.pdf). The Aerospace and Defense data book contains the complete versions of all QPRO data sheets. Double click on the AD_databook.pdf in the root directory and it will open to the Table of Contents.

Registration Advantage

Please take a moment to complete the registration section on the CD-ROM. This will ensure that you automatically begin to receive quarterly updates of the CD-ROM as they become available. By registering, you will receive the next updated CD-ROM free of charge and without any other action required on your part.

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Aerospace and Defense

Programmable Logic Data Book

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Section Titles

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Introduction
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QPRO High-Reliability QML Certified and Radiation Hardened Products for Aerospace and Defense Applications

June 15, 2000 (v2.1)

The High-Reliability Programmable Logic Leader

Xilinx is the leading supplier of High-Reliability programmable logic devices to the aerospace and defense markets. These devices are used in a wide range of applications such as electronic warfare, missile guidance and targeting, RADAR, SONAR, communications, signal processing, avionics and satellites. The Xilinx QPRO™ family of ceramic and plastic QML products (Qualified Manufacturers Listing), certified to MIL-PRF-38585, provide system designers with advanced programmable logic solutions for next generation designs. The QPRO family also includes select products that are radiation hardened for use in satellite and other space applications.

The Xilinx QPRO family addresses the issues that are critical to the aerospace and defense market:

- **Q**ML/Best commercial practices. Commercial manufacturing strengths result in more efficient process flows.
- **P**erformance-based solutions, including cost-effective plastic packages.
- **R**eliability of supply. Controlled mask sets and processes insure the same quality devices, every time, without variation, which remain in production for an extended time.
- **O**ff-the-shelf ASIC solutions. Standard devices readily available, no need for custom logic and gate arrays.

Table 1: **High-Density High-Performance and Radiation-Hardened Products**

Family	Devices	Features
XC/XQ4000/E/EX	XC4005/E XC4010/E XC4013/E XC4025E XQ4028EX	• 5,000-28,000+ gates • Up to 256 user-definable I/Os • Extensive system features include on-chip user RAM, built-in 1149.1 test support and fast carry logic
XQ4000XL	XQ4013XL XQ4036XL XQ4062XL XQ4085XL	• Up to 180,000 system gates • 3.3V, 5V-compatible I/O
XQR4000XL Radiation Hardened	XQR4013XL XQR4036XL XQR4062XL	• Up to 130,000 system gates • 60K-Rads total dose, latchup immune
Virtex	XQV100 XQV300 XQV600 XQV1000	• Up to 1,000,000 system gates, 2.5V
Virtex Radiation Hardened	XQVR300 XQVR600 XQVR1000	• 100K-Rads total dose, latchup immune

Unmatched Product Offering

The QPRO family provides a wide variety of devices, delivering the industry's fastest and biggest devices. The Virtex members of the QPRO family offers FPGAs with densities greater than 1,000,000 system gates, and even larger devices planned for the future. This broad range of devices is available in a wide variety of speed and package options. Both military temperature and full QML/SMD versions are available as standard off-the-shelf products. Select software cores, such as complete PowerPC peripherals, is also available.

Products for Space Applications

Xilinx offers the industry's only radiation hardened reconfigurable FPGAs for satellite and space. These devices are manufactured using an epitaxial wafer process, and have guaranteed total dose, latch up immunity, and low soft upset rates. These products allow for the ultimate in design and mission flexibility in a cost-effective manner.

QML Certification Part of Overall Quality Platform

Being certified to MIL-PRF-38535 QML complemented by ISO-9000 certification results in an overall product quality platform that makes Xilinx a world-class supplier of programmable logic devices. Designers can confidently design with Xilinx for High-Reliability systems with the knowledge they are getting unsurpassed quality and reliability, and long-term commitment to the aerospace and defense market.

Commitment to the Aerospace and Defense Market

Xilinx understands that our customers need to be able to count on their suppliers to be around for the long-term. Xilinx is committed to the long-term support of the aerospace and defense market, and we are continually expanding our product portfolio. Because our focus is in the form of a vertical market concept, we are able to provide emphasis on all of our customer's product requirements.

Software and Core Support for Xilinx QPRO High-Reliability Products

Component Selection

The Alliance™ and Foundation™ Series Xilinx core implementation software tool suites do not differentiate between Commercial, Industrial, and Military grade components. From the perspective of the implementation tools these are identical devices with identical architectures and available programming features. Therefore, there is no designation for QPRO or Radiation-Hardened devices in the available device selection menus. However, the High-Reliability product offering does typically include extended package selections to include available ceramic packages.

To select a Hi-Rel device for implementation the user should specify the commercial equivalent along with the specific package selection. Table 2 shows an example of Hi-Rel components and the corresponding device selections that should be specified in the software.

Table 2: **Hi-Rel Device Selections**

Target Device	Device Selection
XQVR1000 CG560-4	XCV1000 CG560-4
XQV300 CB228-4M	XCV300 CB228-4
XQ4085XL HQ240-1N(1)	XC4085XLA HQ240-1
XQR4062XL CB228-3	XC4062XL CB228-3

Notes:

1. The XQ4085XL is the only XQ4000XL series device that uses an XLA rather than XL designation.

Speed Grades

When making a device selection in the implementation tools, always select a speed grade that corresponds to the specific target device. In other words, a “-4” speed grade is still a “-4” regardless of whether it is a Commercial, Industrial, or Military grade part.

The AC characteristics and guaranteed timing specifications for a given device are specified per a specific speed grade. However, these parameters do not vary per product grade (i.e., Commercial, Industrial, Military, or other). Therefore, a Commercial grade device (C) of a particular speed grade will have identical guaranteed worst case timing specifications as the Industrial or Military version (I, M, B, or N) of the same part and same speed grade. However, this is not the case for best case or minimum delay timing specifications.

Xilinx devices are assigned a speed grade based on the whether or not the device can pass all the guaranteed worst case timing (maximum delays) for that speed grade. A device that does not pass all AC parametric tests for the fastest speed grade classification may test successfully for a slower speed grade classification and subsequently be assigned that grade. Therefore, a faster device may be categorized to a slower speed grade as long as there aren’t any associated guaranteed minimum timing delay specifications, or the part successfully meets such specifications.

Industrial and Military grade devices are tested at a greater junction temperature range than Commercial grade devices. The commercial range for junction temperature is 0°C to +85°C. The industrial temperature range –40°C to +100°C, and the military range is –55°C to +125°C. The military version of a specific device must meet the same timing specifications at +125°C as the corresponding commercial version at +85°C (for a specific speed grade). For example, a device that meets all timing specifications for a -6 speed grade at +85°C may only meet the timing specifications for a -4 speed grade when tested at +125°C. Therefore, the commercial grade devices will typically have an extended speed grade offering over the availability of devices tested at extended temperature ranges.

Core and IP Support

Cores and IP modules developed for Commercial grade Xilinx devices may also be implemented in Industrial and Military grade as well as Radiation Hardened devices. Device architectures do vary across product grades. However, some cores may have been characterized for speed grades that are unavailable in the extended temperature ranges. Additionally, some cores, such as the Xilinx PCI Core Solution, have been characterized for required minimum timing specifications. In such a case if the Core or IP module has not been specifically characterized for the extended temperature range then it may not be guaranteed to operate over the full temperature range of the device. However, such a core would operate successfully within the temperature range for which it was characterized.

Standard Microcircuit Drawing (SMD) Cross Reference

XC1700 Products (Serial PROMS)

SMD Number	XC1700 Products (Serial PROMS)	Speed	Package	Mark Loc
5962-9471701MPA	XC1765DDD8B		DD8	TOP
5962-9561701MPA	XC17256DDD8B		DD8	TOP
5962-9951401QXA	XQ1701LS020N		SO20	TOP
5962-9951401QYA	XQ1701LCC44B		CC44	TOP

XC3000 Products(1,2)

SMD Number	Equivalent "B" Grade P/N	Speed	Package	Mark Loc
5962-8994803MXC	XC3020-100PG84B	-100	PG84	TOP
5962-8994803MNC	XC3020-100CB100B	-100	CB100	BASE
5962-8994803MMC	XC3020-100CB100B	-100	CB100	LID
5962-8971303MXC	XC3042-100PG84B	-100	PG84	TOP
5962-8971303MZC	XC3042-100PG132B	-100	PG132	TOP
5962-8971303M9C	XC3042-100CB100B	-100	CB100	BASE
5962-8971303MMC	XC3042-100CB100B	-100	CB100	LID
5962-8982303MXC	XC3090-100PG175B	-100	PG175	TOP
5962-8982303MZC	XC3090-100CB164B	-100	CB164	BASE
5962-8982303MTC	XC3090-100CB164B	-100	CB164	LID

Notes:
1. All devices listed also available as military temperature only.
2. **Do not use for new designs.**

XC4000 Products(1,2)

SMD Number	Equivalent "B" Grade P/N	Speed	Package	Mark Loc
5962-9225203MXC	XC4005-5PG156B	-5	PG156	TOP
5962-9225203MYC	XC4005-5CB164B	-5	CB164	LID
5962-9225203MZC	XC4005-5CB164B	-5	CB164	BASE
5962-9230503MXC	XC4010-5PG191B	-5	PG191	TOP
5962-9230503MYC	XC4010-5CB196B	-5	CB196	BASE
5962-9230503MZC	XC4010-5CB196B	-5	CB196	LID
5962-9473002MYC	XC4013-6CB228B[2]	-6	CB228	BASE
5962-9473002MZC	XC4013-6CB228B	-6	CB228	LID
5962-9473002MXC	XC4013-6PG223B	-6	PG223	TOP

Notes:
1. All devices listed also available as military temperature only.
2. **Do not use for new designs.**

XC4000E Products[1,2]

SMD Number	Equivalent "B" Grade P/N	Speed	Package	Mark Loc
5962-9752201QXC	XC4005E-4PG156B	-4	PG156	TOP
5962-9752201QYC	XC4005E-4CB164B	-4	CB164	BASE
5962-9752201QZC	XC4005E-4CB164B	-4	CB164	LID
5962-9752301QXC	XC4010E-4PG191B	-4	PG191	TOP
5962-9752301QYC	XC4010E-4CB164B	-4	CB196	BASE
5962-9752301QZC	XC4010E-4CB164B	-4	CB196	LID
5962-9752401QXC	XC4013E-4PG223B	-4	PG223	TOP
5962-9752401QYC	XC4013E-4CB228B	-4	CB228	BASE
5962-9752401QZC	XC4013E-4CB228B	-4	CB228	LID
5962-9752501QXC	XC4025E-4PG299B	-4	PG299	TOP
5962-9752501QYC	XC4025E-4CB228B	-4	CB228	BASE
5962-9752501QZC	XC4025E-4CB228B	-4	CB228	LID

Notes:
1. All devices listed also available as military temperature only as "XQ" products.
2. XC4010E/XC4013E are also available in plastic as "XQ" products, to -3 speed grade.

XQ4000EX Products[1]

SMD Number	Equivalent "B" Grade P/N	Speed	Package	Mark Loc
5962-985901NTB	XQ4028EX-4HQ240N[2]	-4	HG240	TOP
5962-985901NUA	XQ4028EX-4BG352N[2]	-4	BG352	TOP
5962-985901QXC	XQ4028EX-4PG299B	-4	PG299	TOP
5962-985901QYC	XQ4028EX-4CB228B	-4	CB228	BASE
5962-985901QZC	XQ4028EX-4CB228B	-4	CB228	LID

Notes:
1. All devices listed also available as military temperature only.
2. Plastic package.

XQ4000XL[1]

SMD Number	Equivalent "B" Grade P/N	Speed	Package	Mark Loc
5962-9851301NTB	XQ4013XL-3PQ240N[2]	-3	PG240	TOP
5962-9851301NUA	XQ4013XL-3BG256B[2]	-3	BG256	TOP
5962-9851301QXC	XQ4013XL-3PG223B	-3	PG223	TOP
5962-9851301QYC	XQ4013XL-3CB228B	-3	CB228	BASE
5962-9851301QZC	XQ4013XL-3CB228B	-3	CB288	LID
5962-9851001NTB	XQ4036XL-3HQ240N[2]	-3	HQ240	TOP
5962-9851001NUA	XQ4036XL-3BG352N[2]	-3	BG352	TOP
5962-9851001QXC	XQ4036XL-3PG411B	-3	PG411	TOP
5962-9851001QYC	XQ4036XL-3CB228B	-3	PG228	BASE
5962-9851001QZC	XQ4036XL-3CB228B	-3	CB228	LID
5962-9851101NTB	XQ4062XL-3HQ240N[2]	-3	HQ240	TOP
5962-9851101NUA	XQ4062XL-3BG432N[2]	-3	BG432	TOP
5962-9851101QXC	XQ4062XL-3PG475B	-3	PG475	TOP
5962-9851101QYC	XQ4062XL-3CB228B	-3	CB228	BASE
5962-9851101QZC	XQ4062XL-3CB228B	-3	CB228	LID

Notes:
1. All devices listed also available as military temperature only.
2. Plastic Package

Revision Control

The following table shows the revision history for this document.

Date	Version	Description
01/01/98	1.1	High-Reliability and QML Military Products, correct erroneous information page 2 "XC3000 Products", delete last page, table - "Mil-PRF-3853 QML, Xilinx M Grade and Plastic Commercial Flows"
11/01/98	1.2	Added new products, corrected XC3000, XC4000 products.
02/02/00	2.0	Updated Introduction and product listing.
06/15/00	2.1	Updated product listing and added "Software and Core Support for Xilinx QPRO High-Reliability Products".

QPRO™ QML Certified and Radiation Hardened Products
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QPRO Virtex 2.5V QML High-Reliability FPGAs

DS002 (v1.0) June 1, 2000

Preliminary Product Specification

Features

- Certified to MIL-PRF-38535 (Qualified Manufacturer Listing)
- Guaranteed over the full military temperature range (–55°C to +125°C)
- Ceramic and Plastic Packages
- Fast, high-density Field-Programmable Gate Arrays
  - Densities from 100K to 1M system gates
  - System performance up to 200 MHz
  - Hot-swappable for Compact PCI
- Multi-standard SelectI/O™ interfaces
  - 16 high-performance interface standards
  - Connects directly to ZBTRAM devices
- Built-in clock-management circuitry
  - Four dedicated delay-locked loops (DLLs) for advanced clock control
  - Four primary low-skew global clock distribution nets, plus 24 secondary global nets
- Hierarchical memory system
  - LUTs configurable as 16-bit RAM, 32-bit RAM, 16-bit dual-ported RAM, or 16-bit Shift Register
  - Configurable synchronous dual-ported 4K-bit RAMs
  - Fast interfaces to external high-performance RAMs
- Flexible architecture that balances speed and density
  - Dedicated carry logic for high-speed arithmetic
  - Dedicated multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with clock enable, and dual synchronous/asynchronous set and reset
  - Internal 3-state bussing
  - IEEE 1149.1 boundary-scan logic
  - Die-temperature sensing device
- Supported by FPGA Foundation™ and Alliance Development Systems
  - Complete support for Unified Libraries, Relationally Placed Macros, and Design Manager
  - Wide selection of PC and workstation platforms
- SRAM-based in-system configuration
  - Unlimited reprogrammability
  - Four programming modes
- 0.22 µm 5-layer metal process
- 100% factory tested

Description

The QPRO™ Virtex™ FPGA family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 5-layer-metal 0.22 µm CMOS process. These advances make QPRO Virtex FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex family comprises the four members shown in Table 1.

Building on experience gained from previous generations of FPGAs, the Virtex family represents a revolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the QPRO Virtex family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

Refer to the "Virtex™ 2.5V Field Programmable Gate Arrays" commercial data sheet for more information on device architecture and timing specifications.

Table 1: **QPRO Virtex Field-Programmable Gate Array Family Members**

Device	System Gates	CLB Array	Logic Cells	Maximum Available I/O	Block RAM Bits	Max Select RAM Bits
XQV100	108,904	20 x 30	2,700	180	40,960	38,400
XQV300	322,970	32 x 48	6,912	316	65,536	98,304
XQV600	661,111	48 x 72	15,552	316	98,304	221,184
XQV1000	1,124,022	64 x 96	27,648	404	131,072	393,216

Virtex Electrical Characteristics

Virtex DC Characteristics

Absolute Maximum Ratings

Symbol	Description		Min/Max	Units
V_{CCINT}	Supply voltage relative to GND		–0.5 to 3.0	V
V_{CCO}	Supply voltage relative to GND		–0.5 to 4.0	V
V_{REF}	Input reference Voltage		–0.5 to 3.6	V
V_{IN}	Input voltage relative to GND	Using V_{REF}	–0.5 to 3.6	V
		Internal threshold	–0.5 to 5.5	V
V_{TS}	Voltage applied to 3-state output		–0.5 to 5.5	V
V_{CC}	Longest supply voltage rise time from 1V to 2.375V		50	ms
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_{SOL}	Maximum soldering temp. (10s at 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. Power supplies may turn on in any order.
3. For protracted periods (e.g., longer than a day), V_{IN} should not exceed V_{CCO} by more that 3.6V.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CCINT}	Supply voltage relative to GND, T_C = –55°C to +125°C	Ceramic packages	2.5 – 5%	2.5 + 5%	V
	Supply voltage relative to GND, T_J = –55°C to +125°C	Plastic packages	2.5 – 5%	2.5 + 5%	V
V_{CCO}	Supply voltage relative to GND, T_C = –55°C to +125°C	Ceramic packages	1.2	3.6	V
	Supply voltage relative to GND, T_J = –55°C to +125°C	Plastic packages	1.2	3.6	V
T_{IN}	Input signal transition time		-	250	ns

Notes:
1. Correct operation is guaranteed with a minimum V_{CCINT} of 2.25V (Nominal V_{CCINT} – 10%). Below the minimum value stated above, all delay parameters increase by 3% for each 50 mV reduction in V_{CCINT} below the specified range.
2. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
3. Input and output measurement threshold is ~50% of V_{CC}.

DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Device	Min	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data may be lost)	All	2.0	-	V
V_{DRIO}	Data retention V_{CCO} voltage (below which configuration data may be lost)	All	1.2	-	V
I_{CCINTQ}	Quiescent V_{CCINT} supply current(1)	XQV100	-	50	mA
		XQV300	-	75	mA
		XQV600	-	100	mA
		XQV1000	-	100	mA
I_{CCOQ}	Quiescent V_{CCINT} supply current(1)	XQV100	-	2	mA
		XQV300	-	2	mA
		XQV600	-	2	mA
		XQV1000	-	2	mA
I_{REF}	V_{REF} current per V_{REF} pin	-	-	20	µA
I_L	Input or output leakage current	-	–10	+10	µA
C_{IN}	Input capacitance (sample tested)	-	-	8	pF
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 3.3V (sample tested)	-	(2)	0.25	mA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 3.6V (sample tested)	-	(2)	0.15	mA

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins in a High-Z state and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed output currents over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTL(1)	–0.5	0.8	2.0	5.5	0.4	2.4	24	–24
LVCMOS2	–0.5	0.7	1.7	5.5	0.4	1.9	12	–12
PCI, 3.3 V	–0.5	44% V_{CCINT}	60% V_{CCINT}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	(2)	(2)
PCI, 5.0 V	–0.5	0.8	2.0	5.5	0.55	2.4	(2)	(2)
GTL	–0.5	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	n/a	40	n/a
GTL+	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	n/a	36	n/a
HSTL I	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	8	-8
HSTL III	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	24	–8
HSTL IV	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	48	–8
SSTL3 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	–8
SSTL3 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	–16
SSTL2 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.65	V_{REF} + 0.65	7.6	–7.6
SSTL2 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.80	V_{REF} + 0.80	15.2	–15.2
CTT	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.4	V_{REF} + 0.4	8	–8
AGP	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	(2)	(2)

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested.
2. Tested according to the relevant specifications.

Virtex Switching Characteristics

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Virtex devices unless otherwise noted.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 6.

Symbol	Description	Device	Speed Grade	Units
			-4	
Propagation Delays				
T_{IOPI}	Pad to I output, no delay	All	1.0	ns, max
T_{IOPID}	Pad to I output, with delay	XQV100	1.9	ns, max
		XQV300	1.9	ns, max
		XQV600	2.3	ns, max
		XQV1000	2.7	ns, max
T_{IOPLI}	Pad to output IQ via transparent latch, no delay	All	2.0	ns, max
T_{IOPLID}	Pad to output IQ via transparent latch, with delay	XQV100	4.8	ns, max
		XQV300	5.1	ns, max
		XQV600	5.5	ns, max
		XQV1000	5.9	ns, max
Sequential Delays				
T_{IOCKIQ}	Clock CLK to output IQ	All	0.8	ns, max
Setup and Hold Times with Respect to Clock CLK		**Setup Time / Hold Time**		
T_{IOPICK} / T_{IOICKP}	Pad, no delay	All	2.0 / 0	ns, min
$T_{IOPICKD}$ / $T_{IOICKPD}$	Pad, with delay	All	5.0 / 0	ns, min
$T_{IOICECK}$ / $T_{IOCKICE}$	ICE input	All	1.0 / 0	ns, min
$T_{IOSRCKI}$ / $T_{IOCKISR}$	SR input (IFF, synchronous)	All	1.3 / 0	ns, min
Set/Reset Delays				
T_{IOSRIQ}	SR input to IQ (asynchronous)	All	1.8	ns, max
T_{GSRQ}	GSR to output IQ	All	12.5	ns, max

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

IOB Input Switching Characteristics Standard Adjustments

Symbol	Description	Standard	Speed Grade	Units
			-4	
Data Input Delay Adjustments				
T_{ILVTTL}	Standard-specific data input delay adjustments	LVTTL	0.0	ns
$T_{ILVCMOS2}$		LVCMOS2	–0.05	ns
T_{IPCI33_3}		PCI, 33 MHz, 3.3V	–0.14	ns
T_{IPCI33_5}		PCI, 33 MHz, 5.0V	0.33	ns
T_{IGTL}		GTL	0.26	ns
T_{IGTLP}		GTL+	0.14	ns
T_{IHSTL}		HSTL	0.04	ns
T_{ISSTL2}		SSTL2	–0.10	ns
T_{ISSTL3}		SSTL3	–0.06	ns
T_{ICTT}		CTT	0.02	ns
T_{IAGP}		AGP	–0.08	ns

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" on page 8.

Symbol	Description	Speed Grade -4	Units
Propagation Delays			
T_{IOOP}	O input to pad	3.5	ns, max
T_{IOOLP}	O input to pad via transparent latch	4.0	ns, max
3-State Delays			
T_{IOTHZ}	T input to pad high-impedance(1)	2.4	ns, max
T_{IOTON}	T input to valid data on pad	3.7	ns, max
$T_{IOTLPHZ}$	T input to pad high-impedance via transparent latch(1)	3.0	ns, max
$T_{IOTLPON}$	T input to valid data on pad via transparent latch	4.2	ns, max
T_{GTS}	GTS to pad high impedance(1)	6.3	ns, max
Sequential Delays			
T_{IOCKP}	Clock CLK to pad	3.5	ns, max
T_{IOCKHZ}	Clock CLK to pad high-impedance (synchronous)(1)	2.9	ns, max
T_{IOCKON}	Clock CLK to valid data on pad (synchronous)	4.1	ns, max
Setup and Hold Times before/after Clock CLK		**Setup Time / Hold Time(2)**	
T_{IOOCK}/T_{IOCKO}	O input	1.3 / 0	ns, min
$T_{IOOCECK}/T_{IOCKOCE}$	OCE input	1.0 / 0	ns, min
$T_{IOSRCKO}/T_{IOCKOSR}$	SR input (OFF)	1.4 / 0	ns, min
T_{IOTCK}/T_{IOCKT}	3-state setup times, T input	0.9 / 0	ns, min
$T_{IOTCECK}/T_{IOCKTCE}$	3-state setup times, TCE input	1.1 / 0	ns, min
$T_{IOSRCKT}/T_{IOCKTSR}$	3-state setup times, SR input (TFF)	1.3 / 0	ns, min
Set/Reset Delays			
T_{IOSRP}	SR input to pad (asynchronous)	4.6	ns, max
T_{IOSRHZ}	SR input to pad high-impedance (asynchronous)(1)	3.9	ns, max
T_{IOSRON}	SR input to valid data on pad (asynchronous)	5.1	ns, max

Notes:

1. High-impedance turn-off delays should not be adjusted.
2. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Symbol	Description	Standard		Speed Grade -4	Units
Output Delay Adjustments					
T_{OLVTTL_S2}	Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, C_{sl})	LVTTL, slow	2 mA	17.0	ns
T_{OLVTTL_S4}			4 mA	8.6	ns
T_{OLVTTL_S6}			6 mA	5.6	ns
T_{OLVTTL_S8}			8 mA	3.5	ns
T_{OLVTTL_S12}			12 mA	2.2	ns
T_{OLVTTL_S16}			16 mA	2.0	ns
T_{OLVTTL_S24}			24 mA	1.6	ns
T_{OLVTTL_F2}		LVTTL, fast	2 mA	15.1	ns
T_{OLVTTL_F4}			4 mA	6.1	ns
T_{OLVTTL_F6}			6 mA	3.6	ns
T_{OLVTTL_F8}			8 mA	1.2	ns
T_{OLVTTL_F12}			12 mA	0.0	ns
T_{OLVTTL_F16}			16 mA	–0.05	ns
T_{OLVTTL_F24}			24 mA	–0.23	ns
$T_{OLVCMOS2}$		LVCMOS2		0.12	ns
T_{OPCI33_3}		PCI, 33 MHz, 3.3V		2.7	ns
T_{OPCI33_5}		PCI, 33 MHz, 5.0V		3.3	ns
T_{OGTL}		GTL		0.6	ns
T_{OGTLP}		GTL+		1.0	ns
T_{OHSTL_I}		HSTL I		–0.5	ns
T_{OHSTL_III}		HSTL III		–1.0	ns
T_{OHSTL_IV}		HSTL IV		–1.1	ns
T_{OSSTL2_I}		SSTL2 I		–0.5	ns
T_{OSSTL2_II}		SSTL2 II		–1.0	ns
T_{OSSTL3_I}		SSTL3 I		–0.5	ns
T_{OSSTL3_II}		SSTL3 II		–1.1	ns
T_{OCTT}		CTT		–0.6	ns
T_{OAGP}		AGP		–1.0	ns

Calculation of T_{ioop} as a Function of Capacitance

The values for T_{ioop} were based on the standard capacitive load (Csl) for each I/O standard as listed in Table 2.

For other capacitive loads, use the formulas below to calculate the corresponding T_{ioop}:

$$T_{ioop} = T_{ioopl} + T_{opadjust} + (C_{load} - C_{sl}) * fl$$

Where:

$T_{opadjust}$ is reported above in the Output Delay Adjustment section.

C_{load} is the capacitive load for the design.

Table 2: **Constants for Use in Calculation of T_{op}**

Standard		C_{sl} (pF)	fl (ns/pF)
LVTTL slow slew rate	2 mA drive	35	0.41
	4 mA drive	35	0.20
	6 mA drive	35	0.100
	8 mA drive	35	0.086
	12 mA drive	35	0.058
	16mA drive	35	0.050
	24 mA drive	35	0.048
LVTTL fast slew rate	2 mA drive	35	0.41
	4 mA drive	35	0.20
	6 mA drive	35	0.13
	8 mA drive	35	0.079
	12 mA drive	35	0.044
	16mA drive	35	0.043
	24 mA drive	35	0.033

Table 2: **Constants for Use in Calculation of T_{op}** ***(Continued)***

Standard	C_{sl} (pF)	fl (ns/pF)
LVCMOS2	35	0.041
PCI 33 MHz 5V	50	0.050
PCI 33 MHZ 3.3V	10	0.050
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class 1	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

Clock Distribution Guidelines

Symbol	Description	Device	Speed Grade -4	Units
Global Clock Skew				
$T_{GSKEWIOB}$	Global clock skew between IOB flip-flops	XQV100	0.15	ns, max
		XQV300	0.18	ns, max
		XQV600	0.17	ns, max
		XQV1000	0.25	ns, max

Notes:

1. These clock-distribution delays are provided for guidance only. They reflect the delays encountered in a typical design under worst-case conditions. Precise values for a particular design are provided by the timing analyzer.

Clock Distribution Switching Characteristics

Symbol	Description	Speed Grade -4	Units
GCLK IOB and Buffer			
T_{GPIO}	Global clock pAD to output	0.9	ns, max

Symbol	Description	Speed Grade	Units
		-4	
T_{GIO}	Global clock buffer I input to O output	0.9	ns, max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Symbol	Description	Speed Grade	Units
		-4	
Combinatorial Delays			
T_{ILO}	4-input function: F/G inputs to X/Y outputs	0.8	ns, max
T_{IF5}	5-input function: F/G inputs to F5 output	0.9	ns, max
T_{IF5X}	5-input function: F/G inputs to X output	1.0	ns, max
T_{IF6Y}	6-input function: F/G inputs to Y output via F6 MUX	1.2	ns, max
T_{F5INY}	6-input function: F5IN input to Y output	0.5	ns, max
T_{IFNCTL}	Incremental delay routing through transparent latch to XQ/YQ outputs	0.8	ns, max
T_{BYYB}	BY input to YB output	0.7	ns, max
Sequential Delays			
T_{CKO}	FF clock CLK to XQ/YQ outputs	1.4	ns, max
T_{CKLO}	Latch clock CLK to XQ/YQ outputs	1.6	ns, max
Setup and Hold Times before/after Clock CLK		**Setup Time / Hold Time**	
T_{ICK}/T_{CKI}	4-input function: F/G Inputs	1.5 / 0	ns, min
T_{IF5CK}/T_{CKIF5}	5-input function: F/G inputs	1.7 / 0	ns, min
T_{F5INCK}/T_{CKF5IN}	6-input function: F5IN input	1.2 / 0	ns, min
T_{IF6CK}/T_{CKIF6}	6-input function: F/G inputs via F6 MUX	1.9 / 0	ns, min
T_{DICK}/T_{CKDI}	BX/BY inputs	0.8 / 0	ns, min
T_{CECK}/T_{CKCE}	CE input	1.0 / 0	ns, min
$T_{RCK}T_{CKR}$	SR/BY inputs (synchronous)	0.9 / 0	ns, min
Clock CLK			
T_{CH}	Minimum pulse width, High	2.0	ns, min
T_{CL}	Minimum pulse width, Low	2.0	ns, min
Set/Reset			
T_{RPW}	Minimum pulse width, SR/BY inputs	3.3	ns, min
T_{RQ}	Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	1.4	ns, max
T_{IOGSRQ}	Delay from GSR to XQ/YQ outputs	12.5	ns, max

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

Symbol	Description	Speed Grade	Units
		-4	
Combinatorial Delays			
T_{OPX}	F operand inputs to X via XOR	1.0	ns, max
T_{OPXB}	F operand input to XB output	1.4	ns, max
T_{OPY}	F operand input to Y via XOR	2.0	ns, max
T_{OPYB}	F operand input to YB output	2.0	ns, max
T_{OPCYF}	F operand input to COUT output	1.5	ns, max
T_{OPGY}	G operand inputs to Y via XOR	1.2	ns, max
T_{OPGYB}	G operand input to YB output	2.1	ns, max
T_{OPCYG}	G operand input to COUT output	1.6	ns, max
T_{BXCY}	BX initialization input to COUT	1.1	ns, max
T_{CINX}	CIN input to X output via XOR	0.6	ns, max
T_{CINXB}	CIN input to XB	0.1	ns, max
T_{CINY}	CIN input to Y via XOR	0.6	ns, max
T_{CINYB}	CIN input to YB	0.6	ns, max
T_{BYP}	CIN input to COUT output	0.2	ns, max
Multiplier Operation			
T_{FANDXB}	F1/2 operand inputs to XB output via AND	0.5	ns, max
T_{FANDYB}	F1/2 operand inputs to YB output via AND	1.1	ns, max
T_{FANDCY}	F1/2 operand inputs to COUT output via AND	0.6	ns, max
T_{GANDYB}	G1/2 operand inputs to YB output via AND	0.7	ns, max
T_{GANDCY}	G1/2 operand inputs to COUT output via AND	0.2	ns, max
Setup and Hold Times before/after Clock CLK		**Setup Time / Hold Time**	
T_{CCKX}/T_{CKCX}	CIN input to FFX	1.3 / 0	ns, min
T_{CCKY}/T_{CKCY}	CIN input to FFY	1.4 / 0	ns, min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

CLB SelectRAM Switching Characteristics

Symbol	Description	Speed Grade -4	Units
Sequential Delays			
T_{SHCKO}	Clock CLK to X/Y outputs (WE active)	3.0	ns, max
Shift-Register Mode			
T_{SHCKO}	Clock CLK to X/Y outputs	3.0	ns, max
Setup Times before Clock CLK		**Setup Time / Hold Time**	
T_{AS}/T_{AH}	F/G address inputs	0.7 / 0	ns, min
T_{DS}/T_{DH}	BX/BY data inputs (DIN)	0.9 / 0	ns, min
T_{WS}/T_{WH}	CE input (WE)	1.0 / 0	ns, min
Shift-Register Mode			
T_{SHDICK}	BX/BY data inputs (DIN)	0.9	ns, min
T_{SHCECK}	CE input (WS)	1.0	ns, min
Clock CLK			
T_{WPH}	Minimum pulse width, High	3.1	ns, min
T_{WPL}	Minimum pulse width, Low	3.1	ns, min
T_{WC}	Minimum clock period to meet address write cycle time	6.2	ns, min
Shift-Register Mode			
T_{SRPH}	Minimum pulse width, High	3.1	ns, min
T_{SRPL}	Minimum pulse width, Low	3.1	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

BLOCKRAM Switching Characteristics

Symbol	Description	Speed Grade -4	Units
Sequential Delays			
T_{BCKO}	Clock CLK to DOUT output	4.1	ns, max
Setup Times Before Clock Clk			
T_{BACK}/T_{BCKA}	ADDR inputs	1.5 / 0	ns, min
T_{BDCK}/T_{BCKD}	DIN inputs	1.5 / 0	
T_{BECK}/T_{BCKE}	EN input	3.4 / 0	ns, min
T_{BRCK}/T_{BCKR}	RST input	3.2 / 0	ns, min
T_{BWCK}/T_{BCKW}	WEN input	3.0 / 0	ns, min
Clock CLK			
T_{BPWH}	Minimum pulse width, High	2.0	ns, min
T_{BPWL}	Minimum pulse width, Low	2.0	ns, min
T_{BCCS}	CLKA -> CLKB setup time for different ports	4.0	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

TBUF Switching Characteristics

Symbol	Description	Speed Grade	Units
		-4	
Combinatorial Delays			
T_{IO}	IN input to OUT output	0.0	ns, max
T_{OFF}	TRI input to OUT output high-impedance	0.2	ns, max
T_{ON}	Tri input to valid data on OUT output	0.2	ns, max

JTAG Test Access Port Switching Characteristics

Symbol	Description	Speed Grade	Units
		-4	
T_{TAPTCK}	TMS and TDI setup times before TCK	4.0	ns, min
T_{TCKTAP}	TMS and TDI hold times after TCK	2.0	ns, min
T_{TCKTDO}	Output delay from clock TCK to output TDO	11.0	ns, max
F_{TCK}	Maximum TCK clock frequency	33	MHz, max

Virtex Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL

Symbol	Description	Device	Speed Grade	Units
			-4	
	LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DLL. For data *output* with different standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" on page 8.	XQV100	3.6	ns, max
		XQV300	3.6	ns, max
		XQV600	3.6	ns, max
		XQV1000	3.6	ns, max

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For different loads, see Table 2.
3. DLL output jitter is already included in the timing calculation.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DLL

Symbol	Description	Device	Speed Grade	Units
			-4	
	LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *without* DLL. For data *output* with different standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" on page 8.	XQV100	5.7	ns, max
		XQV300	5.9	ns, max
		XQV600	6.0	ns, max
		XQV1000	6.3	ns, max

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column,and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For different loads, see Table 2.

Minimum Clock to Out for Virtex Devices

I/O Standard	With DLL	Without DLL				
	All Devices	V100	V300	V600	V1000	Units
LVTTL_S2(1)	5.2	6.0	6.1	6.1	6.1	ns
LVTTL_S4(1)	3.5	4.3	4.4	4.4	4.4	ns
LVTTL_S6(1)	2.8	3.6	3.7	3.7	3.7	ns
LVTTL_S8(1)	2.2	3.1	3.1	3.2	3.2	ns
LVTTL_S12(1)	2.0	2.9	2.9	3.0	3.0	ns
LVTTL_S16(1)	1.9	2.8	2.8	2.9	2.9	ns
LVTTL_S24(1)	1.8	2.6	2.7	2.7	2.8	ns
LVTTL_F2(1)	2.9	3.8	3.8	3.9	3.9	ns
LVTTL_F4(1)	1.7	2.6	2.6	2.7	2.7	ns
LVTTL_F6(1)	1.2	2.0	2.1	2.1	2.2	ns
LVTTL_F8(1)	1.1	1.9	2.0	2.0	2.0	ns
LVTTL_F12(1)	1.0	1.8	1.9	1.9	1.9	ns
LVTTL_F16(1)	0.9	1.8	1.8	1.8	1.9	ns
LVTTL_F24(1)	0.9	1.7	1.8	1.8	1.9	ns
LVCMOS2	1.1	1.9	2.0	2.0	2.1	ns
PCI33_3	1.5	2.4	2.4	2.5	2.5	ns
PCI33_5	1.4	2.2	2.3	2.3	2.4	ns
GTL	1.6	2.5	2.5	2.6	2.6	ns
GTL+	1.7	2.5	2.6	2.6	2.7	ns
HSTL I	1.1	1.9	2.0	2.0	2.0	ns
HSTL III	0.9	1.7	1.8	1.8	1.9	ns
HSTL IV	0.8	1.6	1.7	1.7	1.8	ns
SSTL2 I	0.9	1.7	1.8	1.8	1.8	ns
SSTL2 II	0.8	1.6	1.7	1.7	1.7	ns
SSTL3 I	0.8	1.7	1.7	1.7	1.8	ns
SSTL3 II	0.7	1.5	1.6	1.6	1.7	ns
CTT	1.0	1.8	1.9	1.9	2.0	ns
AGP	1.0	1.8	1.9	1.9	2.0	ns

Notes:
1. S = Slow Slew Rate, F = Fast Slew Rate
2. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column. and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
3. Output timing is measured at 50% V_{CC} threshold with 8 pF external capacitive load.

Virtex Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

Global Clock Setup and Hold for LVTTL Standard, *with* DLL

Symbol	Description	Device	Speed Grade	Units
			-4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in Input Delay Adjustments.				
T_{PSDLL}/T_{PHDLL}	**No Delay** Global clock and IFF, with DLL	XQV100	2.1 / –0.4	ns, min
		XQV300	2.1 / –0.4	ns, min
		XQV600	2.1 / –0.4	ns, min
		XQV1000	2.1 / –0.4	ns, min

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DLL output jitter is already included in the timing calculation.

Global Clock Setup and Hold for LVTTL Standard, *without* DLL

Symbol	Description	Device	Speed Grade	Units
			-4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in Input Delay Adjustments.				
T_{PSFD}/T_{PHFD}	**Full Delay** Global clock and IFF, without DLL	XQV100	3.0 / 0.0	ns, min
		XQV300	3.1 / 0.0	ns, min
		XQV600	3.3 / 0.0	ns, min
		XQV1000	3.6 / 0.0	ns, min

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

DLL Timing Parameters

Switching parameters testing is modeled after testing methods specified by MIL-M-38510/605; all devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

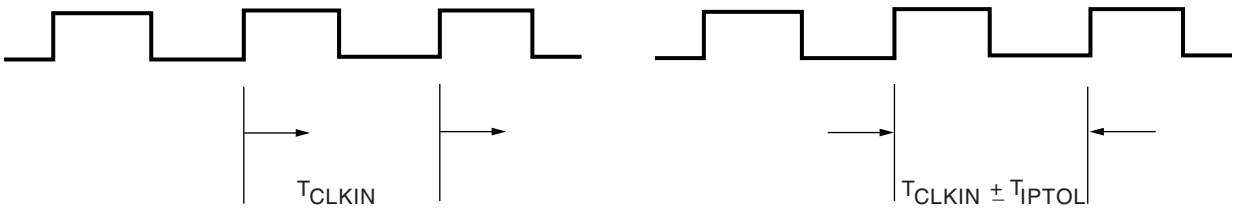
Symbol	Description	Speed Grade -4		Units
		Min	Max	
$F_{CLKINHF}$	Input clock frequency (CLKDLLHF)	60	180	MHz
$F_{CLKINLF}$	Inputclock frequency (CLKDLL)	25	90	MHz
$T_{DLLPWHF}$	Input clock pulse width (CLKDLLHF)	2.4	-	ns
$T_{DLLPWLF}$	Input clock pulse width (CLKDLL)	3.0	-	ns

Notes:
1. All specifications correspond to Commercial Operating Temperatures (0°C to +100°C).

Symbol	Description		CLKDLLHF		CLKDLL		Units
			Min	Max	Min	Max	
T_{IPTOL}	Input clock period tolerance		-	1.0	-	1.0	ns
T_{IJITCC}	Input clock jitter cycle to cycle		-	±150	-	±300	ps
T_{LOCK}	Time required for DLL to acquire Lock						
	F_{CLKIN}	> 60 MHz	-	20	-	20	µs
		50-60 MHz	-	-	-	25	µs
		40-50 MHz	-	-	-	50	µs
		30-40 MHz	-	-	-	90	µs
		25-30 MHz	-	-	-	120	µs
T_{SKEW}	DLL output skew (between any DLL output)		-	±150	-	±150	ps
T_{OPHASE}	DLL output long term phase differential		-	±100	-	±100	ps
T_{OJITCC}	DLL output ditter cycle to cycle			±60		±60	ps

Notes:
1. All specifications correspond to Commercial Operating Temperatures (0°C to +100°C).

Period Tolerance: the allowed input clock period change in nanoseconds.



Clock Jitter: the difference between an ideal reference clock edgfe and the actual design.

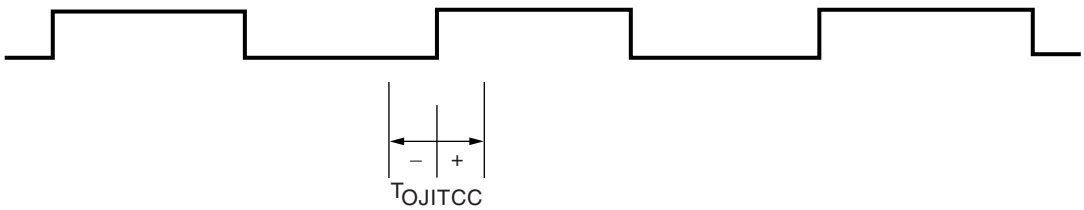


Figure 1: **Frequency Tolerance and Clock Jitter**

QPRO Virtex Pinouts

Pinout Tables

See the Xilinx WebLINX web site (http://www.xilinx.com/partinfo/databook.htm) for updates or additional pinout information. For convenience, Table 3, Table 4 and Table 5 list the locations of special-purpose and power-supply pins. Pins not listed are user I/Os.

Table 3: **Virtex QFP Package Pinout Information**

Pin Name	Device	PQ/HQ240
GCK0	All	92
GCK1	All	89
GCK2	All	210
GCK3	All	213
M0	All	60
M1	All	58
M2	All	62
CCLK	All	179
PROGRAM	All	122
DONE	All	120
INIT	All	123
BUSY/DOUT	All	178
D0/DIN	All	177
D1	All	167
D2	All	163
D3	All	156
D4	All	145
D5	All	138
D6	All	134
D7	All	124
WRITE	All	185
CS	All	184
TDI	All	183
TDO	All	181
TMS	All	2
TCK	All	239
V_{CCINT}	All	16, 32, 43, 77, 88, 104, 137, 148, 164, 198, 214, 225
V_{CCO}	All	No I/O Banks in this package: 15, 30, 44, 61, 76, 90, 105, 121, 136, 150, 165, 180, 197, 212, 226, 240

Table 3: **Virtex QFP Package Pinout Information *(Continued)***

Pin Name	Device	PQ/HQ240
V_{REF}, Bank 0 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQV100	... + 229
	XQV300	... + 236
	XQV600	... + 230
V_{REF}, Bank 1 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQV100	... + 194
	XQV300	... + 187
	XQV600	... + 193
V_{REF}, Bank 2 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQV100	... + 168
	XQV300	... + 175
	XQV600	... + 169
V_{REF}, Bank 3 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQV100	... + 133
	XQV300	... + 126
	XQV600	... + 132
V_{REF}, Bank 4 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQV100	... + 108
	XQV300	... + 115
	XQV600	... + 109
V_{REF}, Bank 5 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQV100	... + 73
	XQV300	... + 66
	XQV600	... + 72
V_{REF}, Bank 6 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQV100	... + 47
	XQV300	... + 54
	XQV600	... + 48

Table 3: **Virtex QFP Package Pinout Information *(Continued)***

Pin Name	Device	PQ/HQ240
V_{REF}, Bank 7 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQV100	... + 12
	XQV300	... + 5
	XQV600	... + 11
GND	All	1, 8, 14, 22, 29, 37, 45, 51, 59, 69, 75, 83, 91, 98, 106, 112, 119, 129, 135, 143, 151, 158, 166, 172, 182, 190, 196, 204, 211, 219, 227, 233

Table 4: **Virtex Plastic Ball Grid and Ceramic Column Grid Pinout Information**

Pin Name	Device	BG256	BG352	BG432	BG560/CG560
GCK0	All	Y11	AE13	AL16	AL17
GCK1	All	Y10	AF14	AK16	AJ17
GCK2	All	A10	B14	A16	D17
GCK3	All	B10	D14	D17	A17
M0	All	Y1	AD24	AH28	AJ29
M1	All	U3	AB23	AH29	AK30
M2	All	W2	AC23	AJ28	AN32
CCLK	All	B19	C3	D4	C4
PROGRAM	All	Y20	AC4	AH3	AM1
DONE	All	W19	AD3	AH4	AJ5
INIT	All	U18	AD2	AJ2	AH5
BUSY/DOUT	All	D18	E4	D3	D4
D0/DIN	All	C19	D3	C2	E4
D1	All	E20	G1	K4	K3
D2	All	G19	J3	K2	L4
D3	All	J19	M3	P4	P3
D4	All	M19	R3	V4	W4
D5	All	P19	U4	AB1	AB5
D6	All	T20	V3	AB3	AC4
D7	All	V19	AC3	AG4	AJ4
WRITE	All	A19	D5	B4	D6
CS	All	B18	C4	D5	A2
TDI	All	C17	B3	B3	D5
TDO	All	A20	D4	C4	E6
TMS	All	D3	D23	D29	B33
TCK	All	A1	C24	D28	E29
DXN	All	W3	AD23	AH27	AK29

Table 4: **Virtex Plastic Ball Grid and Ceramic Column Grid Pinout Information *(Continued)***

Pin Name	Device	BG256	BG352	BG432	BG560/CG560
DXP	All	V4	AE24	AK29	AJ28
V_{CCINT} (V_{CCINT} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XQV100	C10, D6, D15, F4, F17, L3, L18, R4, R17, U6, U15, V10			
	XQV300		A20, B16, C14, D10, D12, J24, K4, L1, L25, P2, P25, R23, T1, V24, W2, AC10, AE14, AE19, AF11, AF16,	A10, A17, B23, C14, C19, K3, K29, N2, N29, T1, T29, W2, W31, AB2, AB30, AJ10, AJ16, AK13, AK19, AK22	
	XQV600			... + B26, C7, F1, F30, AE29, AF1, AH8, AH24	
	XQV1000				A21, B12, B14, B18, B28, C22, C24, E9, E12, F2, H30, J1, K32, M3, N1, N29, N33, U5, U30, Y2, Y31, AB2, AB32, AD2, AD32, AG3, AG31, AJ13, AK8, AK11, AK17, AK20, AL14, AL22, AL27, AN25
V_{CCO}, Bank 0	All	D7, D8	A17, B25, D19	A21, C29, D21	A22, A26, A30, B19, B32
V_{CCO}, Bank 1	All	D13, D14	A10, D7, D13	A1, A11, D11	A10, A16, B13, C3, E5
V_{CCO}, Bank 2	All	G17, H17	B2, H4, K1	C3, L1, L4	B2, D1, H1, M1, R2
V_{CCO}, Bank 3	All	N17, P17	P4, U1, Y4	AA1, AA4, AJ3	V1, AA2, AD1, AK1, AL2
V_{CCO}, Bank 4	All	U13, U14	AC8, AE2, AF10	AH11, AL1, AL11	AM2, AM15, AN4, AN8, AN12
V_{CCO}, Bank 5	All	U7, U8	AC14, AC20, AF17	AH21, AJ29, AL21	AL31, AM21, AN18, AN24, AN30
V_{CCO}, Bank 6	All	N4, P4	U26, W23, AE25	AA28, AA31, AL31	W32, AB33, AF33, AK33, AM32
V_{CCO}, Bank 7	All	G4, H4	G23, K26, N23	A31, L28, L31	C32, D33, K33, N32, T33

Table 4: **Virtex Plastic Ball Grid and Ceramic Column Grid Pinout Information *(Continued)***

Pin Name	Device	BG256	BG352	BG432	BG560/CG560
V_{REF}, Bank 0 (VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQV100	A4, A8, B4			
	XQV300		A16, C19, C21, D21	B19, D22, D24, D26	
	XQV600			... + C18, C24	
	XQV1000				A19, D20, D26, D29, E21, E23, E24, E27,
V_{REF}, Bank 1 (VREF pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQV100	A17, B12, B15			
	XQV300		B6, C9, C12, D6	A13, B7, C6, C10	
	XQV600			... + B15, D10	
	XQV1000				A6, D7, D10, D11, D13, D16, E7, E15
V_{REF}, Bank 2 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQV100	C20, F19, J18			
	XQV300		D2, E2, H2, M4	E2, G3, J2, N1	
	XQV600			... + H1, R3	
	XQV1000				B3, G5, H4, K5, L5, N5, P4, R1
V_{REF}, Bank 3 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQV100	M18, R19, V20			
	XQV300		R4, V4, Y3, AC2	V2, AB4, AD4, AF3	
	XQV600			... + U2, AC3	
	XQV1000				V4, W5, AA4, AD3, AE5, AF1, AH4, AK2

Table 4: **Virtex Plastic Ball Grid and Ceramic Column Grid Pinout Information *(Continued)***

Pin Name	Device	BG256	BG352	BG432	BG560/CG560
V_{REF}, Bank 4 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQV100	V12, W15, Y18			
	XQV300		AC12, AE4, AE5, AE8	AJ7, AL4, AL8, AL13	
	XQV600			... + AK8, AK15	
	XQV1000				AK13, AL7, AL9, AL10, AL16, AM4, AM14,AN3
V_{REF}, Bank 5 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQV100	V9, W6, Y3			
	XQV300		AC15, AC18, AD20, AE23	AJ18, AJ25, AK23, AK27	
	XQV600			... + AJ17, AL24	
	XQV1000				AJ18, AJ25, AK28, AL20, AL24, AL29, AM26, AN23
V_{REF}, Bank 6 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQV100	M2, R3, T1			
	XQV300		R24, Y26, AA25, AD26	V28, AB28, AE30, AF28	
	XQV600			... + U28, AC28	
	XQV1000				V29, Y32, AA30,AD31, AE29, AK32, AE31, AH30
V_{REF}, Bank 7 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQV100	D1, G3, H1			
	XQV300		D26, E24, G26, L26	F28, F31, J30, N30	
	XQV600			... + J28, R31	
	XQV1000				D31, E31, G31, H32, K31, P31, T31

Table 4: **Virtex Plastic Ball Grid and Ceramic Column Grid Pinout Information *(Continued)***

Pin Name	Device	BG256	BG352	BG432	BG560/CG560
GND	All	C3, C18, D4, D5, D9, D10, D11, D12, D16, D17. E4, E17, J4, J17, K4, K17, L4, L17, M4, M9, M10, M17, T4, T17, U4, U5, U9, U10, U11, U12, U16, U17, V3, V18	A1, A2, A5, A8, A14, A19, A22, A25, A26, B1, B26, E1, E26, H1, H26, N1, P26, W1, W26, AB1, AB26, AE1, AE26, AF1, AF2, AF5, AF8, AF13, AF19, AF22, AF25, AF26	A2, A3, A7, A9, A14, A18, A23, A25, A29, A30, B1, B2, B30, B31, C1, C31, D16, G1, G31, J1, J31, P1, P31, T4, T28, V1, V31, AC1, AC31, AE1, AE31, AH16, AJ1, AJ31, AK1, AK2, AK30, AK31, AL2, AL3, AL7, AL9, AL14, AL18, AL23, AL25, AL29, AL30	A1, A7, A12, A14, A18, A20, A24, A29, A32, A33, B1, B6, B9, B15, B23, B27, B31, C2, E1, F32, G2, G33, J32, K1, L2, M33, P1, P33, R32, T1, V33, W2, Y1, Y33, AB1, AC32, AD33, AE2, AG1, AG32, AH2, AJ33, AL32, AM3, AM7, AM11, AM19, AM25, AM28, AM33, AN1, AN2, AN5, AN10, AN14, AN16, AN20, AN22, AN27, AN33
GND(1)	All	J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11,M12			
No Connect					C31, AC2, AK4, AL3

Notes:
1. 16 extra balls (grounded) at package center.

Ceramic Quad Flat Package (CB228) Pinout Information

Table 5: **CQFP Package (CB228)**

Function	Pin No.
GND	1
TMS	2
IO	3
IO	4
IO_VREF_7	5
IO	6
IO	7
GND	8
OIIO	9
IO	10
IO	11
IO_VREF_7	12
IO	13
GND	14
VCCINT	15
IO	16
IO	17
VCCO	18
IO	19
IO	20
IO_VREF_7	21
IO	22
IO	23
IO	24
IO	25
IO_IRDY	26
GND	27
VCCO	28
IO_TRDY	29
VCCINT	30
IO	31
IO	32
IO	33
IO_VREF_6	34
IO	35
IO	36
VCCO	37
IO	38

Table 5: **CQFP Package (CB228)** ***(Continued)***

Function	Pin No.
OP	39
IO	40
VCCINT	41
GND	42
IO	43
IO_VREF_6	44
IO	45
IO	46
IO_VREF_6	47
GND	48
IO	49
IO	50
IO_VREF_6	51
IO	52
IO	53
IO	54
M1	55
GND	56
M0	57
VCCO	58
M2	59
IO	60
IO	61
IO	62
IO_VREF_5	63
IO	64
IO	65
GND	66
IO_VREF_5	67
IO	68
IO	69
IO_VREF5	70
IO	71
GND	72
VCCINT	73
IO	74
IO	75
VCCO	76
IO	77
IO	78

Table 5: **CQFP Package (CB228) *(Continued)***

Function	Pin No.
IO_VREF_5	79
IO	80
IO	81
IO	82
VCCINT	83
GCK1	84
VCCO	85
GND	86
GCKO	87
IO	89
IO	90
IO	91
IO_VREF_4	92
IO	93
IO	94
VCCO	95
IO	96
IO	97
IO	98
VCCINT	99
GND	100
IO	101
IO_VREF_4	102
IO	103
IO	104
IO_VREF_4	105
GND	106
IO	107
IO	108
IO_VREF_4	109
IO	110
IO	111
IO	112
GND	113
DONE	114
VCCO	115
PROGRAM	116
IO_INIT	117
IO_D7	118
IO	119

Table 5: **CQFP Package (CB228) *(Continued)***

Function	Pin No.
IO_VREF_3	120
IO	121
IO	122
GND	123
IO_VREF_3	124
IO	125
IO	126
IO_VREF_3	127
IO_D6	128
GND	129
VCCINT	130
IO_D5	131
IO	132
VCCO	133
IO	134
IO	135
IO_VREF_3	136
IO_D4	137
IO	138
IO	139
VCCINT	140
IO_TRDY	141
VCCO	142
GND	143
IO_IRDY	144
IO	145
IO	146
IO	147
IO_D3	148
IO_VREF_2	149
IO	150
IO	151
VCCO	152
IO	153
IO	154
IO_D2	155
VCCINT	156
GND	157
IO_D1	158
IO_VREF_2	159

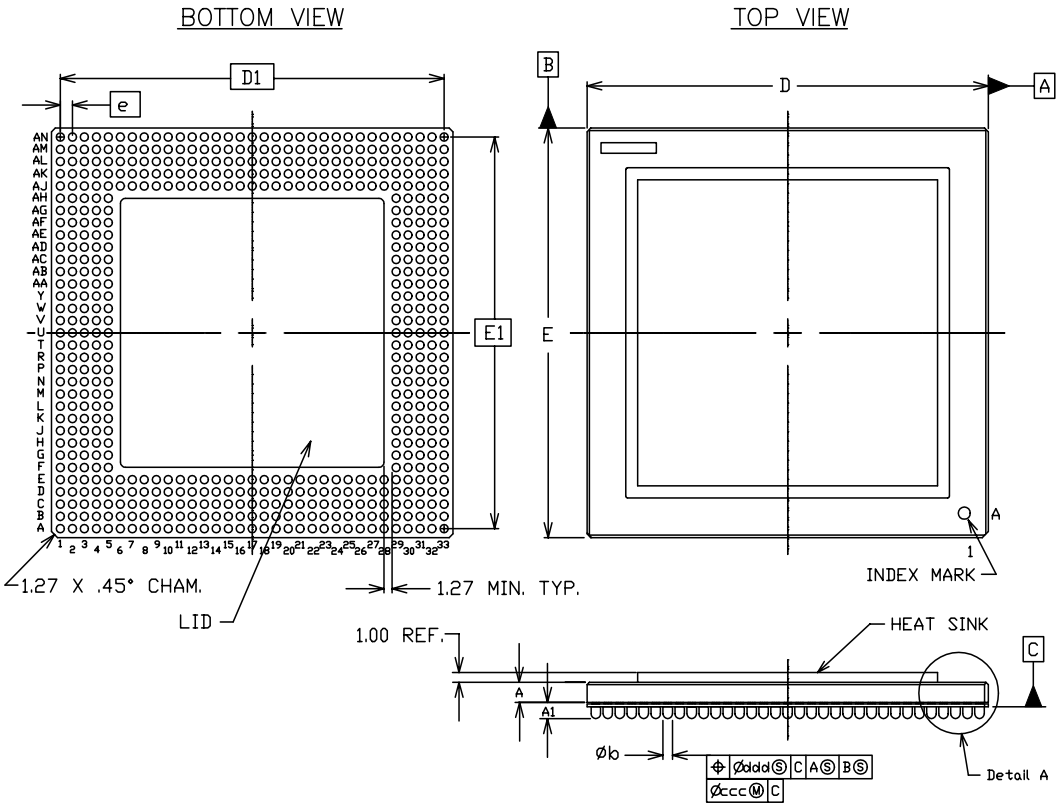
Table 5: **CQFP Package (CB228) *(Continued)***

Function	Pin No.
IO	160
IO	161
IO_VREF_2	162
GND	163
IO	164
IO	165
IO_VREF_2	166
IO	167
IO_DIN_D0	168
IO_DOUT_BUSY	169
CCLK	170
VCCO	171
TDO	172
GND	173
TDI	174
IO_CS	175
IO_WRITE	176
IO	177
IO_VREF_1	178
IO	179
GND	180
IO_VREF_1	181
IO	182
IO	183
IO_VREF_1	184
IO	185
GND	186
VCCINT	187
IO	188
IO	189
IO	190
VCCO	191
IO	192
IO	193
IO_VREF_1	194
IO	195
IO	196
IO	197
IO	198
GCK2	199

Table 5: **CQFP Package (CB228) *(Continued)***

Function	Pin No.
GND	200
VCCO	201
GCK3	202
VCCINT	203
IO	204
IO	205
IO	206
IO_VREF_0	207
IO	208
IO	209
VCCO	210
IO	211
IO	212
IO	213
VCCINT	214
GND	215
IO	216
IO_VREF_0	217
IO	218
IO	219
IO_VREF_0	220
GND	221
IO	222
IO	223
IO_VREF_0	224
IO	225
IO	226
TCK	227
VCCO	228
GND*	1, 8, 14, 27, 42, 48, 56, 66, 72, 86, 100, 106, 113, 123, 129, 143, 157, 163, 173, 180, 186, 200, 215, 221
VCCINT*	15, 30, 41, 73, 83, 99, 130, 140, 156, 187, 203, 214
VCCO	18, 28, 37, 58, 76, 85, 95, 115, 133, 142, 152, 171, 191, 201, 210, 228

Package Drawing CG560 Ceramic Column Grid



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	1.80	2.00	2.20	
A_1	1.55	1.62	1.70	
D/E	42.10	42.50	42.90	
D_1/E_1	40.64 REF.			
e	1.27 BSC			
øb	0.79	0.89	0.99	
ccc	—	—	0.15	
ddd	—	—	0.30	
M	33			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. LEAD FINISH: HIGH TEMP. SOLDER Pb(90%)/Sn(10%)

CG560 Ceramic Column Grid Package

Device/Package Combinations and Maximum I/O

Package	Maximum User I/O (Excluding dedicated clock pins.)			
	XQV100	XQV300	XQV600	XQV1000
PQ240	166	166	-	-
HQ240	-	-	166	-
BG256	180	-	-	-
BG352	-	-	-	-
BG432	-	316	316	-
BG560	-	-	-	-
CB228	162	162	162	
CG560	-	-	-	404

Ordering Information

Example: **XQV300 -4 CB228 M**

Device Type

Speed Grade

Temperature Range

M = Military Ceramic (T_C = -55°C to +125°C)
N = Military Plastic (T_J = -55°C to +125°C)

Number of Pins

Package Type

PQ = Plastic Quad Flat Pack
HQ = High Heat Dissipation QFP (Plastic)
BG = Plastic Ball Grid Array
CB = Ceramic Quad Flat Pack
CG = Ceramic Grid Column Array (Surface Mount)

Revision History

The following table shows the revision history for this document

Date	Version	Revision
10/04/99	1.0	Initial Xilinx release.
06/01/00	1.1	Upated format.

QPRO™ Virtex™ 2.5V Radiation Hardened FPGAs

DS028 (v1.0) April 25, 2000

Advance Product Specification

Features

- 0.22 µm 5-layer epitaxial process
- QML certified
- Radiation hardened FPGAs for space and satellite applications
- Guaranteed total ionizing dose to 100K Rad(si)
- Latch-up immune to LET = 125 MeV cm^2/mg
- SEU immunity achievable with recommended redundancy implementation
- Guaranteed over the full military temperature range (–55°C to +125°C)
- Fast, high-density Field-Programmable Gate Arrays
  - Densities from 100k to 1M system gates
  - System performance up to 200 MHz
  - Hot-swappable for Compact PCI
- Multi-standard SelectI/O™ interfaces
  - 16 high-performance interface standards
  - Connects directly to ZBTRAM devices
- Built-in clock-management circuitry
  - Four dedicated delay-locked loops (DLLs) for advanced clock control
  - Four primary low-skew global clock distribution nets, plus 24 secondary global nets
- Hierarchical memory system
  - LUTs configurable as 16-bit RAM, 32-bit RAM, 16-bit dual-ported RAM, or 16-bit Shift Register
  - Configurable synchronous dual-ported 4k-bit RAMs
  - Fast interfaces to external high-performance RAMs
- Flexible architecture that balances speed and density
  - Dedicated carry logic for high-speed arithmetic
  - Dedicated multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with clock enable, and dual synchronous/asynchronous set and reset
  - Internal 3-state bussing
  - IEEE 1149.1 boundary-scan logic
  - Die-temperature sensing device
- Supported by FPGA Foundation™ and Alliance Development Systems
  - Complete support for Unified Libraries, Relationally Placed Macros, and Design Manager
  - Wide selection of PC and workstation platforms
- SRAM-based in-system configuration
  - Unlimited reprogrammability
  - Four programming modes

2

Description

The QPRO Virtex FPGA family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 5-layer-metal 0.22 µm CMOS process. These advances make QPRO Virtex FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex radiation hardened family comprises the three members shown in Table 1.

Building on experience gained from previous generations of FPGAs, the Virtex family represents a revolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the QPRO Virtex family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

Refer to the "Virtex™ 2.5V Field Programmable Gate Arrays" commercial data sheet for more information on device architecture and timing specifications.

Table 1: **QPRO Virtex Radiation Hardened Field-Programmable Gate Array Family Members.**

Device	System Gates	CLB Array	Logic Cells	Maximum Available I/O	Block RAM Bits	Max Select RAM Bits
XQVR300	322,970	32x48	6,912	316	65,536	98,304
XQVR600	661,111	48x72	15,552	316	98,304	221,184
XQVR1000	1,124,022	64x96	27,648	404	131,072	393,216

Radiation Specifications(1)

Symbol	Description	Min	Max	Units
TID	Total Ionizing Dose Method 1019, Dose Rate ~9.0 rads(Si)/sec	100K		RAD(Si)
SEL	Single Event Latch-up Immunity Heavy Ion Saturation Cross Section LET > 125 MeV cm^2/mg		0	(cm^2/Device)
SEU_{FH}	Single Event Upset CLB Flip-flop Heavy Ion Saturation Cross Section		6.5E – 8	(cm^2/Bit)
SEU_{CH}	Single Event Upset Configuration Latch Heavy Ion Saturation Cross Section		8.0E – 8	(cm^2/Bit)
SEU_{CP}	Single Event Upset Configuration Latch Proton (63MeV) Saturation Cross Section		2.2E – 14	(cm^2/Bit)
SEU_{BH}	Single Event Upset BRAM Bit Heavy Ion Saturation Cross Section		1.6E – 7	(cm^2/Bit)

Notes:
1. For more information, refer to "Radiation Test Results of the Virtex FPGA for Space Based Reconfigurable Computing" and "SEU Mitigation Techniques for Virtex FPGAs in Space Applications" at **http://www.xilinx.com/products/hirel_qml.htm**.

Virtex Electrical Characteristics

The specifications in this advance information data sheet are initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. Contact the factory for design considerations requiring more detailed information.

Virtex DC Characteristics

Absolute Maximum Ratings

Symbol	Description		Min/Max	Units
V_{CCINT}	Supply voltage relative to GND		–0.5 to 3.0	V
V_{CCO}	Supply voltage relative to GND		–0.5 to 4.0	V
V_{REF}	Input reference voltage		–0.5 to 3.6	V
V_{IN}	Input voltage relative to GND	Using V_{REF}	–0.5 to 3.6	V
		Internal threshold	–0.5 to 5.5	V
V_{TS}	Voltage applied to 3-state output		–0.5 to 5.5	V
V_{CC}	Longest supply voltage rise time from 1V to 2.375V		50	ms
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s at 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature		+150	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. Power supplies may turn on in any order.
3. For protracted periods (e.g., longer than a day), V_{IN} should not exceed V_{CCO} by more that 3.6V.

Recommended Operating Conditions

Symbol	Description	Device	Min	Max	Units
V_{CCINT}	Supply voltage relative to GND, T_C = –55°C to +125°C		2.5 – 5%	2.5 + 5%	V
V_{CCO}	Supply voltage relative to GND, T_C = –55°C to +125°C		1.2	3.6	V
T_{IN}	Input signal transition time			250	ns
ICC_{INTQ}	Quiescent V_{CCINT} supply current	XQVR300		150	mA
		XQVR600		200	mA
		XQVR1000		200	mA
ICC_{CCOQ}	Quiescent V_{CCO} supply current	XQVR300		4.0	mA
		XQVR600		4.0	mA
		XQVR1000		4.0	mA

Notes:
1. Correct operation is guaranteed with a minimum V_{CCINT} of 2.25V (Nominal V_{CCINT} – 10%). Below the minimum value stated above, all delay parameters increase by 3% for each 50 mV reduction in V_{CCINT} below the specified range.
2. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
3. Input and output measurement threshold is ~50% of V_{CC}.

QPRO Virtex Pin Outs

Pinout Tables

See the Xilinx WebLINX web site (http://www.xilinx.com/partinfo/databook.htm) for updates or additional pinout information. For convenience, Table 2 and Table 3 list the locations of special-purpose and power-supply pins. Pins not listed are user I/Os.

Table 2: **Virtex Ceramic Column Grid (CG560) Pinout**

Pin Name	Device	CG560
GCK0	XQVR1000	AL17
GCK1		AJ17
GCK2		D17
GCK3		A17
M0		AJ29
M1		AK30
M2		AN32
CCLK		C4
PROGRAM		AM1
DONE		AJ5
INIT		AH5
BUSY/DOUT		D4
D0/DIN		E4

Table 2: **Virtex Ceramic Column Grid (CG560) Pinout *(Continued)***

Pin Name	Device	CG560
D1	XQVR1000	K3
D2		L4
D3		P3
D4		W4
D5		AB5
D6		AC4
D7		AJ4
WRITE		D6
CS		A2
TDI		D5
TDO		E6
TMS		B33
TCK		E29
DXN		AK29
DXP		AJ28

Table 2: **Virtex Ceramic Column Grid (CG560) Pinout *(Continued)***

Pin Name	Device	CG560
V_{CCINT} (V_{CCINT} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XQVR1000	A21, B12, B14, B18, B28, C22, C24, E9, E12, F2, H30, J1, K32, M3, N1, N29, N33, U5, U30, Y2, Y31, AB2, AB32, AD2, AD32, AG3, AG31, AJ13, AK8, AK11, AK17, AK20, AL14, AL22, AL27, AN25
V_{CCO}, Bank 0		A22, A26, A30, B19, B32
V_{CCO}, Bank 1		A10, A16, B13, C3, E5
V_{CCO}, Bank 2		B2, D1, H1, M1, R2
V_{CCO}, Bank 3		V1, AA2, AD1, AK1, AL2
V_{CCO}, Bank 4		AM2, AM15, AN4, AN8, AN12
V_{CCO}, Bank 5		AL31, AM21, AN18, AN24, AN30
V_{CCO}, Bank 6	XQVR1000	W32, AB33, AF33, AK33, AM32
V_{CCO}, Bank 7	XQVR1000	C32, D33, K33, N32, T33

Table 2: **Virtex Ceramic Column Grid (CG560) Pinout *(Continued)***

Pin Name	Device	CG560
V_{REF}, Bank 0 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQVR1000	A19, D20, D26, D29, E21, E23, E24, E27,
V_{REF}, Bank 1 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQVR1000	A6, D7, D10, D11, D13, D16, E7, E15
V_{REF}, Bank 2 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQVR1000	B3, G5, H4, K5, L5, N5, P4, R1
V_{REF}, Bank 3 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQVR1000	V4, W5, AA4, AD3, AE5, AF1, AH4, AK2

Table 2: **Virtex Ceramic Column Grid (CG560) Pinout *(Continued)***

Pin Name	Device	CG560
V_{REF}, Bank 4 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQVR1000	AK13, AL7, AL9, AL10, AL16, AM4, AM14,AN3
V_{REF}, Bank 5 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQVR1000	AJ18, AJ25, AK28, AL20, AL24, AL29, AM26, AN23
V_{REF}, Bank 6 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQVR1000	V29, Y32, AA30,AD31, AE29, AK32, AE31, AH30
V_{REF}, Bank 7 (V_{REF} pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.) Within each bank, if input reference voltage is not required, all V_{REF} pins are general I/O.	XQVR1000	D31, E31, G31, H32, K31, P31, T31

Table 2: **Virtex Ceramic Column Grid (CG560) Pinout *(Continued)***

Pin Name	Device	CG560
GND	XQVR1000	A1, A7, A12, A14, A18, A20, A24, A29, A32, A33, B1, B6, B9, B15, B23, B27, B31, C2, E1, F32, G2, G33, J32, K1, L2, M33, P1, P33, R32, T1, V33, W2, Y1, Y33, AB1, AC32, AD33, AE2, AG1, AG32, AH2, AJ33, AL32, AM3, AM7, AM11, AM19, AM25, AM28, AM33, AN1, AN2, AN5, AN10, AN14, AN16, AN20, AN22, AN27, AN33
GND*	All	
No Connect		C31, AC2, AK4, AL3

* 16 extra balls (grounded) at package center.

Table 3: **CQFP Package (CB228)**

Function	Pin #	Bank #
GND	1	7
TMS	2	
IO	3	
IO	4	
IO_VREF_7	5	
IO	6	
IO	7	
GND	8	
IO	9	
IO	10	
IO	11	
IO_VREF_7	12	
IO	13	
GND	14	
V_{CCINT}	15	
IO	16	
IO	17	
V_{CCO}	18	
IO	19	
IO	20	
IO_VREF_7	21	
IO	22	
IO	23	
IO	24	
IO	25	
IO_IRDY	26	
GND	27	

Table 3: **CQFP Package (CB228)** ***(Continued)***

Function	Pin #	Bank #
V_{CCO}	28	6
IO_TRDY	29	
V_{CCINT}	30	
IO	31	
IO	32	
IO	33	
IO_VREF_6	34	
IO	35	
IO	36	
V_{CCO}	37	
IO	38	
IO	39	
IO	40	
V_{CCINT}	41	
GND	42	
IO	43	
IO_VREF_6	44	
IO	45	
IO	46	
IO_VREF_6	47	
GND	48	
IO	49	
IO	50	
IO_VREF_6	51	
IO	52	
IO	53	
IO	54	
M1	55	
GND	56	
M0	57	

Table 3: **CQFP Package (CB228) *(Continued)***

Function	Pin #	Bank #
V_{CCO}	58	5
M2	59	
IO	60	
IO	61	
IO	62	
IO_VREF_5	63	
IO	64	
IO	65	
GND	66	
IO_VREF_5	67	
IO	68	
IO	69	
IO_VREF5	70	
IO	71	
GND	72	
V_{CCINT}	73	
IO	74	
IO	75	
V_{CCO}	76	
IO	77	
IO	78	
IO_VREF_5	79	
IO	80	
IO	81	
IO	82	
V_{CCINT}	83	4
GCK1	84	
VCCO	85	
GND	86	
GCKO	87	
IO	89	
IO	90	
IO	91	
IO_VREF_4	92	

Table 3: **CQFP Package (CB228) *(Continued)***

Function	Pin #	Bank #
IO	93	4
IO	94	
V_{CCO}	95	
IO	96	
IO	97	
IO	98	
V_{CCINT}	99	
GND	100	
IO	101	
IO_VREF_4	102	
IO	103	
IO	104	
IO_VREF_4	105	
GND	106	
IO	107	
IO	108	
IO_VREF_4	109	
IO	110	
IO	111	
IO	112	
GND	113	
DONE	114	
V_{CCO}	115	

Table 3: **CQFP Package (CB228) *(Continued)***

Function	Pin #	Bank #
PROGRAM	116	3
IO_INIT	117	
IO_D7	118	
IO	119	
IO_VREF_3	120	
IO	121	
IO	122	
GND	123	
IO_VREF_3	124	
IO	125	
IO	126	
IO_VREF_3	127	
IO_D6	128	
GND	129	
V_{CCINT}	130	
IO_D5	131	
IO	132	
V_{CCO}	133	
IO	134	
IO	135	
IO_VREF_3	136	
IO_D4	137	
IO	138	
IO	139	
V_{CCINT}	140	
IO_TRDY	141	
V_{CCO}	142	

Table 3: **CQFP Package (CB228) *(Continued)***

Function	Pin #	Bank #
GND	143	2
IO_IRDY	144	
IO	145	
IO	146	
IO	147	
IO_D3	148	
IO_VREF_2	149	
IO	150	
IO	151	
V_{CCO}	152	
IO	153	
IO	154	
IO_D2	155	
V_{CCINT}	156	
GND	157	
IO_D1	158	
IO_VREF_2	159	
IO	160	
IO	161	
IO_VREF_2	162	
GND	163	
IO	164	
IO	165	
IO_VREF_2	166	
IO	167	
IO_DIN_D0	168	
IO_DOUT_BUSY	169	
CCLK	170	
V_{CCO}	171	

Table 3: **CQFP Package (CB228) *(Continued)***

Function	Pin #	Bank #
TDO	172	1
GND	173	
TDI	174	
IO_CS	175	
IO_WRITE	176	
IO	177	
IO_VREF_1	178	
IO	179	
GND	180	
IO_VREF_1	181	
IO	182	
IO	183	
IO_VREF_1	184	
IO	185	
GND	186	
V_{CCINT}	187	
IO	188	
IO	189	
IO	190	
V_{CCO}	191	
IO	192	
IO	193	
IO_VREF_1	194	
IO	195	
IO	196	
IO	197	
IO	198	
GCK2	199	
GND	200	
V_{CCO}	201	

Table 3: **CQFP Package (CB228) *(Continued)***

Function	Pin #	Bank #
GCK3	202	0
V_{CCINT}	203	
IO	204	
IO	205	
IO	206	
IO_VREF_0	207	
IO	208	
IO	209	
V_{CCO}	210	
IO	211	
IO	212	
IO	213	
V_{CCINT}	214	
GND	215	
IO	216	
IO_VREF_0	217	
IO	218	
IO	219	
IO_VREF_0	220	
GND	221	
IO	222	
IO	223	
IO_VREF_0	224	
IO	225	
IO	226	
TCK	227	
V_{CCO}	228	

Table 3: **CQFP Package (CB228) *(Continued)***

Function	Pin #	Bank #
GND*	1, 8, 14, 27, 42, 48, 56, 66, 72, 86, 100, 106, 113, 123, 129, 143, 157, 163, 173, 180, 186, 200, 215, 221	
V_{CCINT}*	15, 30, 41, 73, 83, 99, 130, 140, 156, 187, 203, 214	
V_{CCO}	18, 28, 37, 58, 76, 85, 95, 115, 133, 142, 152, 171, 191, 201, 210, 228	

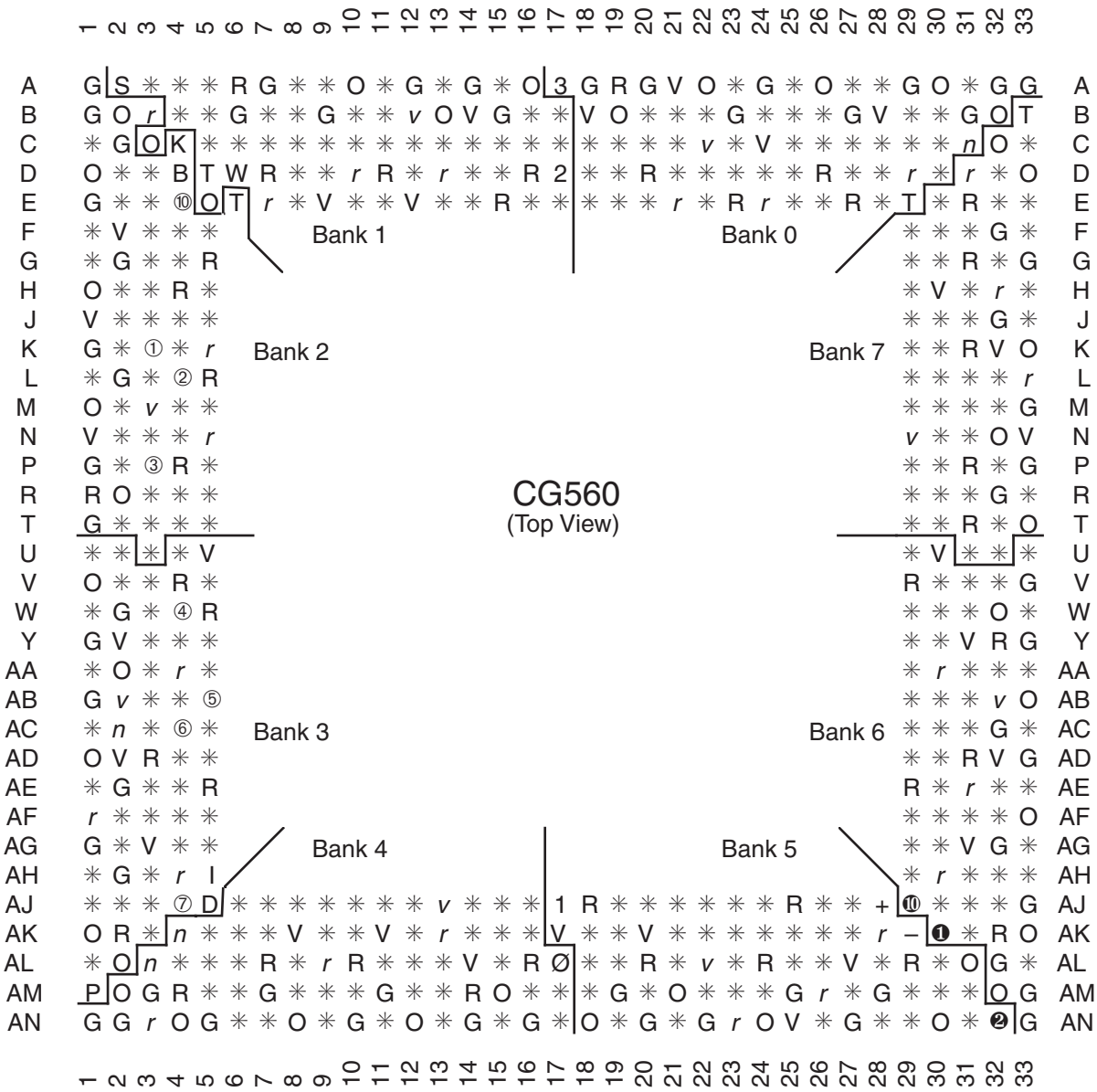
Pinout Diagrams

The following diagrams illustrate the locations of special-purpose pins on Virtex FPGAs. Table 4 lists the symbols used in these diagrams. The diagrams also show I/O-bank boundaries.

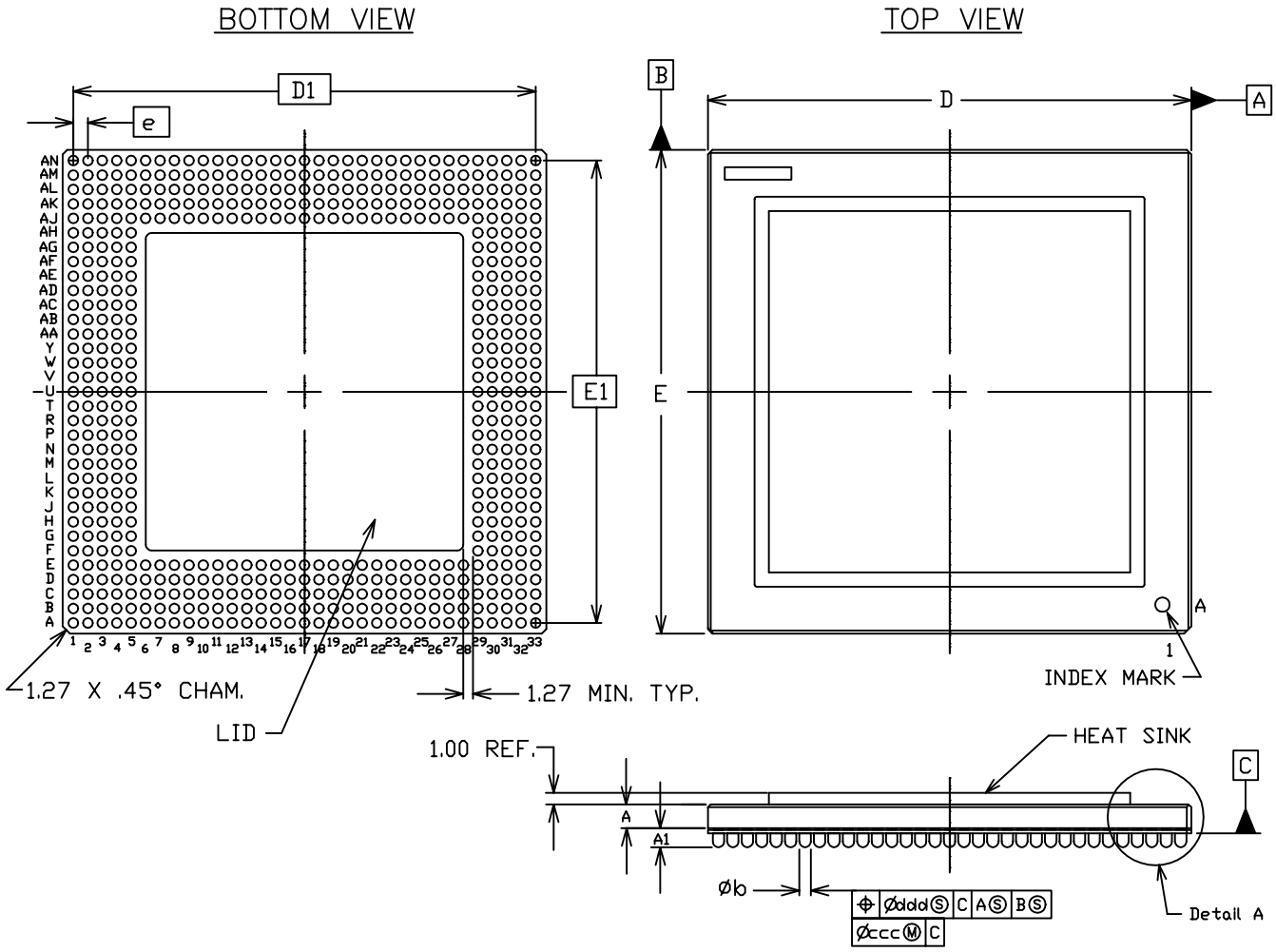
Table 4: **Pinout Diagram Symbols**

Symbol	Pin Function
S	General I/O
d	Device-dependent general I/O, n/c on smaller devices
V	V_{CCINT}
v	Device-dependent V_{CCINT}, n/c on smaller devices
O	V_{CCO}
R	V_{REF}
r	Device-dependent V_{REF}, remains I/O on smaller devices
G	Ground
Ø, 1, 2, 3	Global Clocks
⓿, ❶, ❷	M0, M1, M2
⓾, ①, ②, ③, ④, ⑤, ⑥, ⑦	D0/DIN, D1, D2, D3, D4, D5, D6, D7
B	DOUT/BUSY
D	DONE
P	PROGRAM
I	INIT
K	CCLK
W	WRITE
S	CS
T	Boundary-scan test aAccess port
+	Temperature diode, anode
–	Temperature diode, cathode
n	No connect

CG560 Pin Function Diagram



Package Drawing CG560 Ceramic Column Grid



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	1.80	2.00	2.20	
A_1	1.55	1.62	1.70	
D/E	42.10	42.50	42.90	
D_1/E_1	40.64 REF.			
e	1.27 BSC			
øb	0.79	0.89	0.99	
ccc			0.15	
ddd			0.30	
M	33			2

NOTES:

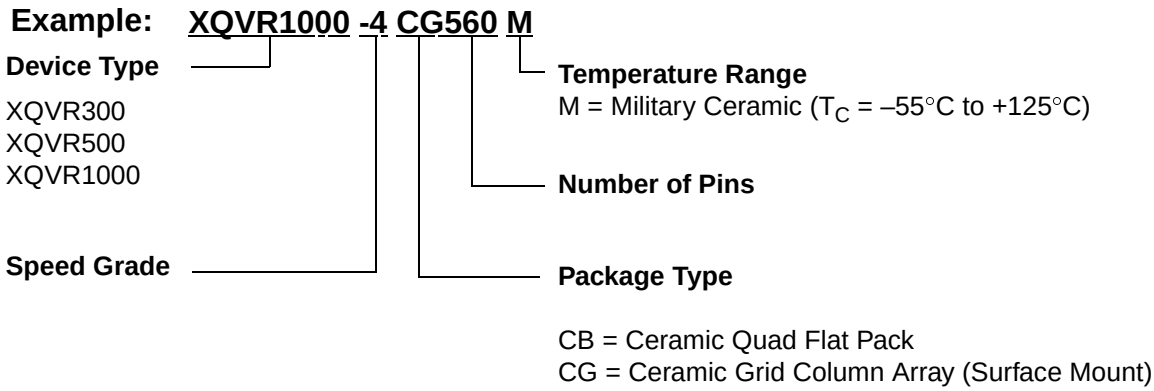
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. LEAD FINISH: HIGH TEMP. SOLDER Pb(90%)/Sn(10%)

DS028_01_011900

Device/Package Combinations and Maximum I/O

Package	Maximum User I/O (excluding dedicated clock pins)		
	XQVR300	XQVR600	XQVR1000
CB228	162	162	
CG560			404

Ordering Information



Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/25/00	1.0	Initial Xilinx release.

QPRO XQ4000E/EX QML High-Reliability FPGAs

DS021 (v2.2) June 25, 2000 **Product Specification**

Product Features

- Certified to MIL-PRF-38535, appendix A QML (Qualified Manufacturers Listing)
- Also available under the following Standard Microcircuit Drawings (SMD)
  - XC4005E 5962-97522
  - XC4010E 5962-97523
  - XC4013E 5962-97524
  - XC4025E 5962-97525
  - XC4028EX 5962-98509
- For more information contact the Defense Supply Center Columbus (DSCC) http://www.dscc.dla.mis/v/va/smd/smdsrch.html
- System featured Field-Programmable Gate Arrays
  - Select-RAM™ memory: on-chip ultra-fast RAM with
    - Synchronous write option
    - Dual-port RAM option
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - Eight global low-skew clock or signal distribution networks
- System Performance beyond 60 MHz
- Flexible Array Architecture
- Low Power Segmented Routing Architecture
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary scan logic support
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12 mA sink current per XQ4000E/EX output
- Configured by Loading Binary File
  - Unlimited reprogrammability
- Readback Capability
  - Program verification
  - Internal node observability
- Backward Compatible with XC4000 Devices
- Development System runs on most common computer platforms
  - Interfaces to popular design environments
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization
- Available Speed Grades:
  - XQ4000E -3 for plastic packages only
  - -4 for ceramic packages only
  - XQ4028EX -4 for all packages

More Information

For more information refer to Xilinx XC4000E and XC4000X series Field Programmable Gate Arrays product specification. This data sheet contains pinout tables for XQ4010E only. Refer to Xilinx web site for pinout tables for other devices. (Pinouts for XQ4000E/EX are identical to XC4000E/EX.)
(http://www.xilinx.com/partinfo/databook.htm)

Table 1: **XQ4000E/EX Field Programmable Gate Arrays**

Device	Max. Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)(1)	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. Decode Inputs per Side	Max. User I/O	Packages
XQ4005E	5,000	6,272	3,000 - 9,000	14 x 14	196	616	42	112	PG156, CB164
XQ4010E	10,000	12,800	7,000 - 20,000	20 x 20	400	1,120	60	160	PG191, CB196, HQ208
XQ4013E	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	72	192	PG223, CB228, HQ240
XQ4025E	25,000	32,768	15,000 - 45,000	32 x 32	1,024	2,560	96	256	PG299, CB228
XQ4028EX	28,000	32,768	18,000 - 50,000	32 x 32	1,024	2,560	96	256	PG299, CB228, HQ240, BG352

Notes:
1. Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

XQ4000E Switching Characteristics

XQ4000E Absolute Maximum Ratings(1)

Symbol	Description			Units
V_{CC}	Supply voltage relative to GND		–0.5 to +7.0	V
V_{IN}	Input voltage relative to GND(2)		–0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to High-Z output(2)		–0.5 to V_{CC} + 0.5	V
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic package	+150	°C
		Plastic package	+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. Maximum DC excursion above V_{CC} or below Ground must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0V or overshoot to V_{CC} + 2.0V, provided this over or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

XQ4000E Recommended Operating Conditions(1,2)

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = –55°C to +125°C	Plastic	4.5	5.5	V
	Supply voltage relative to GND, T_C = –55°C to +125°C	Ceramic	4.5	5.5	V
V_{IH}	High-Level Input Voltage	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-Level Input Voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time		-	250	ns

Notes:
1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Input and output measurement threshold are 1.5V for TTL and 2.5V for CMOS.

XQ4000E DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = –4.0 mA, V_{CC} min	TTL outputs	2.4	-	V
	High-level output voltage @ I_{OH} = –1.0 mA, V_{CC} min	CMOS outputs	V_{CC} – 0.5	-	V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} min(1)	TTL outputs	-	0.4	V
		CMOS outputs	-	0.4	V
I_{CCO}	Quiescent FPGA supply current(2)		-	50	mA
I_L	Input or output leakage current		–10	+10	µA
C_{IN}	Input capacitance (sample tested)		-	16	pF
I_{RIN}	Pad pull-up (when selected) at V_{IN} = 0V (sample tested)(3)		–0.02	–0.25	mA
I_{RLL}	Horizontal longline pull-up (when selected) at logic Low(3)		0.2	2.5	mA

Notes:
1. With 50% of the outputs simultaneously sinking 12 mA, up to a maximum of 64 pins.
2. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the FPGA configured with the development system Tie option.
3. Characterized Only.

XQ4000E Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Note: -3 Speed Grade only applies to XQ4010E and XQ4013E Plastic Package options only. -4 Speed Grade applies to all XQ devices and is only available in Ceramic Packages only.

XQ4000E Global Buffer Switching Characteristics

Symbol	Description	Device	-3(1) Max	-4(2) Max	Units
T_{PG}	From pad through primary buffer, to any clock K	XQ4005E	-	7.0	ns
		XQ4010E	6.3	11.0	ns
		XQ4013E	6.8	11.5	ns
		XQ4025E	-	12.5	ns
T_{SG}	From pad through secondary buffer, to any clock K	XQ4005E	-	7.5	ns
		XQ4010E	6.8	11.5	ns
		XQ4013E	7.3	12.0	ns
		XQ4025E	-	13.0	ns

Notes:
1. For plastic package options only.
2. For ceramic package options only.

XQ4000E Horizontal Longline Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist.

These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E devices unless otherwise noted.

The following guidelines reflect worst-case values over the recommended operating conditions.

Symbol	Description	Device	-3 Max	-4 Max	Units
TBUF Driving a Horizontal Longline (LL):					
T_{IO1}	I going High or Low to LL going High or Low, while T is Low. Buffer is constantly active.(1)	XQ4005E	-	5.0	ns
		XQ4010E	6.4	8.0	ns
		XQ4013E	7.2	9.0	ns
		XQ4025E	-	11.0	ns
T_{IO2}	I going Low to LL going from resistive pull-up High to active Low. TBUF configured as open-drain.(1)	XQ4005E	-	6.0	ns
		XQ4010E	6.9	10.5	ns
		XQ4013E	7.7	11.0	ns
		XQ4025E	-	12.0	ns
T_{ON}	T going Low to LL going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.(1)	XQ4005E	-	7.0	ns
		XQ4010E	7.3	8.5	ns
		XQ4013E	7.5	8.7	ns
		XQ4025E	-	11.0	ns
T_{OFF}	T going High to TBUF going inactive, not driving LL.	XQ4005E	-	1.8	ns
		XQ4010E	1.5	1.8	ns
		XQ4013E	1.5	1.8	ns
		XQ4025E	-	1.8	ns
T_{PUS}	T going High to LL going from Low to High, pulled up by a single resistor.(1)	XQ4005E	-	23.0	ns
		XQ4010E	22.0	29.0	ns
		XQ4013E	26.0	32.0	ns
		XQ4025E	-	42.0	ns
T_{PUF}	T going High to LL going from Low to High, pulled up by two resistors.(1)	XQ4005E	-	10.0	ns
		XQ4010E	11.0	13.5	ns
		XQ4013E	13.0	15.0	ns
		XQ4025E	-	18.0	ns

Notes:
1. These values include a minimum load. Use the static timing analyzer to determine the delay for each destination.

XQ4000E Wide Decoder Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist.

These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E devices unless otherwise noted.

The following guidelines reflect worst-case values over the recommended operating conditions.

Symbol	Description[1,2]	Device	-3	-4	Units
			Max	Max	
T_{WAF}	Full length, both pull-ups, inputs from IOB I-pins	XQ4005E	-	9.5	ns
		XQ4010E	9.0	15.0	ns
		XQ4013E	11.0	16.0	ns
		XQ4025E	-	18.0	ns
T_{WAFL}	Full length, both pull-ups, inputs from internal logic	XQ4005E	-	12.5	ns
		XQ4010E	11.0	18.0	ns
		XQ4013E	13.0	19.0	ns
		XQ4025E	-	21.0	ns
T_{WAO}	Half length, one pull-up, inputs from IOB I-pins	XQ4005E	-	10.5	ns
		XQ4010E	10.0	16.0	ns
		XQ4013E	12.0	17.0	ns
		XQ4025E	-	19.0	ns
T_{WAOL}	Half length, one pull-up, inputs from internal logic	XQ4005E	-	12.5	ns
		XQ4010E	12.0	18.0	ns
		XQ4013E	14.0	19.0	ns
		XQ4025E	-	21.0	ns

Notes:

1. These delays are specified from the decoder input to the decoder output.
2. Fewer than the specified number of pull-up resistors can be used, if desired. Using fewer pull-ups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pull-ups are used.

XQ4000E CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist.

These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E devices unless otherwise noted.

Symbol	Description	-3		-4		Units
		Min	Max	Min	Max	
Combinatorial Delays						
T_{ILO}	F/G inputs to X/Y outputs	-	2.01	-	2.7	ns
T_{IHO}	F/G inputs via H to X/Y outputs	-	4.3	-	4.7	ns
T_{HH0O}	C inputs via SR through H to X/Y outputs	-	3.3	-	4.1	ns
T_{HH1O}	C inputs via H to X/Y outputs	-	3.6	-	3.7	ns
T_{HH2O}	C inputs via D_{IN} through H to X/Y outputs	-	3.6	-	4.5	ns
CLB Fast Carry Logic						
T_{OPCY}	Operand inputs (F1, F2, G1, G4) to C_{OUT}	-	2.6	-	3.2	ns
T_{ASCY}	Add/Subtract input (F3) to C_{OUT}	-	4.4	-	5.5	ns
T_{INCY}	Initialization inputs (F1, F3) to C_{OUT}	-	1.7	-	1.7	ns
T_{SUM}	C_{IN} through function generators to X/Y outputs	-	3.3	-	3.8	ns
T_{BYP}	C_{IN} to C_{OUT}, bypass function generators	-	0.7	-	1.0	ns
Sequential Delays						
T_{CKO}	Clock K to outputs Q	-	2.8	-	3.7	ns
Setup Time before Clock K						
T_{ICK}	F/G inputs	3.0	-	4.0	-	ns
T_{IHCK}	F/G inputs via H	4.6	-	6.1	-	ns
T_{HH0CK}	C inputs via H0 through H	3.6	-	4.5	-	ns
T_{HH1CK}	C inputs via H1 through H	4.1	-	5.0	-	ns
T_{HH2CK}	C inputs via H2 through H	3.8	-	4.8	-	ns
T_{DICK}	C inputs via D_{IN}	2.4	-	3.0	-	ns
T_{ECCK}	C inputs via EC	3.0	-	4.0	-	ns
T_{RCK}	C inputs via S/R, going Low (inactive)	4.0	-	4.2	-	ns
T_{CCK}	C_{IN} input via F/G	2.1	-	2.5	-	ns
T_{CHCK}	C_{IN} input via F/G and H	3.5	-	4.2	-	ns

XQ4000E CLB Switching Characteristic Guidelines *(continued)*

Symbol	Description	-3		-4		Units
		Min	Max	Min	Max	
Hold Time after Clock K						
T_{CKI}	F/G inputs	0	-	0	-	ns
T_{CKIH}	F/G inputs via H	0	-	0	-	ns
T_{CKHH0}	C inputs via H0 through H	0	-	0	-	ns
T_{CKHH1}	C inputs via H1 through H	0	-	0	-	ns
T_{CKHH2}	C inputs via H2 through H	0	-	0	-	ns
T_{CKDI}	C inputs via DIN/H2	0	-	0	-	ns
T_{CKEC}	C inputs via EC	0	-	0	-	ns
T_{CKR}	C inputs via SR, going Low (inactive)	0	-	0	-	ns
Clock						
T_{CH}	Clock High time	4.0	-	4.5	-	ns
T_{CL}	Clock Low time	4.0	-	4.5	-	ns
Set/Reset Direct						
T_{RPW}	Width (High)	4.0	-	5.5	-	ns
T_{RIO}	Delay from C inputs via S/R, going High to Q	-	4.0	-	6.5	ns
Master Set/Reset(1)						
T_{MRW}	Width (High or Low)	11.5	-	13.0	-	ns
T_{MRQ}	Delay from Global Set/Reset net to Q	-	18.7	-	23.0	ns
T_{MRK}	Global Set/Reset inactive to first active clock K edge	-	18.7	-	23.0	ns
F_{TOG}	Toggle Frequency(2)	-	125	-	111	MHz

Notes:
1. Timing is based on the XC4005E. For other devices see the static timing analyzer.
2. Export Control Max. flip-flop toggle rate.

XQ4000E CLB Edge-Triggered (Synchronous) RAM Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E/EX devices unless otherwise noted.

Single-Port RAM Synchronous (Edge-Triggered) Write Operation Characteristics

Symbol	Write Operation Description	Size	-3		-4		Units
			Min	Max	Min	Max	
T_{WCS}	Address write cycle time (clock K period)	16x2	14.4	-	15.0	-	ns
T_{WCTS}		32x1	14.4	-	15.0	-	ns
T_{WPS}	Clock K pulse width (active edge)	16x2	7.2	1 ms	7.5	1 ms	ns
T_{WPTS}		32x1	7.2	1 ms	7.5	1 ms	ns
T_{ASS}	Address setup time before clock K	16x2	2.4	-	2.8	-	ns
T_{ASTS}		32x1	2.4	-	2.8	-	ns
T_{AHS}	Address hold time after clock K	16x2	0	-	0	-	ns
T_{AHTS}		32x1	0	-	0	-	ns
T_{DSS}	D_{IN} setup time before clock K	16x2	3.2	-	3.5	-	ns
T_{DSTS}		32x1	1.9	-	2.5	-	ns
T_{DHS}	D_{IN} hold time after clock K	16x2	0	-	0	-	ns
T_{DHTS}		32x1	0	-	0	-	ns
T_{WSS}	WE setup time before clock K	16x2	2.0	-	2.2	-	ns
T_{WSTS}		32x1	2.0	-	2.2	-	ns
T_{WHS}	WE hold time after clock K	16x2	0	-	0	-	ns
T_{WHTS}		32x1	0	-	0	-	ns
T_{WOS}	Data valid after clock K	16x2	8.8	-	-	10.3	ns
T_{WOTS}		32x1	10.3	-	-	11.6	ns

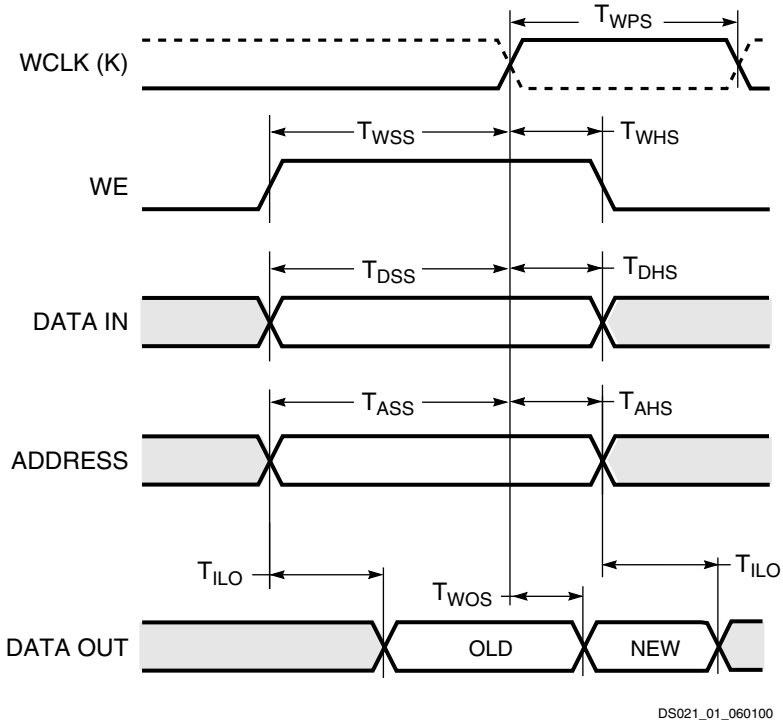
Notes:
1. Timing for the 16x1 RAM option is identical to 16x2 RAM timing.
2. Applicable Read timing specifications are identical to Level-Sensitive Read timing.

Dual-Port RAM Synchronous (Edge-Triggered) Write Operation Characteristics

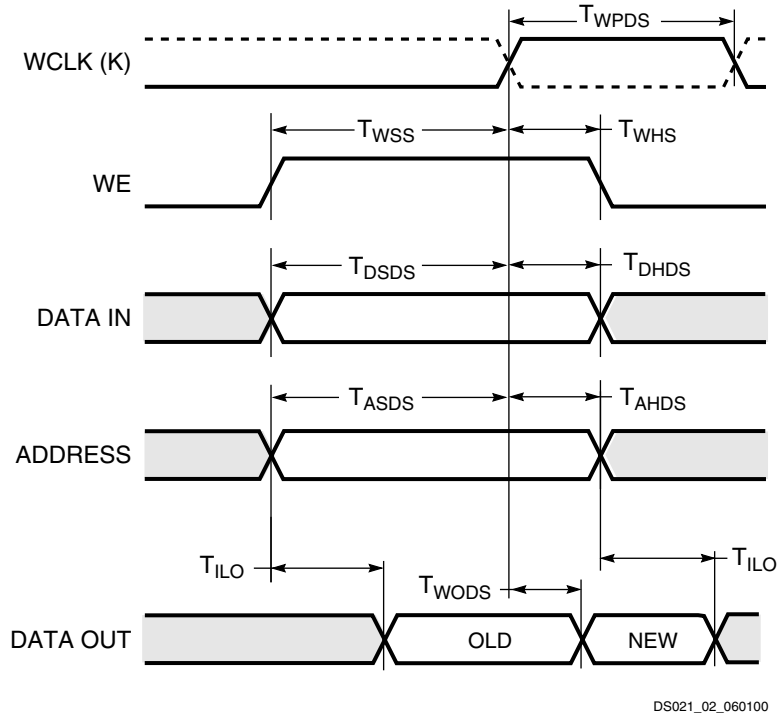
Symbol	Write Operation Description	Size[1]	-3		-4		Units
			Min	Max	Min	Max	
T_{WCDS}	Address write cycle time (clock K period)	16x1	14.4		15.0		ns
T_{WPDS}	Clock K pulse width (active edge)	16x1	7.2	1 ms	7.5	1 ms	ns
T_{ASDS}	Address setup time before clock K	16x1	2.5	-	2.8	-	ns
T_{AHDS}	Address hold time after clock K	16x1	0	-	0	-	ns
T_{DSDS}	D_{IN} setup time before clock K	16x1	2.5	-	2.2	-	ns
T_{DHDS}	D_{IN} hold time after clock K	16x1	0	-	0	-	ns
T_{WSDS}	WE setup time before clock K	16x1	1.8	-	2.2	-	ns
T_{WHDS}	WE hold time after clock K	16x1	0	-	0.3	-	ns
T_{WODS}	Data valid after clock K	16x1	-	7.8	-	10.0	ns

Notes:
1. Applicable Read timing specifications are identical to Level-Sensitive Read timing.

XQ4000E CLB RAM Synchronous (Edge-Triggered) Write Timing Waveform



XQ4000E CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing Waveform



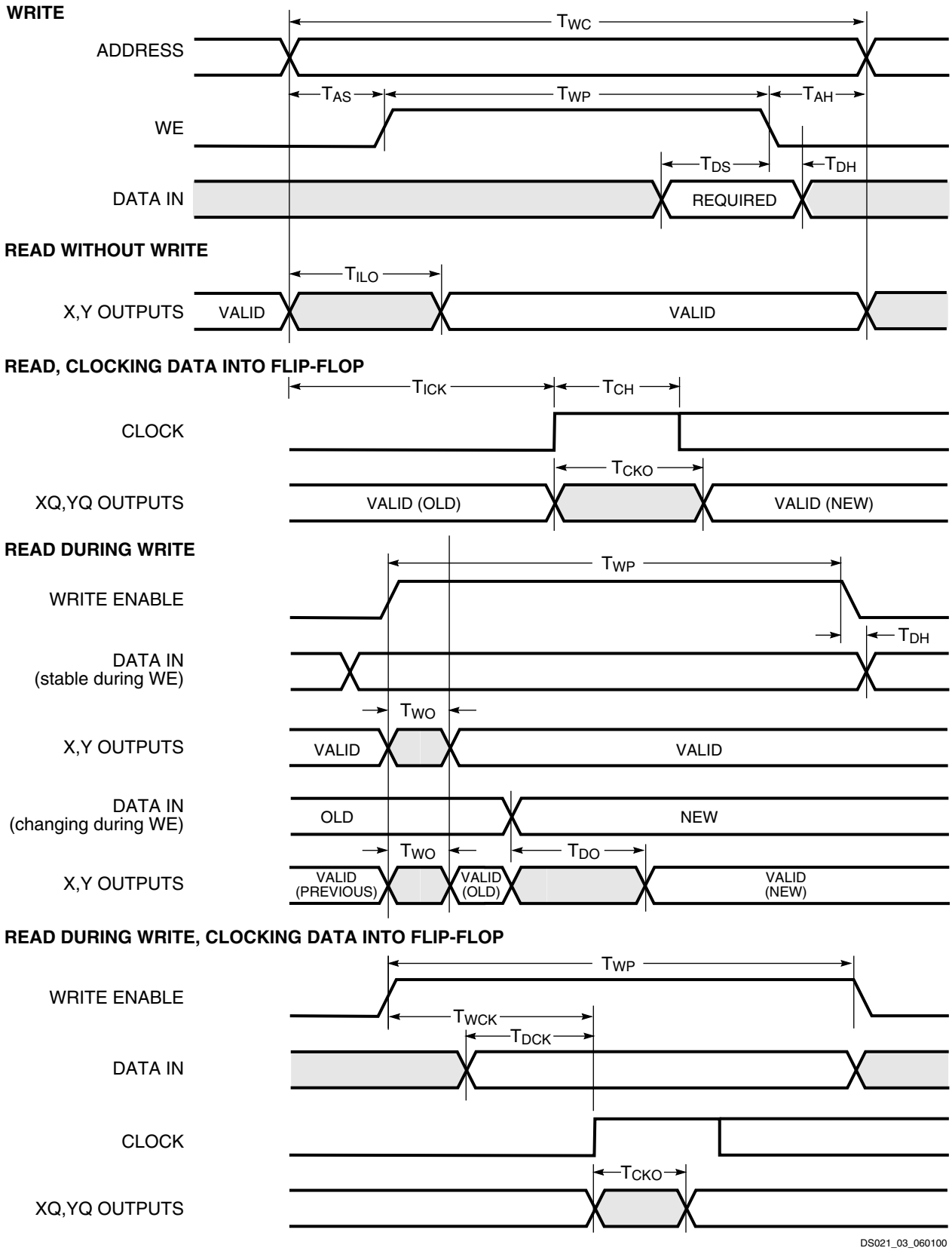
XQ4000E CLB Level-Sensitive RAM Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E devices unless otherwise noted.

Symbol	Single Port RAM	Size	-3		-4		Units
			Min	Max	Min	Max	
Write Operation							
T_{WC}	Address write cycle time	16x2	8.0	-	8.0	-	ns
T_{WCT}		32x1	8.0	-	8.0	-	ns
T_{WP}	Write Enable pulse width (High)	16x2	4.0	-	4.0	-	ns
T_{WPT}		32x1	4.0	-	4.0	-	ns
T_{AS}	Address setup time before WE	16x2	2.0	-	2.0	-	ns
T_{AST}		32x1	2.0	-	2.0	-	ns
T_{AH}	Address hold time after end of WE	16x2	2.0	-	2.5	-	ns
T_{AHT}		32x1	2.0	-	2.0	-	ns
T_{DS}	D_{IN} setup time before end of WE	16x2	2.2	-	4.0	-	ns
T_{DST}		32x1	2.2	-	5.0	-	ns
T_{DH}	D_{IN} hold time after end of WE	16x2	2.0	-	2.0	-	ns
T_{DHT}		32x1	2.0	-	2.0	-	ns
Read Operation							
T_{RC}	Address read cycle time	16x2	3.1	-	4.5	-	ns
T_{RCT}		32x1	5.5	-	6.5	-	ns
T_{ILO}	Data valid after address change (no Write Enable)	16x2	-	1.8	-	2.7	ns
T_{IHO}		32x1	-	3.2	-	4.7	ns
Read Operation, Clocking Data into Flip-Flop							
T_{ICK}	Address setup time before clock K	16x2	3.0	-	4.0	-	ns
T_{IHCK}		32x1	4.6	-	6.1	-	ns
Read During Write							
T_{WO}	Data valid after WE goes active (D_{IN} stable before WE)	16x2	-	6.0	-	10.0	ns
T_{WOT}		32x1	-	7.3	-	12.0	ns
T_{DO}	Data valid after D_{IN} (D_{IN} changes during WE)	16x2	-	6.6	-	9.0	ns
T_{DOT}		32x1	-	7.6	-	11.0	ns
Read During Write, Clocking Data into Flip-Flop							
T_{WCK}	WE setup time before clock K	16x2	6.0	-	8.0	-	ns
T_{WCKT}		32x1	6.8	-	9.6	-	ns
T_{DCK}	Data setup time before clock K	16x2	5.2	-	7.0	-	ns
T_{DOCK}		32x1	6.2	-	8.0	-	ns

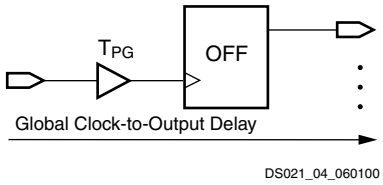
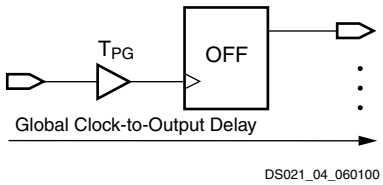
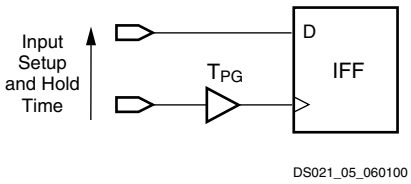
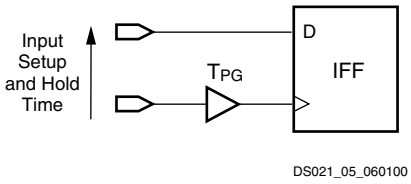
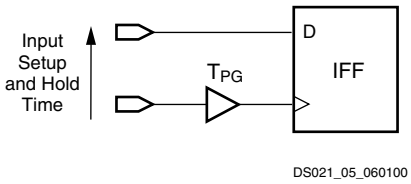
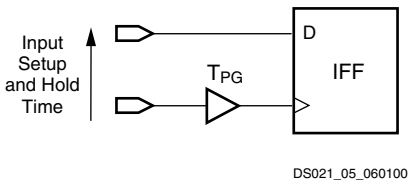
Notes:
1. Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

XQ4000E CLB Level-Sensitive RAM Timing Characteristics



XQ4000E Guaranteed Input and Output Parameters (Pin-to-Pin, TTL I/O)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XQ4000E devices unless otherwise noted.

Symbol	Description	Device	-3	-4	Units
T_{ICKOF} (Max)	Global clock to output (fast) using OFF 	XQ4005E	-	14.0	ns
		XQ4010E	10.9	16.0	ns
		XQ4013E	11.0	16.5	ns
		XQ4025E	-	17.0	ns
T_{ICKO} (Max)	Global clock to output (slew-limited) using OFF 	XQ4005E	-	18.0	ns
		XQ4010E	14.9	20.0	ns
		XQ4013E	15.0	20.5	ns
		XQ4025E	-	21.0	ns
T_{PSUF} (Min)	Input setup time, using IFF (no delay) 	XQ4005E	-	2.0	ns
		XQ4010E	0.2	1.0	ns
		XQ4013E	0	0.5	ns
		XQ4025E	-	0	ns
T_{PHF} (Min)	Input hold time, using IFF (no delay) 	XQ4005E	-	4.6	ns
		XQ4010E	5.5	6.0	ns
		XQ4013E	6.5	7.0	ns
		XQ4025E	-	8.0	ns
T_{PSU} (Min)	Input setup time, using IFF (with delay) 	XQ4005E	-	8.5	ns
		XQ4010E	7.0	8.5	ns
		XQ4013E	7.0	8.5	ns
		XQ4025E	-	9.5	ns
T_{PH} (Min)	Input hold time, using IFF (with delay) 	XQ4005E	-	0	ns
		XQ4010E	0	0	ns
		XQ4013E	0	0	ns
		XQ4025E	-	0	ns

Notes:
1. OFF = Output Flip-Flop
2. IFF = Input Flip-Flop or Latch

XQ4000E IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XQ4000E devices unless otherwise noted.

Symbol	Description	Device	-3		-4		Units
			Min	Max	Min	Max	
Propagation Delays (TTL Inputs)(1)							
T_{PID}	Pad to I1, I2	All devices	-	2.5	-	3.0	ns
T_{PLI}	Pad to I1, I2 via transparent input latch, no delay	All devices	-	3.6	-	4.8	ns
T_{PDLI}	Pad to I1, I2 via transparent FCL and input latch, with delay	XQ4005E	-	-	-	10.8	ns
		XQ4010E	-	10.8	-	11.0	ns
		XQ4013E	-	11.2	-	11.4	ns
		XQ4025E	-	-	-	13.8	ns
Propagation Delays (CMOS Inputs)(1)							
T_{PIDC}	Pad to I1, I2	All devices	-	4.1	-	5.5	ns
T_{PLIC}	Pad to I1, I2 via transparent input latch, no delay	All devices	-	8.8	-	6.8	ns
T_{PDLIC}	Pad to I1, I2 via transparent FCL and input latch, with delay	XQ4005E	-	-	-	16.5	ns
		XQ4010E	-	14.0	-	17.5	ns
		XQ4013E	-	14.4	-	18.0	ns
		XQ4025E	-	-	-	20.8	ns
Propagation Delays (TTL Inputs)							
T_{IKRI}	Clock (IK) to I1, I2 (flip-flop)	All devices	-	2.8	-	5.6	ns
T_{IKLI}	Clock (IK) to I1, I2 (latch enable, active Low)	All devices	-	4.0	-	6.2	ns
Hold Times(2)							
T_{IKPI}	Pad to clock (IK), no delay	All devices	0	-	0	-	ns
T_{IKPID}	Pad to clock (IK), with delay	All devices	0	-	0	-	ns
T_{IKEC}	Clock enable (EC) to clock (K), no delay	All devices	1.5	-	1.5	-	ns
T_{IKECD}	Clock enable (EC) to clock (K), with delay	All devices	0	-	0	-	ns

Notes:

1. Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.
2. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XQ4000E IOB Input Switching Characteristic Guidelines *(continued)*

Symbol	Description	Device	-3		-4		Units
			Min	Max	Min	Max	
Setup Times (TTL Inputs)(1,2)							
T_{PICK}	Pad to clock (IK), no delay	All devices	2.6	-	4.0	-	ns
T_{PICKD}	Pad to clock (IK), with delay	XQ4005E	-	-	10.9	-	ns
		XQ4010E	9.8	-	11.3	-	ns
		XQ4013E	10.2	-	11.8	-	ns
		XQ4025E	-	-	14.0	-	ns
Setup Times (CMOS Inputs)(1,2)							
T_{PICKC}	Pad to clock (IK), no delay	All devices	3.3	-	6.0	-	ns
T_{PICKDC}	Pad to clock (IK), with delay	XQ4005E	-	-	12.0	-	ns
		XQ4010E	10.5	-	13.0	-	ns
		XQ4013E	10.9	-	13.5	-	ns
		XQ4025E	-	-	16.0	-	ns
(TTL or CMOS)							
T_{ECIK}	Clock enable (EC) to clock (IK), no delay	All devices	2.5	-	3.5	-	ns
T_{ECIKD}	Clock enable (EC) to clock (IK), with delay	XQ4005E	-	-	10.4	-	ns
		XQ4010E	9.7	-	10.7	-	ns
		XQ4013E	10.1	-	11.1	-	ns
		XQ4025E	-	-	14.0	-	ns
Global Set/Reset(3)							
T_{RRI}	Delay from GSR net through Q to I1, I2	All devices	-	7.8	-	12.0	ns
T_{MRW}	GSR width	All devices	11.5	-	13.0	-	ns
T_{MRI}	GSR inactive to first active clock (IK) edge	All devices	11.5	-	13.0	-	ns

Notes:

1. Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.
2. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.
3. Timing is based on the XC4005E. For other devices see the XACT timing calculator.

XQ4000E IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values apply to all XQ4000E devices unless otherwise noted.

Symbol	Description	-3		-4		Units
		Min	Max	Min	Max	
Propagation Delays (TTL Output Levels)						
T_{OKPOF}	Clock (OK) to pad, fast	-	6.5	-	7.5	ns
T_{OKPOS}	Clock (OK) to pad, slew-rate limited	-	9.5	-	11.5	ns
T_{OPF}	Output (O) to pad, fast	-	5.5	-	8.0	ns
T_{OPS}	Output (O) to pad, slew-rate limited	-	8.6	-	12.0	ns
T_{TSHZ}	3-state to pad High-Z, slew-rate independent	-	4.2	-	10.0	ns
T_{TSONF}	3-state to pad active and valid, fast	-	8.1	-	10.0	ns
T_{TSONS}	3-state to pad active and valid, slew-rate limited	-	11.1	-	13.7	ns
Propagation Delays (CMOS Output Levels)						
T_{OKPOFC}	Clock (OK) to pad, fast	-	7.8	-	9.5	ns
T_{OKPOSC}	Clock (OK) to pad, slew-rate limited	-	11.6	-	13.5	ns
T_{OPFC}	Output (O) to pad, fast	-	9.7	-	10.0	ns
T_{OPSC}	Output (O) to pad, slew-rate limited	-	13.4	-	14.0	ns
T_{TSHZC}	3-state to pad High-Z, slew-rate independent	-	4.3	-	5.2	ns
T_{TSONFC}	3-state to pad active and valid, fast	-	7.6	-	9.1	ns
T_{TSONSC}	3-state to pad active and valid, slew-rate limited	-	11.4	-	13.1	ns
Setup and Hold Times						
T_{OOK}	Output (O) to clock (OK) setup time	4.6	-	5.0	-	ns
T_{OKO}	Output (O) to clock (OK) hold time	0	-	0	-	ns
T_{ECOK}	Clock enable (EC) to clock (OK) setup	3.5	-	4.8	-	ns
T_{OKEC}	Clock enable (EC) to clock (OK) hold	1.2	-	1.2	-	ns
Clock						
T_{CH}	Clock High	4.0	-	4.5	-	ns
T_{CL}	Clock Low	4.0	-	4.5	-	ns
Global Set/Reset(3)						
T_{RRO}	Delay from GSR net to pad	-	11.8	-	15.0	ns
T_{MRW}	GSR width	11.5	-	13.0	-	ns
T_{MRO}	GSR inactive to first active clock (OK) edge	11.5	-	13.0	-	ns

Notes:

1. Output timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the "Additional XC4000 Data" section on the Xilinx web site, **www.xilinx.com/partinfo/databook.htm**.
2. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.
3. Timing is based on the XC4005E. For other devices see the XACT timing calculator.

XC4000E Boundary Scan (JTAG) Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF-S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

		-3		-4		
Symbol	**Description**	**Min**	**Max**	**Min**	**Max**	**Units**
Setup Times						
T_{TDITCK}	Input (TDI) to clock (TCK)	30.0		30.0		ns
T_{TMSTCK}	Input (TMS) to clock (TCK)	15.0		15.0		ns
Hold Times						
T_{TCKTDI}	Input (TDI) to clock (TCK)	0		0		ns
T_{TCKTMS}	Input (TMS) to clock (TCK)	0		0		ns
Propagation Delay						
T_{TCKPO}	Clock (TCK) to pad (TDO)		30.0		30.0	ns
Clock						
T_{TCKH}	Clock (TCK) High	5.0		5.0		ns
T_{TCKL}	Clock (TCK) Low	5.0		5.0		ns
F_{MAX}	Frequency		15.0		15.0	MHz

Notes:

1. Input setup and hold times and clock-to-pad times are specified with respect to external signal pins.
2. Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the “Additional XC4000 Data” section of the Programmable Logic Data Book.
3. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XQ4028EX Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Except for pin-to-pin input and output parameters, the A.C. parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions.

All specifications subject to change without notice.

XQ4028EX Absolute Maximum Ratings(1)

Symbol	Description			Units
V_{CC}	Supply voltage relative to GND		–0.5 to +7.0	V
V_{IN}	Input voltage relative to GND(2)		–0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to High-Z output(2)		–0.5 to V_{CC} + 0.5	V
V_{CCt}	Longest supply voltage rise time from 1V to 4V		50	ms
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic package	+150	°C
		Plastic package	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. Maximum DC excursion above V_{CC} or below Ground must be limited to either 0.5V or 10 mA, whichever is easier to achieve. Maximum total combined current on all dedicated inputs and Tri-state outputs must not exceed 200 mA. During transitions, the device pins may undershoot to –2.0V or overshoot toV_{CC} +2.0V, provided this over or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

XQ4028EX Recommended Operating Conditions(1)

Symbol	Descriptiont		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = –55°C to +125°C	Plastic	4.5	5.5	V
	Supply voltage relative to GND, T_C = –55°C to +125°C	Ceramic	4.5	5.5	V
V_{IH}	High-level input voltage(2)	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time		-	250	ns

Notes:
1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Input and output measurement threshold are 1.5V for TTL and 2.5V for CMOS.

XQ4028EX DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage at I_{OH} = –4 mA, V_{CC} min	TTL outputs	2.4	-	V
	High-level output voltage at I_{OH} = –1 mA	CMOS outputs	V_{CC} – 0.5	-	V
V_{OL}	Low-level output voltage at I_{OL} = 12 mA, V_{CC} min(1)	TTL outputs	-	0.4	V
		CMOS outputs	-	0.4	V
V_{DR}	Data retention supply voltage (below which configuration data may be lost)		3.0	-	V
I_{CCO}	Quiescent FPGA supply current(2)		-	25	mA
I_L	Input or output leakage current		–10	10	µA
C_{IN}	Input capacitance (sample tested)	Plastic packages	-	10	V
		Ceramic packages	-	16	V
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 5.5V (sample tested)		0.02	0.25	mA
I_{RLL}	Horizontal longline pull-up (when selected) at logic Low(3)		0.3	2.0	mA

Notes:
1. With up to 64 pins simultaneously sinking 12 mA.
2. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND.

XQ4028EX Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature)

Global Buffer Switching Characteristics.

Symbol	Description	-4 Max	Units
T_{GLS}	From pad through Global Low Skew buffer, to any clock K	9.2	ns
T_{GE}	From pad through Global Early buffer, to any clock K in same quadrant	5.7	ns

XQ4028EX Horizontal Longline Switching Characteristic Guidelines

Symbol	Description	-4 Max	Units
TBUF Driving a Horizontal Longline			
T_{IO1}	I going High or Low to horizontal longline going High or Low, while T is Low. Buffer is constantly active.	13.7	ns
T_{ON}	T going Low to horizontal longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.	14.7	ns
TBUF Driving Half a Horizontal Longline			
T_{HIO1}	I going High or Low to half of a horizontal longline going High or Low, while T is Low. Buffer is constantly active.	6.3	ns
T_{HON}	T going Low to half of a horizontal longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.	7.2	ns

Notes:

1. These values include a minimum load of one output, spaced as far as possible from the activated pull-up(s). Use the static timing analyzer to determine the delay for each destination.

XQ4028EX CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000EX devices unless otherwise noted.

CLB Switching Characteristics

Symbol	Description	-4		Units
		Min	Max	
Combinatorial Delays				
T_{ILO}	F/G inputs to X/Y outputs	-	2.2	ns
T_{IHO}	F/G inputs via H' to X/Y outputs	-	3.8	ns
T_{ITO}	F/G inputs via transparent latch to Q outputs	-	3.2	ns
T_{HH0O}	C inputs via SR/H0 via H to X/Y outputs	-	3.6	ns
T_{HH1O}	C inputs via H1 via H to X/Y outputs	-	3.0	ns
T_{HH2O}	C inputs via DIN/H2 via H to X/Y outputs	-	3.6	ns
T_{CBYP}	C inputs via EC, DIN/H2 to YQ, XQ output (bypass)	-	2.0	ns
CLB Fast Carry Logic				
T_{OPCY}	Operand inputs (F1, F2, G1, G4) to C_{OUT}	-	2.5	ns
T_{ASCY}	Add/Subtract input (F3) to C_{OUT}	-	4.1	ns
T_{INCY}	Initialization inputs (F1, F3) to C_{OUT}	-	1.9	ns
T_{SUM}	C_{IN} through function generators to X/Y outputs	-	3.0	ns
T_{BYP}	C_{IN} to C_{OUT}, bypass function generators	-	0.60	ns
T_{NET}	Carry net selay, C_{OUT} to C_{IN}	-	0.18	ns
Sequential Delays				
T_{CKO}	Clock K to flip-flop outputs Q	-	2.2	ns
T_{CKLO}	Clock K to latch outputs Q	-	2.2	ns
Setup Time before Clock K				
T_{ICK}	F/G inputs	1.3	-	ns
T_{IHCK}	F/G inputs via H	3.0	-	ns
T_{HH0CK}	C inputs via H0 through H	2.8	-	ns
T_{HH1CK}	C inputs via H1 through H	2.2	-	ns
T_{HH2CK}	C inputs via H2 through H	2.8	-	ns
T_{DICK}	C inputs via DIN	1.2	-	ns
T_{ECCK}	C inputs via EC	1.2	-	ns
T_{RCK}	C inputs via S/R, going Low (inactive)	0.8	-	ns
T_{CCK}	CIN input via F/G	2.2	-	ns
T_{CHCK}	CIN input via F/G and H	3.9	-	ns
Hold Time after Clock K				
T_{CKI}	F/G inputs	0	-	ns

CLB Switching Characteristics *(Continued)*

Symbol	Description	-4		Units
		Min	Max	
T_{CKIH}	F/G inputs via H	0	-	ns
T_{CKHH0}	C inputs via SR/H0 through H	0	-	ns
T_{CKHH1}	C inputs via H1 through H	0	-	ns
T_{CKHH2}	C inputs via DIN/H2 through H	0	-	ns
T_{CKDI}	C inputs via DIN/H2	0	-	ns
T_{CKEC}	C inputs via EC	0	-	ns
T_{CKR}	C inputs via SR, going Low (inactive)	0	-	ns
Clock				
T_{CH}	Clock High time	3.5	-	ns
T_{CL}	Clock Low time	3.5	-	ns
Set/Reset Direct				
T_{RPW}	Width (High)	3.5	-	ns
T_{RIO}	Delay from C inputs via S/R, going High to Q	-	4.5	ns
Global Set/Reset				
T_{MRW}	Minimum GSR pulse width	-	13.0	ns
T_{MRQ}	Delay from GSR input to any Q	-	22.8	
F_{TOG}	Toggle frequency (MHz) (for export control)	-	143	MHz

XQ4028EX CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000EX devices unless otherwise noted.

Symbol	Single Port RAM	Size	-4		Units
			Min	Max	
Write Operation					
T_{WCS}	Address write cycle time (clock K period)	16x2	11.0	-	ns
T_{WCTS}		32x1	11.0	-	ns
T_{WPS}	Clock K pulse width (active edge)	16x2	5.5	-	ns
T_{WPTS}		32x1	5.5	-	ns
T_{ASS}	Address setup time before clock K	16x2	2.7	-	ns
T_{ASTS}		32x1	2.6	-	ns
T_{AHS}	Address hold time after clock K	16x2	0	-	ns
T_{AHTS}		32x1	0	-	ns
T_{DSS}	DIN setup time before clock K	16x2	2.4	-	ns
T_{DSTS}		32x1	2.9	-	ns
T_{DHS}	DIN hold time after clock K	16x2	0	-	ns
T_{DHTS}		32x1	0	-	ns
T_{WSS}	WE setup time before clock K	16x2	2.3	-	ns
T_{WSTS}		32x1	2.1	-	ns
T_{WHS}	WE hold time after clock K	16x2	0	-	ns
T_{WHTS}		32x1	0	-	ns
T_{WOS}	Data valid after clock K	16x2	-	8.2	ns
T_{WOTS}		32x1	-	10.1	ns

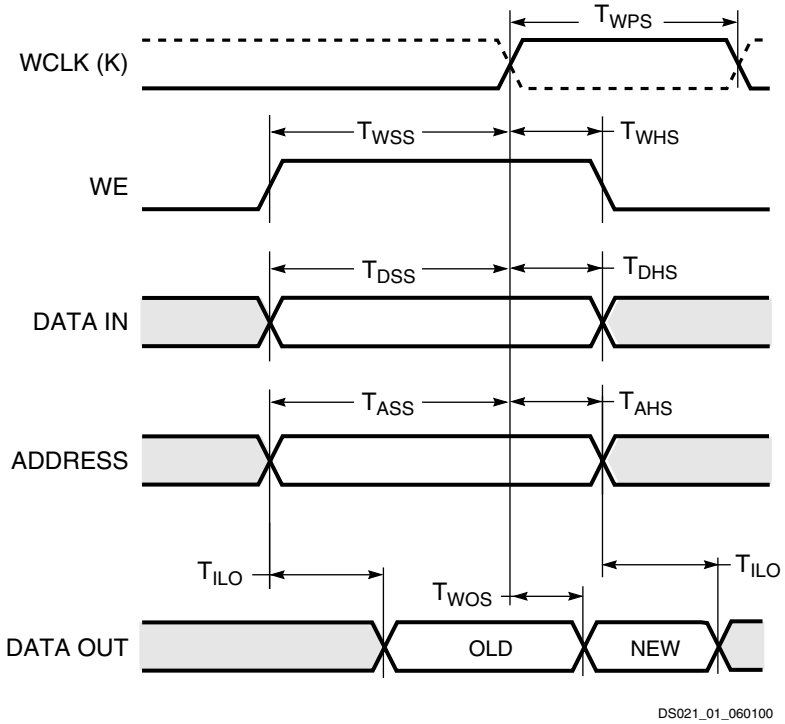
Notes:
1. Applicable Read timing specifications are identical to Level-Sensitive Read timing.

Dual-Port RAM Synchronous (Edge-Triggered) Write Operation Characteristics

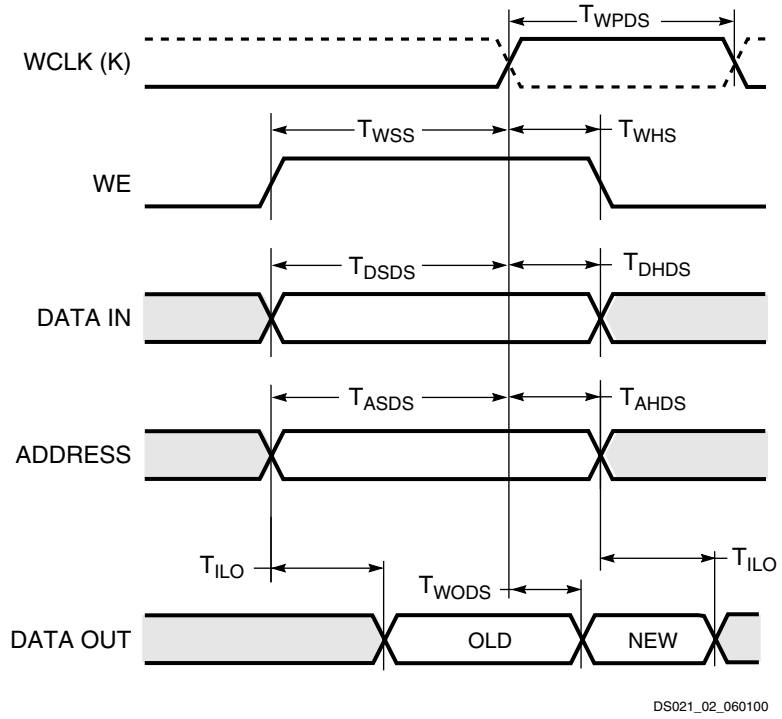
Symbol	Dual Port RAM	Size[1]	-4		Units
			Min	Max	
Write Operation					
T_{WCDS}	Address write cycle time (clock K period)	16x1	11.0		ns
T_{WPDS}	Clock K pulse width (active edge)	16x1	5.5	-	ns
T_{ASDS}	Address setup time before clock K	16x1	3.1	-	ns
T_{AHDS}	Address hold time after clock K	16x1	0	-	ns
T_{DSDS}	DIN setup time before clock K	16x1	2.9	-	ns
T_{DHDS}	DIN hold time after clock K	16x1	0	-	ns
T_{WSDS}	WE setup time before clock K	16x1	2.1	-	ns
T_{WHDS}	WE hold time after clock K	16x1	0	-	ns
T_{WODS}	Data valid after clock K	16x1	-	9.4	ns

Notes:
1. Timing for the 16x1 RAM option is identical to 16x2 RAM timing.
2. Applicable Read timing specifications are identical to Level-Sensitive Read timing.

XQ4028EX CLB RAM Synchronous (Edge-Triggered) Write Timing Waveform



XQ4028EX CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing Waveform



XQ4028EX CLB RAM Asynchronous (Level-Sensitive) Write and Read Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000EX devices unless otherwise noted.

Symbol	Single Port RAM	Size	-4		Units
			Min	Max	
Write Operation					
T_{WC}	Address write cycle time	16x2	10.6	-	ns
T_{WCT}		32x1	10.6	-	ns
T_{WP}	Write Enable pulse width (High)	16x2	5.3	-	ns
T_{WPT}		32x1	5.3	-	ns
T_{AS}	Address setup time before WE	16x2	2.8	-	ns
T_{AST}		32x1	2.8	-	ns
T_{AH}	Address hold time after end of WE	16x2	1.7	-	ns
T_{AHT}		32x1	1.7	-	ns
T_{DS}	DIN setup time before end of WE	16x2	1.1	-	ns
T_{DST}		32x1	1.1	-	ns
T_{DH}	DIN hold time after end of WE	16x2	6.6	-	ns
T_{DHT}		32x1	6.6	-	ns
Read Operation					
T_{RC}	Address read cycle time	16x2	4.5	-	ns
T_{RCT}		32x1	6.5	-	ns
T_{ILO}	Data valid after address change (no Write Enable)	16x2	-	2.2	ns
T_{IHO}		32x1	-	3.8	ns
Read Operation, Clocking Data into Flip-Flop					
T_{ICK}	Address setup time before clock K	16x2	1.5	-	ns
T_{IHCK}		32x1	3.2	-	ns
Read During Write					
T_{WO}	Data valid after WE goes active (DIN stable before WE)	16x2	-	6.5	ns
T_{WOT}		32x1	-	7.4	ns
T_{DO}	Data valid after DIN (DIN changes during WE)	16x2	-	7.7	ns
T_{DOT}		32x1	-	8.2	ns
Read During Write, Clocking Data into Flip-Flop					
T_{WCK}	WE setup time before clock K	16x2	7.1	-	ns
T_{WCKT}		32x1	9.2	-	ns
T_{DCK}	Data setup time before clock K	16x2	5.9	-	ns
T_{DOCK}		32x1	8.4	-	ns

Notes:
1. Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

XQ4028EX CLB Level-Sensitive RAM Timing Waveforms

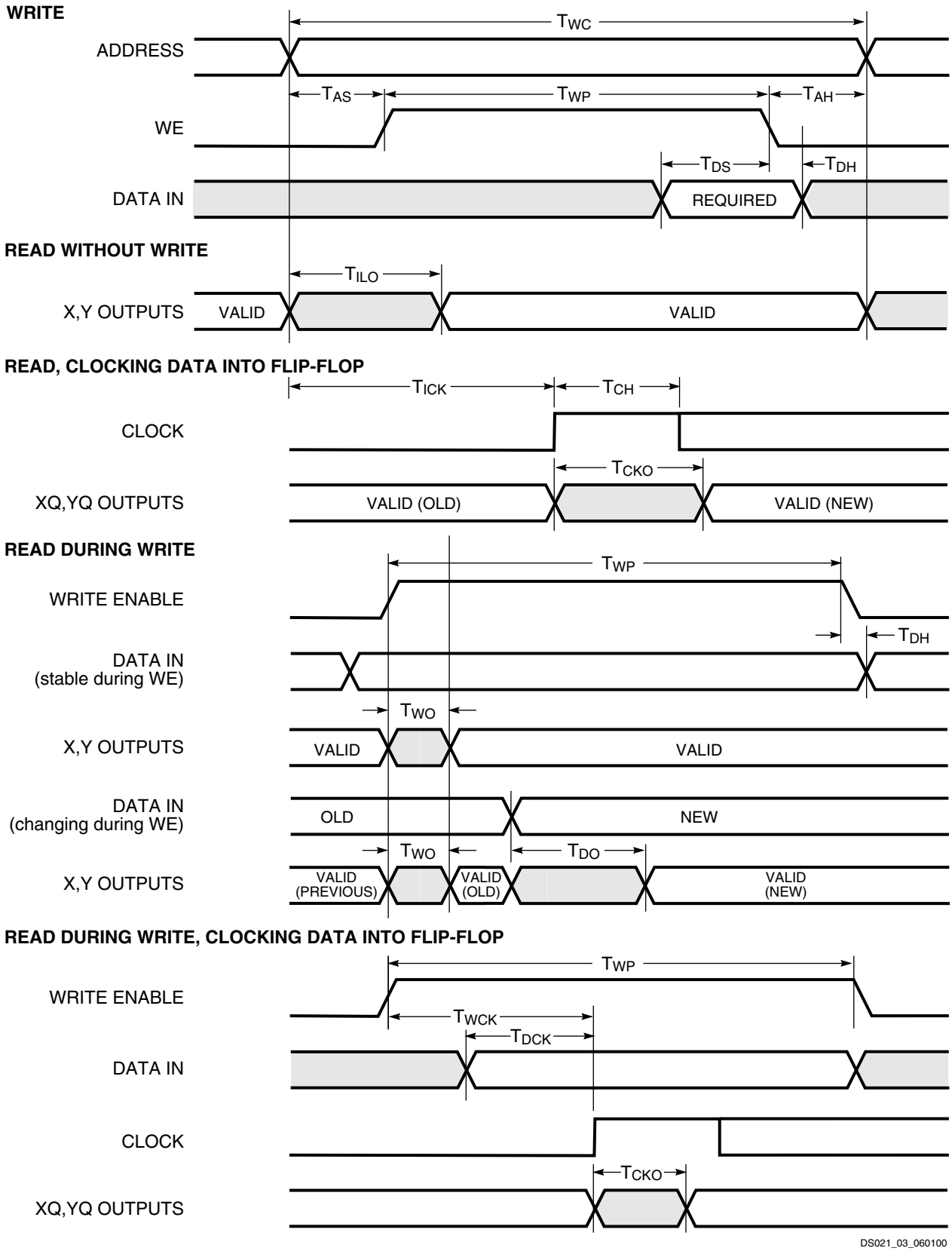


Figure 1:

XQ4028EX Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XQ4000EX devices unless otherwise noted.

XQ4028EX Output Flip-Flop, Clock to Out(1,2)

Symbol	Description	-4 Max	Units
T_{ICKOF}	Global low skew clock to output using OFF(3)	16.6	ns
T_{ICKEOF}	Global early clock to output using OFF(3)	13.1	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at TTL threshold with 50 pF external capacitive load.
3. OFF = Output Flip-Flop

XQ4028EX Output Mux, Clock to Out(1,2)

Symbol	Description	-4 Max	Units
T_{PFPF}	Global low skew clock to TTL output (fast) using OMUX3)	15.9	ns
T_{PEFPF}	Global early clock to TTL output (fast) using OMUXF(3)	12.4	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see graph below.
3. OMUX = Output MUX

XQ4028EX Output Level and Slew Rate Adjustments

The following table must be used to adjust output parameters and output switching characteristics.

Symbol	Description	-4 Max	Units
T_{TTLOF}	For TTL output FAST add	0	ns
T_{TTLO}	For TTL output SLOW add	2.9	ns
T_{CMOSOF}	For CMOS FAST output add	1.0	ns
T_{CMOSO}	For CMOS SLOW output add	3.6	ns

XQ4028EX Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XQ4000EX devices unless otherwise noted

XQ4028EX Global Low Skew Clock, Setup and Hold

Symbol	Description	-4 Min	Units
T_{PSD}	Input setup time, using Global Low Skew clock and IFF (full delay)	8.0	ns
T_{PHD}	Input hold time, using Global Low Skew clock and IFF (full delay)	0	ns

Notes:
1. IFF = Flip-Flop or Latch

XQ4028EX Global Early Clock, Setup and Hold for IFF

Symbol	Description	-4 Min(2)	Units
T_{PSEP}	Input setup time, using Global Early clock and IFF (full delay)	6.5	ns
T_{PHEP}	Input hold time, using Global Early clock and IFF (full delay)	0	ns

Notes:
1. IFF = Flip-Flop or Latch
2. Setup parameters are for BUFGE #s 3, 4, 7 and 8. Add 1.6 ns for BUFGE #s 1, 2, 5 and 6.

XQ4028EX Global Early Clock, Setup and Hold for FCL

Symbol	Description	-4 Min(2)	Units
T_{PFSEP}	Input setup time, using Global Early clock and FCL (partial delay)	3.4	ns
T_{PFHEP}	Input hold time, using Global Early clock and FCL (partial delay)	0	ns

Notes:
1. FCL = Fast Capture Latch
2. For CMOS input levels, see the XQ4028EX Input Threshold Adjustments.
3. Setup time is measured with the fastest route and the lightest load. Use the static timing analyzer to determine the setup time under given design conditions.
4. Hold time is measured using the farthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer to determine the setup and hold times under given design conditions.
5. Setup parameters are for BUFGE #s 3, 4, 7 and 8. Add 1.2 ns for BUFGE #s 1, 2, 5 and 6.

XQ4028EX Input Threshold Adjustments

The following table must be used to adjust input parameters and input switching characteristics.

Symbol	Description	-4 Max	Units
T_{TTLI}	For TTL input add	0	ns
T_{CMOSI}	For CMOS input add	0.3	ns

XQ4028EX IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000EX devices unless otherwise noted.

Symbol	Description	-4 Min	Units
Clocks			
T_{OKIK}	Delay from FCL enable (OK) active to IFF clock (IK) active edge	3.2	ns
Propagation Delays			
T_{PID}	Pad to I1, I2	2.2	ns
T_{PLI}	Pad to I1, I2 via transparent input latch, no delay	3.8	ns
T_{PPLI}	Pad to I1, I2 via transparent input latch, partial delay	13.3	ns
T_{PDLI}	Pad to I1, I2 via transparent input latch, full delay	18.2	ns
T_{PFLI}	Pad to I1, I2 via transparent FCL and input latch, no delay	5.3	ns
T_{PPFLI}	Pad to I1, I2 via transparent FCL and input latch, partial delay	13.6	ns
Propagation Delays (TTL Inputs)			
T_{IKRI}	Clock (IK) to I1, I2 (flip-flop)	3.0	ns
T_{IKLI}	Clock (IK) to I1, I2 (latch enable, active Low)	3.2	ns
T_{OKLI}	FCL enable (OK) active edge to I1, I2 (via transparent standard input latch)	6.2	ns
Global Set/Reset			
T_{MRW}	Minimum GSR pulse width	13.0	ns
T_{RRI}	Delay from GSR input to any Q	22.8	ns

Notes:
1. FCL = Fast Capture Latch, IFF = Input Flip-Flop or Latch
2. For CMOS input levels, see the "XQ4028EX Input Threshold Adjustments" on page 70.
3. For setup and hold times with respect to the clock input pin, see the Global Low Skew Clock and Global Early Clock Setup and Hold tables on page 70.

XQ4028EX IOB Input Switching Characteristic Guidelines (Continued)

Symbol	Description	-4 Min	Units
Setup Times			
T_{PICK}	Pad to Clock (IK), no delay	2.5	ns
T_{PICKP}	Pad to Clock (IK), partial delay	10.8	ns
T_{PICKD}	Pad to Clock (IK), full delay	15.7	ns
T_{PICKF}	Pad to Clock (IK), via transparent Fast Capture Latch, no delay	3.9	ns
T_{PICKFP}	Pad to Clock (IK), via transparent Fast Capture Latch, partial delay	12.3	ns
T_{POCK}	Pad to Fast Capture Latch Enable (OK), no delay	0.8	ns
T_{POCKP}	Pad to Fast Capture Latch Enable (OK), partial delay	9.1	ns
Setup Times (TTL or CMOS Inputs)			
T_{ECIK}	Clock Enable (EC) to Clock (IK)	0.3	ns
Hold Times			
T_{IKPI}	Pad to Clock (IK), no delay	0	ns
T_{IKPIP}	Pad to Clock (IK), partial delay	0	ns
T_{IKPID}	Pad to Clock (IK), full delay	0	ns
T_{IKPIF}	Pad to Clock (IK) via transparent Fast Capture Latch, no delay	0	ns
T_{IKFPIP}	Pad to Clock (IK) via transparent Fast Capture Latch, partial delay	0	ns
T_{IKFPID}	Pad to Clock (IK) via transparent Fast Capture Latch, full delay	0	ns
T_{IKEC}	Clock Enable (EC) to Clock (IK), no delay	0	ns
T_{IKECP}	Clock Enable (EC) to Clock (IK), partial delay	0	ns
T_{IKECD}	Clock Enable (EC) to Clock (IK), full delay	0	ns
T_{OKPI}	Pad to Fast Capture Latch Enable (OK), no delay	0	ns
T_{OKPIP}	Pad to Fast Capture Latch Enable (OK), partial delay	0	ns

Notes:
1. For CMOS input levels, see the "XQ4028EX Input Threshold Adjustments" on page 70.
2. For setup and hold times with respect to the clock input pin, see the Global Low Skew Clock and Global Early Clock Setup and Hold tables on page 70.

FXQ4028EX IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values apply to all XQ4000EX devices unless otherwise noted.

Symbol	Description	-4		Units
		Min	Max	
Propagation Delays (TTL Output Levels)				
T_{OKPOF}	Clock (OK) to pad, fast	-	7.4	ns
T_{OPF}	Output (O) to pad, fast	-	6.2	ns
T_{TSHZ}	3-state to pad High-Z, slew-rate independent	-	4.9	ns
T_{TSONF}	3-state to pad active and valid, fast	-	6.2	ns
T_{OKFPF}	Output MUX select (OK) to pad	-	6.7	ns
T_{CEFPF}	Fast path output MUX input (EC) to pad	-	6.2	
T_{OFPF}	Slowest path output MUX input (EC) to pad	-	7.3	
Setup and Hold Times				
T_{OOK}	Output (O) to clock (OK) setup time	0.6	-	ns
T_{OKO}	Output (O) to clock (OK) hold time	0	-	ns
T_{ECOK}	Clock enable (EC) to clock (OK) setup	0	-	ns
T_{OKEC}	Clock enable (EC) to clock (OK) hold	0	-	ns
Clocks				
T_{CH}	Clock High	3.5	-	ns
T_{CL}	Clock Low	3.5	-	ns
Global Set/Reset				
T_{MRW}	Minimum GSR pulse width	13.0	-	ns
T_{RRI}	Delay from GSR input to any pad	30.2	-	ns

Notes:
1. Output timing is measured at TTL threshold, with 35 pF external capacitive loads.
2. For CMOS output levels, see the "XQ4028EX Output Level and Slew Rate Adjustments" on page 69.

CB191/196 Package for XQ4010E

Pin Description	PG191	CB196	Bound Scan
GND	D4	P1	-
PGCK1_(A16*I/0)	C3	P2	122
I/O_(A17)	C4	P3	125
I/0	B3	P4	128
-	-	P5(1)	-
I/O	C5	P6	131
I/O_(TDI)	A2	P7	134
I/O_(TCK)	B4	P8	137
I/O	C6	P9	140
I/O	A3	P10	143
I/O	B5	P11	146
I/O	B6	P12	149
GND	C7	P13	-
I/O	A4	P14	152
I/O	A5	P15	155
I/O_(TMS)	B7	P16	158
I/O	A6	P17	161
I/O	C8	P18	164
I/O	A7	P19	167
I/O	B8	P20	170
I/O	A8	P21	173
I/O	B9	P22	176
I/O	C9	P23	179
GND	D9	P24	-
VCC	D10	P25	-
I/O	C10	P26	182
I/O	B10	P27	185
I/O	A9	P28	-
I/O	A10	P29	191
I/O	A11	P30	194
I/O	C11	P31	197
I/O	B11	P32	200
I/O	A12	P33	203
I/O	B12	P34	206
I/O	A13	P35	209
GND	C12	P36	-
I/O	B13	P37	212
I/O	A14	P38	215
I/O	A15	P39	218
I/O	C13	P40	221
I/O	B14	P41	224
I/O	A16	P42	227
I/O	B15	P43	230
I/O	C14	P44	233
I/O	A17	P45	236
SCGK2_(I/O)	B16	P46	239
M1	C15	P47	242
GND	D15	P48	-
M0	A18	P49	245(2)
VCC	D16	P50	-
M2	C16	P51	246(2)
PGCK2_(I/O)	B17	P52	247
I/O_(HDC)	E16	P53	250
-	-	P54(1)	-
I/O	C17	P55	253
I/0	D17	P56	256
I/O	B18	P57	259
I/O_(LDC)	E17	P58	262
I/O	F16	P59	265
I/O	C18	P60	268
I/O	D18	P61	271
I/O	F17	P62	274
GND	G16	P63	-
I/O	E18	P64	277
I/O	F18	P65	280
I/O	G17	P66	283
I/O	G18	P67	286

Notes:
1. Indicates unconnected package pins.
2. Contributes only one bit (.I) to the boundary scan register.
   Boundary Scan Bit 0 = TD0.T
   Boundary Scan Bit 1 = TD0.0
   Boundary Scan Bit 487 = BSCAN.UPD

Notes:
1. Indicates unconnected package pins.
2. Contributes only one bit (.I) to the boundary scan register.
   Boundary Scan Bit 0 = TD0.T
   Boundary Scan Bit 1 = TD0.0
   Boundary Scan Bit 487 = BSCAN.UPD

Pin Description	PG191	CB196	Bound Scan
I/O	H16	P68	286
I/O	H17	P69	291
I/O	H18	P70	295
I/O	J18	P71	298
I/O	J17	P72	301
I/O_(/ERR_/INIT)	J16	P73	304
VCC	J15	P74	-
GND	K15	P75	-
I/O	K16	P76	307
I/O	K17	P77	310
I/O	K18	P78	313
I/O	L18	P79	316
I/O	L17	P80	319
I/O	L16	P81	322
I/O	M18	P82	325
I/O	M17	P83	328
I/O	N18	P84	331
I/O	P18	P85	334
GND	M16	P86	-
I/O	N17	P87	337
I/O	R18	P88	340
I/O	T18	P89	343
I/O	P17	P90	349
I/O	N16	P91	349
I/O	T17	P92	352
I/O	R17	P93	355
I/O	P16	P94	358
I/O	U18	P95	361
SGCK3_(I/O)	T16	P96	364
GND	R16	P97	-
DONE	U17	P98	-
VCC	R15	P99	-
/PROG	V18	P100	-
I/O_(D7)	T15	P101	367

Notes:
1. Indicates unconnected package pins.
2. Contributes only one bit (.I) to the boundary scan register.
   Boundary Scan Bit 0 = TD0.T
   Boundary Scan Bit 1 = TD0.0
   Boundary Scan Bit 487 = BSCAN.UPD

Pin Description	PG191	CB196	Bound Scan
PGCK3_(I/O)	U16	P102	370
-	-	P103(1)	-
I/O	T14	P104	376
I/O	U15	P105	376
I/O_(D6)	V17	P106	379
I/O	V16	P107	382
I/O	T13	P108	385
I/O	U14	P109	388
I/O	V15	P110	391
I/O	V14	P111	394
GND	T12	P112	-
I/O	U13	P113	397
I/O	V13	P114	400
I/O_(D5)	U12	P115	403
I/O_(/CSO)	V12	P116	406
I/O	T11	P117	409
I/O	U11	P118	412
I/O	V11	P119	415
I/O	V1	P120	418
I/O_(D4)	U10	P121	421
I/O	T10	P122	424
VCC	R10	P123	-
GND	R9	P124	-
I/O_(D3)	T9	P125	427
I/O_(/RS)	U9	P126	430
I/O	V9	P127	433
I/O	V8	P128	436
I/O	U8	P129	439
I/O	T8	P130	442
I/O_(D2)	V7	P131	445
I/O	U7	P132	448
I/O	V6	P133	451
I/O	U6	P134	454
GND	T7	P135	-

Notes:
1. Indicates unconnected package pins.
2. Contributes only one bit (.I) to the boundary scan register.
   Boundary Scan Bit 0 = TD0.T
   Boundary Scan Bit 1 = TD0.0
   Boundary Scan Bit 487 = BSCAN.UPD

Pin Description	PG191	CB196	Bound Scan
I/O	V5	P136	457
I/O	V4	P137	460
I/O	U5	P138	463
I/O	T6	T139	446
I/O_(D1)	V3	P140	469
I/O_(RCLK-/BUSY/RDY)	V2	P141	472
I/O	U4	P142	475
I/O	T5	P143	478
I/O_(D0*_DIN)	U3	P144	481
SGCK4_(DOUT*_I/O)	T4	P145	484
CCLK	V1	P146	-
VCC	R4	P147	-
TDO	U2	P148	-
GND	R3	P149	-
I/O_(A0*_WS)	T3	P150	2
PGCK4_(I/O*_A1)	U1	P151	5
-	-	P152(1)	-
I/O	P3	P153	8
I/O	R2	P154	11
I/O_(CS1*_A2)	T2	P155	14
I/O_(A3)	N3	P156	17
I/O	P2	P157	20
I/O	T1	P158	23
I/O	R1	P159	26
I/O	N2	P160	29
GND	M3	P161	-
I/O	P1	P162	32
I/O	N1	P163	35
I/O_(A4)	M2	P164	38
I/O_(A5)	M1	P165	41
I/O	L3	P166	44
I/O	L2	P167	47
I/O	L1	P168	50

Notes:
1. Indicates unconnected package pins.
2. Contributes only one bit (.I) to the boundary scan register.
   Boundary Scan Bit 0 = TD0.T
   Boundary Scan Bit 1 = TD0.0
   Boundary Scan Bit 487 = BSCAN.UPD

Pin Description	PG191	CB196	Bound Scan
I/O	K1	P169	53
I/O_(A6)	K2	P170	56
I/O_(A7)	K3	P171	59
GND	K4	P172	-
VCC	J4	P173	-
I/O_(A8)	J3	P174	62
I/O_(A9)	J2	P175	65
I/O	J1	P176	68
I/O	H1	P177	71
I/O	H2	P178	74
I/O	H3	P179	77
I/O_(A10)	G1	P180	80
I/O_(A11)	G2	P181	83
I/O	F1	P182	86
I/O	E1	P183	89
GND	G3	P184	-
I/O	F2	P185	92
I/O	D1	P186	96
I/O	C1	P187	98
I/O	E2	P188	101
I/O_(A12)	F3	P189	104
I/O_(A13	D2	P190	107
-	-	P192(1)	-
I/O	E3	P193	113
I/O_(A14)	C2	P194	116
SGCK1(A15*I/O)	B2	P195	119
VCC	D3	P196	-

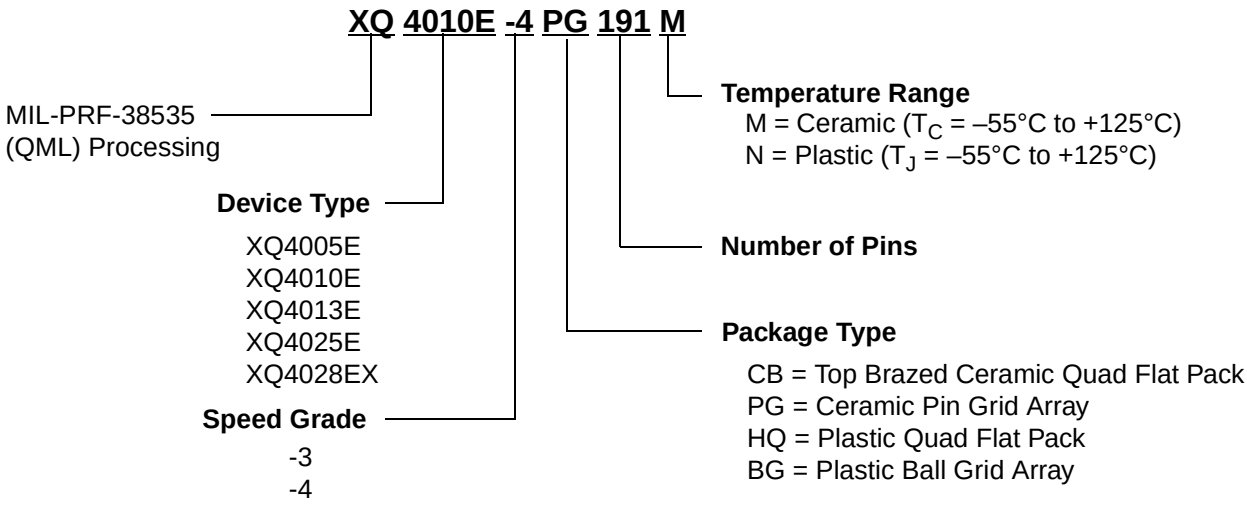
Notes:
1. Indicates unconnected package pins.
2. Contributes only one bit (.I) to the boundary scan register.
   Boundary Scan Bit 0 = TD0.T
   Boundary Scan Bit 1 = TD0.0
   Boundary Scan Bit 487 = BSCAN.UPD

Additional XQ4010E Package Pins

CB196

No Connect Pins			
P5	P54	P103	P152
P192	-	-	-

Ordering Information



2

Revision History

The following table shows the revision history for this document

Date	Version	Description
05/19/98	2.1	Updates.
06/25/00	2.2	Updated timing specifications to match with commercial data sheet. Updated format.

QPRO XQ4000XL Series QML High-Reliability FPGAs

DS029 (v1.3) June 25, 2000

Product Specification

XQ4000X Series Features

- Certified to MIL-PRF-38535 Appendix A QML (Qualified Manufacturer Listing)
- Ceramic and plastic packages
- Also available under the following standard microcircuit drawings (SMD)
  - XQ4013XL 5962-98513
  - XQ4036XL 5962-98510
  - XQ4062XL 5962-98511
  - XQ4085XL 5962-99575
- For more information contact the Defense Supply Center Columbus (DSCC) http://www.dscc.dla.mis/v/va/smd/smdsrch.html
- Available in -3 speed
- System featured Field-Programmable Gate Arrays
  - SelectRAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - Eight global low-skew clock or signal distribution networks
- System performance beyond 50 MHz
- Flexible array architecture
- Low power segmented routing architecture
- Systems-oriented features
  - IEEE 1149.1-compatible boundary scan logic support
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12 mA sink current per XQ4000XL output
- Configured by loading binary file
  - Unlimited reprogrammability
- Readback capability
  - Program verification
  - Internal node observability
- Development system runs on most common computer platforms
  - Interfaces to popular design environments
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization
- Highest capacity—over 180,000 usable gates
- Additional routing over XQ4000E
  - Almost twice the routing capacity for high-density designs
- Buffered Interconnect for maximum speed
- New latch capability in configurable logic blocks
- Improved VersaRing™ I/O interconnect for better Fixed pinout flexibility
  - Virtually unlimited number of clock signals
- Optional multiplexer or 2-input function generator on device outputs
- 5V tolerant I/Os
- 0.35 µm SRAM process

Introduction

The QPRO™ XQ4000XL Series high-performance, high-capacity Field Programmable Gate Arrays (FPGAs) provide the benefits of custom CMOS VLSI, while avoiding the initial cost, long development cycle, and inherent risk of a conventional masked gate array.

The result of thirteen years of FPGA design experience and feedback from thousands of customers, these FPGAs combine architectural versatility, on-chip Select-RAM memory with edge-triggered and dual-port modes, increased speed, abundant routing resources, and new, sophisticated soft-ware to achieve fully automated implementation of complex, high-density, high-performance designs.

Refer to the complete Commercial XC4000XL Series Field Programmable Gate Arrays Data Sheet for more information on device architecture and timing, and the latest Xilinx databook for package pinouts other than the CB228 (included in this data sheet). (Pinouts for XQ4000XL device are identical to XC4000XL.)

Table 1: **XQ4000XL Series High Reliability Field Progammable Gate Arrays**

Device	Logic Cells	Max Logic Gates (No RAM)(1)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)(1)	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. User I/O	Packages
XQ4013XL	2432	13,000	18,432	10,000-30,000	24x24	576	1,536	192	PG223, CB228, PQ240, BG256
XQ4036XL	3078	36,000	41,472	22,000-65,000	36x36	1,296	3,168	288	PG411, CB228, HQ240, BG352
XQ4062XL	5472	62,000	73,728	40,000-130,000	48x48	2,304	5,376	384	PG475, CB228, HQ240, BG432
XQ4085XL	7448	85,000	100,352	55,000-180,000	56x56	3,136	7,168	448	PG475, CB228, HQ240, BG432

Notes:
1. Maximum values of typical gate range includes 20% to 30% of CLBs used as RAM.

XQ4000XL Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or devicefamilies. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Except for pin-to-pin input and output parameters, the a.c. parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions.

All specifications subject to change without notice.

Additional Specifications

Except for pin-to-pin input and output parameters, the a.c. parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. For design considerations requiring more detailed timing information, see the appropriate family AC supplements available on the Xilinx web site at:

http://www.xilinx.com/partinfo/databook.htm.

Absolute Maximum Ratings(1)

Symbol	Description			Units
V_{CC}	Supply voltage relative to GND		–0.5 to 4.0	V
V_{IN}	Input voltage relative to GND(2)		–0.5 to 5.5	V
V_{TS}	Voltage applied to High-Z output(2)		–0.5 to 5.5	V
V_{CCt}	Longest supply voltage rise time from 1V to 3V		50	ms
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic package	+150	°C
		Plastic package	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. Maximum DC overshoot or undershoot above V_{CC} or below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0 V or overshoot to V_{CC} + 2.0V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Recommended Operating Conditions(1)

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = –55°C to +125°C	Plastic	3.0	3.6	V
	Supply voltage relative to GND, T_C = –55°C to +125°C	Ceramic	3.0	3.6	V
V_{IH}	High-level input voltage(2)		50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage		0	30% of V_{CC}	V
T_{IN}	Input signal transition time		-	250	ns

Notes:

1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Input and output measurement threshold is ~50% of V_{CC}.

XQ4000XL DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage at I_{OH} = –4 mA, V_{CC} min (LVTTL)		2.4	-	V
	High-level output voltage at I_{OH} = –500 µA, (LVCMOS)		90% V_{CC}	-	V
V_{OL}	Low-level output voltage at I_{OL} = 12 mA, V_{CC} min (LVTTL)(1)		-	0.4	V
	Low-level output voltage at I_{OL} = 1500 µA, (LVCMOS)		-	10% V_{CC}	V
V_{DR}	Data retention supply voltage (below which configuration data may be lost)		2.5	-	V
I_{CCO}	Quiescent FPGA supply current(2)		-	5	mA
I_L	Input or output leakage current		–10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, PQ, HQ, packages	-	10	pF
		PGA packages	-	16	pF
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 3.6V (sample tested)		0.02	0.15	mA
I_{RLL}	Horizontal longline pull-up (when selected) at logic Low		0.3	2.0	mA

Notes:
1. With up to 64 pins simultaneously sinking 12 mA.
2. With no output current loads, no active input or Longline pull-up resistors, all I/O pins in a High-Z state and floating.

Power-On Power Supply Requirements

Xilinx FPGAs require a minimum rated power supply current capacity to insure proper initialization, and the power supply ramp-up time does affect the current required. A fast ramp-up time requires more current than a slow ramp-up time. The slowest ramp-up time is 50 ms. Current capacity is not specified for a ramp-up time faster than 2 ms. The current capacity varies linealy with ramp-up time, *e.g.*, an XQ4036XL with a ramp-up time of 25 ms would require a capacity predicted by the point on the straight line drawn from 1A at 120 µs to 500 mA at 50 ms at the 25 ms time mark. This point is approximately 750 mA .

Product	Description	Ramp-up Time	
		Fast (120 µs)	Slow (50 ms)
XQ4013 - 36XL	Minimum required current supply	1A	500 mA
XC4062XL	Minimum required current supply	2A	500 mA
XC4085XL(1)	Minimum required current supply	2A(1)	500 mA

Notes:
1. The XC4085XL fast ramp-up time is 5 ms.
2. Devices are guaranteed to initialize properly with the minimum current listed above. A larger capacity power supply may result in a larger initialization current.
3. This specification applies to Commercial and Industrial grade products only.
4. Ramp-up Time is measured from $0V_{DC}$ to $3.6V_{DC}$. Peak current required lasts less than 3 ms, and occurs near the internal power on reset threshold voltage. After initialization and before configuration, I_{CC} max is less than 10 mA.

XQ4000XL AC Switching Characteristic

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature)

Global Buffer Switching Characteristics

Symbol	Description	Device	All Min	-3 Max	-1 Max	Units
T_{GLS}	Delay from pad through Global Low Skew buffer, to any clock K	XQ4013XL	0.6	3.6	-	ns
		XQ4036XL	1.1	4.8	-	ns
		XQ4062XL	1.4	6.3	-	ns
		XQ4085XL	1.6	-	5.7	ns

Global Early BUFGEs 1, 2, 5, and 6 to IOB Clock Characteristics

Symbol	Description	Device	All Min	-3 Max	-1 Max	Units
T_{GE}	Delay from pad through Global Early buffer, to any IOB clock. Values are for BUFGEs 1, 2, 5 and 6.	XQ4013XL	0.4	2.4	-	ns
		XQ4036XL	0.3	3.1	-	ns
		XQ4062XL	0.3	4.9	-	ns
		XQ4085XL	0.4	-	4.7	ns

Global Early BUFGEs 3, 4, 7, and 8 to IOB Clock Characteristics

Symbol	Description	Device	All Min	-3 Max	-1 Max	Units
T_{GE}	Delay from pad through Global Early buffer, to any IOB clock. Values are for BUFGEs 3, 4, 7 and 8.	XQ4013XL	0.7	2.4	-	ns
		XQ4036XL	0.9	4.7	-	ns
		XQ4062XL	1.2	5.9	-	ns
		XQ4085XL	1.3	-	5.5	ns

XQ4000XL CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000XL devices and expressed in nanoseconds unless otherwise noted.

CLB Switching Characteristics

Symbol	Description	-3		-1		Units
		Min	Max	Min	Max	
Combinatorial Delays						
T_{ILO}	F/G inputs to X/Y outputs	-	1.6	-	1.3	ns
T_{IHO}	F/G inputs via H' to X/Y outputs	-	2.7	-	2.2	ns
T_{ITO}	F/G inputs via transparent latch to Q outputs	-	2.9	-	2.2	ns
T_{HH0O}	C inputs via SR/H0 via H to X/Y outputs	-	2.5	-	2.0	ns
T_{HH1O}	C inputs via H1 via H to X/Y outputs	-	2.4	-	1.9	ns
T_{HH2O}	C inputs via D_{IN}/H2 via H to X/Y outputs	-	2.5	-	2.0	ns
T_{CBYP}	C inputs via EC, D_{IN}/H2 to YQ, XQ output (bypass)	-	1.5	-	1.1	ns
CLB Fast Carry Logic						
T_{OPCY}	Operand inputs (F1, F2, G1, G4) to C_{OUT}	-	2.7	-	2.0	ns
T_{ASCY}	Add/subtract input (F3) to C_{OUT}	-	3.3	-	2.5	ns
T_{INCY}	Initialization inputs (F1, F3) to C_{OUT}	-	2.0	-	1.5	ns
T_{SUM}	C_{IN} through function generators to X/Y outputs	-	2.8	-	2.4	ns
T_{BYP}	C_{IN} to C_{OUT}, bypass function generators	-	0.26	-	0.20	ns
T_{NET}	Carry net delay, C_{OUT} to C_{IN}	-	0.32	-	0.25	ns
Sequential Delays						
T_{CKO}	Clock K to flip-flop outputs Q	-	2.1	-	1.6	ns
T_{CKLO}	Clock K to latch outputs Q	-	2.1	-	1.6	ns
Setup Time Before Clock K						
T_{ICK}	F/G inputs	1.1	-	0.9	-	ns
T_{IHCK}	F/G inputs via H	2.2	-	1.7	-	ns
T_{HH0CK}	C inputs via H0 through H	2.0	-	1.6	-	ns
T_{HH1CK}	C inputs via H1 through H	1.9	-	1.4	-	ns
T_{HH2CK}	C inputs via H2 through H	2.0	-	1.6	-	ns
T_{DICK}	C inputs via D_{IN}	0.9	-	0.7	-	ns
T_{ECCK}	C inputs via EC	1.0	-	0.8	-	ns
T_{RCK}	C inputs via S/R, going Low (inactive)	0.6	-	0.5	-	ns
T_{CCK}	C_{IN} input via F/G	2.3	-	1.9	-	ns
T_{CHCK}	C_{IN} input via F/G and H	3.4	-	2.7	-	ns

CLB Switching Characteristics *(Continued)*

Symbol	Description	-3		-1		Units
		Min	Max	Min	Max	
Hold Time After Clock K						
T_{CKI}	F/G inputs	0	-	0	-	ns
T_{CKIH}	F/G inputs via H	0	-	0	-	ns
T_{CKHH0}	C inputs via SR/H0 through H	0	-	0	-	ns
T_{CKHH1}	C inputs via H1 through H	0	-	0	-	ns
T_{CKHH2}	C inputs via D_{IN}/H2 through H	0	-	0	-	ns
T_{CKDI}	C inputs via D_{IN}/H2	0	-	0	-	ns
T_{CKEC}	C inputs via EC	0	-	0	-	ns
T_{CKR}	C inputs via SR, going Low (inactive)	0	-	0	-	ns
Clock						
T_{CH}	Clock High time	3.0	-	2.5	-	ns
T_{CL}	Clock Low time	3.0	-	2.5	-	ns
Set/Reset Direct						
T_{RPW}	Width (High)	3.0	-	2.5	-	ns
T_{RIO}	Delay from C inputs via S/R, going High to Q	-	3.7	-	2.8	ns
Global Set/Reset						
T_{MRW}	Minimum GSR pulse width	-	19.8	-	15.0	ns
T_{MRQ}	Delay from GSR input to any Q	See page 95 for T_{RRI} values per device.				
F_{TOG}	Toggle frequency (MHz) (for export control)	-	166	-	200	MHz

XQ4000XL RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000XL devices and are expressed in nanoseconds unless otherwise noted.

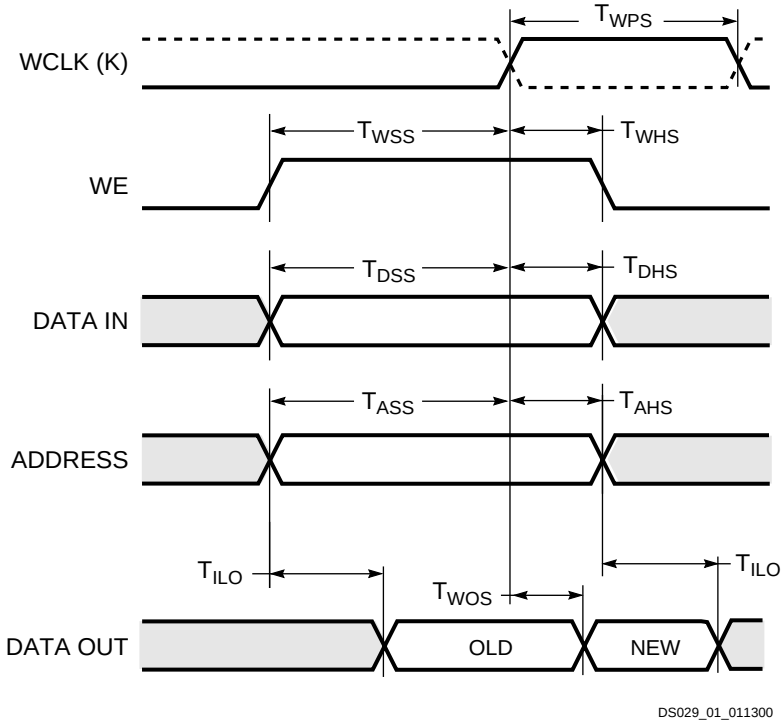
Single-Port RAM Synchronous (Edge-Triggered) Write Operation Characteristics

Symbol	Single Port RAM	Size	-3		-1		Units
			Min	Max	Min	Max	
Write Operation							
T_{WCS}	Address write cycle time (clock K period)	16x2	9.0	-	7.7	-	ns
T_{WCTS}		32x1	9.0	-	7.7	-	ns
T_{WPS}	Clock K pulse width (active edge)	16x2	4.5	-	3.9	-	ns
T_{WPTS}		32x1	4.5	-	3.9	-	ns
T_{ASS}	Address setup time before clock K	16x2	2.2	-	1.7	-	ns
T_{ASTS}		32x1	2.2	-	1.7	-	ns
T_{AHS}	Address hold time after clock K	16x2	0	-	0	-	ns
T_{AHTS}		32x1	0	-	0	-	ns
T_{DSS}	D_{IN} setup time before clock K	16x2	2.0	-	1.7	-	ns
T_{DSTS}		32x1	2.5	-	2.1	-	ns
T_{DHS}	D_{IN} hold time after clock K	16x2	0	-	0	-	ns
T_{DHTS}		32x1	0	-	0	-	ns
T_{WSS}	WE setup time before clock K	16x2	2.0	-	1.6	-	ns
T_{WSTS}		32x1	1.8	-	1.5	-	ns
T_{WHS}	WE hold time after clock K	16x2	0	-	0	-	ns
T_{WHTS}		32x1	0	-	0	-	ns
T_{WOS}	Data valid after clock K	16x2	-	6.8	-	5.8	ns
T_{WOTS}		32x1	-	8.1	-	6.9	ns
Read Operation							
T_{RC}	Address read cycle time	16x2	4.5	-	2.6	-	ns
T_{RCT}		32x1	6.5	-	3.8	-	ns
T_{ILO}	Data valid after address change (no Write Enable)	16x2	-	1.6	-	1.3	ns
T_{IHO}		32x1	-	2.7	-	2.2	ns
T_{ICK}	Address setup time before clock K	16x2	1.1	-	0.9	-	ns
T_{IHCK}		32x1	2.2	-	1.7	-	ns

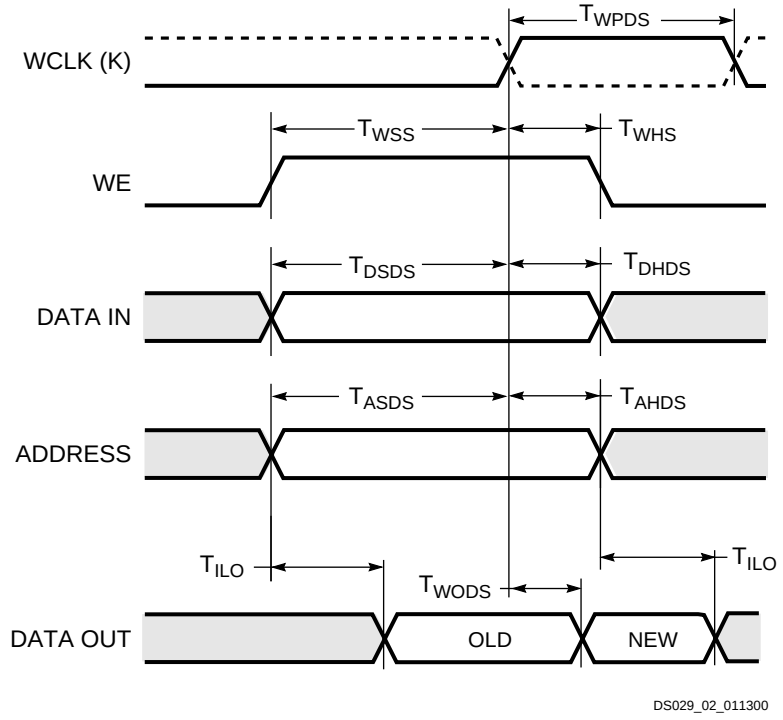
Dual-Port RAM Synchronous (Edge-Triggered) Write Operation Characteristics

Symbol	Dual Port RAM	Size(1)	-3		-1		Units
			Min	Max	Min	Max	
Write Operation							
T_{WCDS}	Address write cycle time (clock K period)	16x1	9.0		7.7		ns
T_{WPDS}	Clock K pulse width (active edge)	16x1	4.5	-	3.9	-	ns
T_{ASDS}	Address setup time before clock K	16x1	2.5	-	1.7	-	ns
T_{AHDS}	Address hold time after clock K	16x1	0	-	0	-	ns
T_{DSDS}	D_{IN} setup time before clock K	16x1	2.5	-	2.0	-	ns
T_{DHDS}	D_{IN} hold time after clock K	16x1	0	-	0	-	ns
T_{WSDS}	WE setup time before clock K	16x1	1.8	-	1.6	-	ns
T_{WHDS}	WE hold time after clock K	16x1	0	-	0	-	ns
T_{WODS}	Data valid after clock K	16x1	-	7.8	-	6.7	ns

XQ4000XL CLB Single-Port RAM Synchronous (Edge-Triggered) Write Timing



XQ4000XL CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing



XQ4000XL Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

Output Flip-Flop, Clock to Out(1,2,3)

Symbol	Description	Device	All Min	-3 Max	-1 Max	Units
T_{ICKOF}	Global low skew clock to output using OFF(4)	XQ4013XL	1.5	8.6	-	ns
		XQ4036XL	2.0	9.8	-	ns
		XQ4062XL	2.3	11.3	-	ns
		XQ4085XL	2.5	-	9.5	ns
T_{SLOW}	For output SLOW option add	All Devices	3.0	3.0	3.0	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs for FAST mode configurations.
3. Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load.
4. OFF = Output Flip-Flop

Output Flip-Flop, Clock to Out, BUFGEs 1, 2, 5, and 6

Symbol	Description	Device	All Min	-3 Max	-1 Max	Units
T_{ICKEOF}	Global early clock to output using OFF Values are for BUFGEs 1, 2, 5, and 6.	XQ4013XL	1.3	7.4	-	ns
		XQ4036XL	1.2	8.1	-	ns
		XQ4062XL	1.2	9.9	-	ns
		XQ4085XL	1.3	-	8.5	ns

Notes:
1. Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs for FAST mode configurations.
2. Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load.

Output Flip-Flop, Clock to Out, BUFGEs 3, 4, 7, and 8

Symbol	Description	Device	All Min	-3 Max	-1 Max	Units
T_{ICKEOF}	Global early clock to output using OFF Values are for BUFGEs 3, 4, 7, and 8.	XQ4013XL	1.8	8.8	-	ns
		XQ4036XL	1.8	9.7	-	ns
		XQ4062XL	2.0	10.9	-	ns
		XQ4085XL	2.2	-	9.3	ns

Notes:

1. Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs for FAST mode configurations.
2. Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load.

Capacitive Load Factor

Figure 1 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay.

Figure 1 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

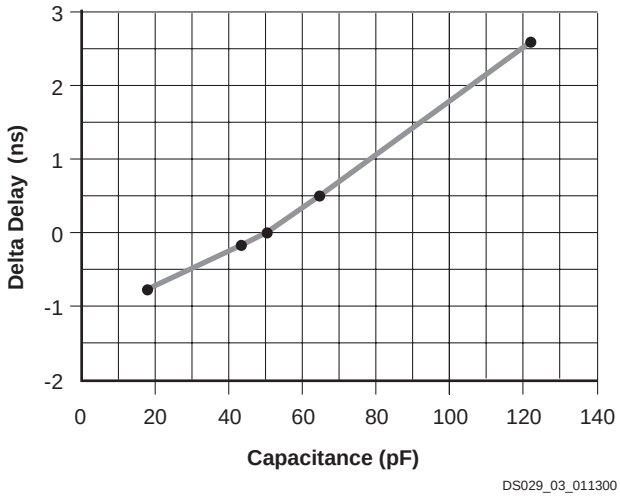


Figure 1: **Delay Factor at Various Capacitive Loads**

XQ4000XL Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

Global Low Skew Clock, Input Setup and Hold Times[1,2]

Symbol	Description	Device[1]	-3 Min	-1 Min	Units
No Delay					
T_{PSN}/T_{PHN}	Global early clock and IFF[3]	XQ4013XL	1.2 / 3.2	-	ns
	Global early clock and FCL[4]	XQ4036XL	1.2 / 5.5	-	ns
		XQ4062XL	1.2 / 7.0	-	ns
		XQ4085XL	-	0.9 / 7.1	ns
Partial Delay					
T_{PSP}/T_{PHP}	Global early clock and IFF[3]	XQ4013XL	6.1 / 0.0	-	ns
	Global early clock and FCL[4]	XQ4036XL	6.4 / 1.0	-	ns
		XQ4062XL	6.7 / 1.2	-	ns
		XQ4085XL	-	9.8 / 1.2	ns
Full Delay					
T_{PSD}/T_{PHD}	Global early clock and IFF[3]	XQ4013XL	6.4 / 0.0	-	ns
		XQ4036XL	6.6 / 0.0	-	ns
		XQ4062XL	6.8 / 0.0	-	ns
		XQ4085XL	-	9.6 / 0.0	ns

Notes:

1. The XQ4013XL, XQ4036XL, and XQ4062XL have significantly faster partial and full delay setup times than other devices.
2. Input setup time is measured with the fastest route and the lightest load. Input hold time is measured using the furthest distance and a reference load of one clock pin per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be used as a worst-case pin-to-pin no-delay input hold specification.
3. IFF = Input Flip-Flop or Latch
4. FCL = Fast Capture Latch

Global Early Clock BUFEs 1, 2, 5, and 6 Setup and Hold for IFF and FCL(1,2)

Symbol	Description	Device	-3 Min	-1 Min
No Delay				
T_{PSEN}/T_{PHEN} T_{PFSEN}/T_{PFHEN}	Global early clock and IFF(3) Global early clock and FCL(4)	XQ4013XL	1.2 / 4.7	-
		XQ4036XL	1.2 / 6.7	-
		XQ4062XL	1.2 / 8.4	-
		XQ4085XL	-	0.9 / 6.6
Partial Delay				
T_{PSEPN}/T_{PHEP} T_{PFSEP}/T_{PFHEP}	Global early clock and IFF(3) Global early clock and FCL(4)	XQ4013XL	6.4 / 0.0	-
		XQ4036XL	7.0 / 0.8	-
		XQ4062XL	9.0 / 0.8	-
		XQ4085XL	-	11.0 / 0.0
Full Delay				
T_{PSEPD}/T_{PHED}	Global early clock and IFF(3)	XQ4013XL	12.0 / 0.0	-
		XQ4036XL	13.8 / 0.0	-
		XQ4062XL	13.1 / 0.0	-
		XQ4085XL	-	13.6 / 0.0

Notes:

1. The XQ4013XL, XQ4036XL, and XQ4062XL have significantly faster partial and full delay setup times than other devices.
2. Input setup time is measured with the fastest route and the lightest load. Input hold time is measured using the furthest distance and a reference load of one clock pin per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be used as a worst-case pin-to-pin no-delay input hold specification.
3. IFF = Input Flip-Flop or Latch
4. FCL = Fast Capture Latch

Global Early Clock BUFEs 3, 4, 7, and 8 Setup and Hold for IFF and FCL(1,2)

Symbol	Description	Device	-3 Min	-1 Min
No Delay				
T_{PSEN}/T_{PHEN} T_{PFSEN}/T_{PFHEN}	Global early clock and IFF(3) Global early clock and FCL(4)	XQ4013XL	1.2 / 4.7	-
		XQ4036XL	1.2 / 6.7	-
		XQ4062XL	1.2 / 8.4	-
		XQ4085XL	-	0.9 / 6.6
Partial Delay				
T_{PSEPN}/T_{PHEP} T_{PFSEP}/T_{PFHEP}	Global early clock and IFF(3) Global early clock and FCL(4)	XQ4013XL	5.4 / 0.0	-
		XQ4036XL	6.4 / 0.8	-
		XQ4062XL	8.4 / 1.5	-
		XQ4085XL	-	11.0 / 0.0
Full Delay				
T_{PSEPD}/T_{PHED}	Global early clock and IFF(3)	XQ4013XL	10.0 / 0.0	-
		XQ4036XL	12.2 / 0.0	-
		XQ4062XL	13.1 / 0.0	-
		XQ4085XL	-	13.6 / 0.0

Notes:

1. The XQ4013XL, XQ4036XL, and XQ4062XL have significantly faster partial and full delay setup times than other devices.
2. Input setup time is measured with the fastest route and the lightest load. Input hold time is measured using the furthest distance and a reference load of one clock pin per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be used as a worst-case pin-to-pin no-delay input hold specification.
3. IFF = Input Flip-Flop or Latch
4. FCL = Fast Capture Latch

XQ4000XL IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol	Description	Device	-3		-1		Units
			Min	Max	Min	Max	
Clocks							
T_{ECIK}	Clock enable (EC) to clock (IK)	All devices	0.1	-	0.1	-	ns
T_{OKIK}	Delay from FCL enable (OK) active edge to IFF clock (IK) active edge	All devices	2.2	-	1.6	-	ns
Setup Times							
T_{PICK}	Pad to clock (IK), no delay	All devices	1.7	-	1.3	-	ns
T_{PICKF}	Pad to clock (IK), via transparent fast capture latch, no delay	All devices	2.3	-	1.8	-	ns
T_{POCK}	Pad to fast capture latch enable (OK), no delay	All devices	1.2	-	0.9	-	ns
Hold Times							
	All Hold Times	All devices	0	-	0	-	ns
Global Set/Reset							
T_{MRW}	Minimum GSR pulse width	All devices	-	19.8	-	15.0	ns
T_{RRI}	Delay from GSR input to any Q(2)	XQ4013XL	-	15.9	-	-	ns
		XQ4036XL	-	22.5	-	-	ns
		XQ4062XL	-	29.1	-	-	ns
		XQ4085XL	-	-	-	26.0	ns
Propagation Delays							
T_{PID}	Pad to I1, I2	All devices	-	1.6	-	1.7	ns
T_{PLI}	Pad to I1, I2 via transparent input latch, no delay	All devices	-	3.1	-	2.4	ns
T_{PFLI}	Pad to I1, I2 via transparent FCL and input latch, no delay	All devices	-	3.7	-	2.8	ns
T_{IKRI}	Clock (IK) to I1, I2 (flip-flop)	All devices	-	1.7	-	1.3	ns
T_{IKLI}	Clock (IK) to I1, I2 (latch enable, active Low)	All devices	-	1.8	-	1.4	ns
T_{OKLI}	FCL enable (OK) active edge to I1, I2 (via transparent standard input latch)	All devices	-	3.6	-	2.7	ns

Notes:
1. IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch
2. Indicates Minimum Amount of Time to Assure Valid Data.

XQ4000XL IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values are expressed in nanoseconds unless otherwise noted.

Symbol	Description	-3		-1		Units
		Min	Max	Min	Max	
Clocks						
T_{CH}	Clock High	3.0	-	2.5	-	ns
T_{CL}	Clock Low	3.0	-	2.5	-	ns
Propagation Delays						
T_{OKPOF}	Clock (OK) to pad	-	5.0	-	3.8	ns
T_{OPF}	Output (O) to pad	-	4.1	-	3.1	ns
T_{TSHZ}	High-Z to pad High-Z (slew-rate independent)	-	4.4	-	3.0	ns
T_{TSONF}	High-Z to pad active and valid	-	4.1	-	3.3	ns
T_{OFPF}	Output (O) to pad via fast output MUX	-	5.5	-	4.2	ns
T_{OKFPF}	Select (OK) to pad via fast MUX	-	5.1	-	3.9	ns
Setup and Hold Times						
T_{OOK}	Output (O) to clock (OK) setup time	0.5	-	0.3	-	ns
T_{OKO}	Output (O) to clock (OK) hold time	0	-	0	-	ns
T_{ECOK}	Clock Enable (EC) to clock (OK) setup time	0	-	0	-	ns
T_{OKEC}	Clock Enable (EC) to clock (OK) hold time	0.3	-	0.1	-	ns
Global Set/Reset						
T_{MRW}	Minimum GSR pulse width	19.8	-	15.0	-	ns
T_{RPO}	Delay from GSR input to any pad(2)					
	XQ4013XL	-	20.5	-	-	ns
	XQ4036XL	-	27.1	-	-	ns
	XQ4062XL	-	33.7	-	-	ns
	XQ4085XL	-		-	29.5	ns
Slew Rate Adjustment						
T_{SLOW}	For output SLOW option add	-	3.0	-	2.0	ns

Notes:
1. Output timing is measured at ~50% V_{CC} threshold, with 50 pF external capacitive loads.
2. Indicates Minimum Amount of Time to Assure Valid Data.

CB228 Pinouts

Table 2: **CB228 Package Pinouts**

Pin Name	CB228
VTT	
GND	P1
BUFGP_TL_A16_GCK1_IO	P2
A17_IO	P3
IO	P4
IO	P5
TDI_IO	P6
TCK_IO	P7
IO	P8
IO	P9
IO	P10
IO	P11
IO	P12
IO	P13
GND	P14
IO_FCLK1	P15
IO	P16
TMS_IO	P17
IO	P18
IO	P19
IO	P20
IO	P21
IO	P22
IO	P23
IO	P24
IO	P25
IO	P26
GND	P27
V_{CC}	P28
IO	P29
IO	P30
IO	P31
IO	P32
IO	P33
IO	P34
IO	P35
IO	P36
V_{CC}	P37
IO	P38

Table 2: **CB228 Package Pinouts *(Continued)***

Pin Name	CB228
IO	P39
IO	P40
IO_FCLK2	P41
GND	P42
IO	P43
IO	P44
IO	P45
IO	P46
IO	P47
IO	P48
IO	P49
IO	P50
IO	P51
IO	P52
IO	P53
BUFGS_BL_GCK2_IO	P54
M1	P55
GND	P56
M0	P57
V_{CC}	P58
M2	P59
BUFGP_BL_GCK3_IO	P60
HDC_IO	P61
IO	P62
IO	P63
IO	P64
LDC_IO	P65
IO	P66
IO	P67
IO	P68
IO	P69
IO	P70
IO	P71
GND	P72
IO	P73
IO	P74
IO	P75
IO	P76
IO	P77
IO	P78

Table 2: **CB228 Package Pinouts *(Continued)***

Pin Name	CB228
IO	P79
IO	P80
IO	P81
IO	P82
IO	P83
/ERR_INIT_IO	P84
V_{CC}	P85
GND	P86
IO	P87
IO	P88
IO	P89
IO	P90
IO	P91
IO	P92
IO	P93
IO	P94
V_{CC}	P95
IO	P96
IO	P97
IO	P98
IO	P99
GND	P100
IO	P101
IO	P102
IO	P103
IO	P104
IO	P105
IO	P106
IO	P107
IO	P108
IO	P109
IO	P110
IO	P111
BUFGS_BR_GCK4_IO	P112
GND	P113
DONE	P114
V_{CC}	P115
/PROGRAM	P116
D7_IO	P117
BUFGP_BR_GCK5_IO	P118

Table 2: **CB228 Package Pinouts *(Continued)***

Pin Name	CB228
IO	P119
IO	P120
IO	P121
IO	P122
D6_IO	P123
IO	P124
IO	P125
IO	P126
IO	P127
IO	P128
GND	P129
IO	P130
IO	P131
IO_FCLK3	P132
IO	P133
D5_IO	P134
/CS0_IO	P135
IO	P136
IO	P137
IO	P138
IO	P139
D4_IO	P140
IO	P141
V_{CC}	P142
GND	P143
D3_IO	P144
/RS_IO	P145
IO	P146
IO	P147
IO	P148
IO	P149
D2_IO	P150
IO	P151
V_{CC}	P152
IO	P153
IO_FCLK4	P154
IO	P155
IO	P156
GND	P157
IO	P158

Table 2: **CB228 Package Pinouts *(Continued)***

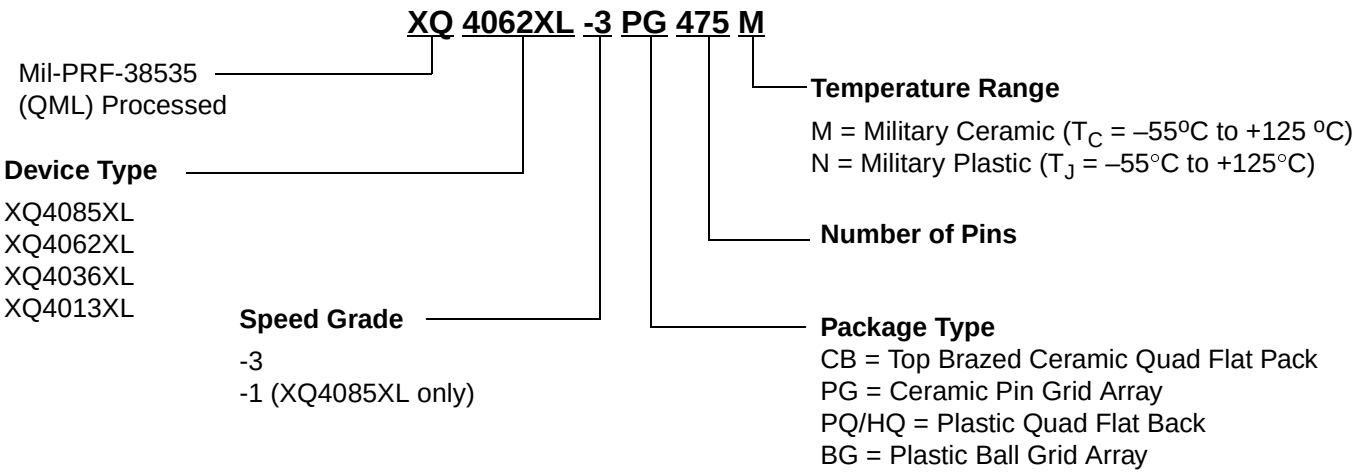
Pin Name	CB228
IO	P159
IO	P160
IO	P161
IO	P162
IO	P163
D1_IO	P164
BUSY_/RDY_RCLK_IO	P165
IO	P166
IO	P167
D0_DIN_IO	P168
BUFGS_TR_GCK6_DOUT_IO	P169
CCLK	P170
V_{CC}	P171
TDO	P172
GND	P173
A0_/WS_IO	P174
BUFGP_TR_GCK7_A1_IO	P175
IO	P176
IO	P177
CSI_A2_IO	P178
A3_IO	P179
IO	P180
IO	P181
IO	P182
IO	P183
IO	P184
IO	P185
GND	P186
IO	P187
IO	P188
IO	P189
IO	P190
V_{CC}	P191
A4_IO	P192
A5_IO	P193
IO	P194
IO	P195
A21_IO	P196
A20_IO	P197
A6_IO	P198

Table 2: **CB228 Package Pinouts *(Continued)***

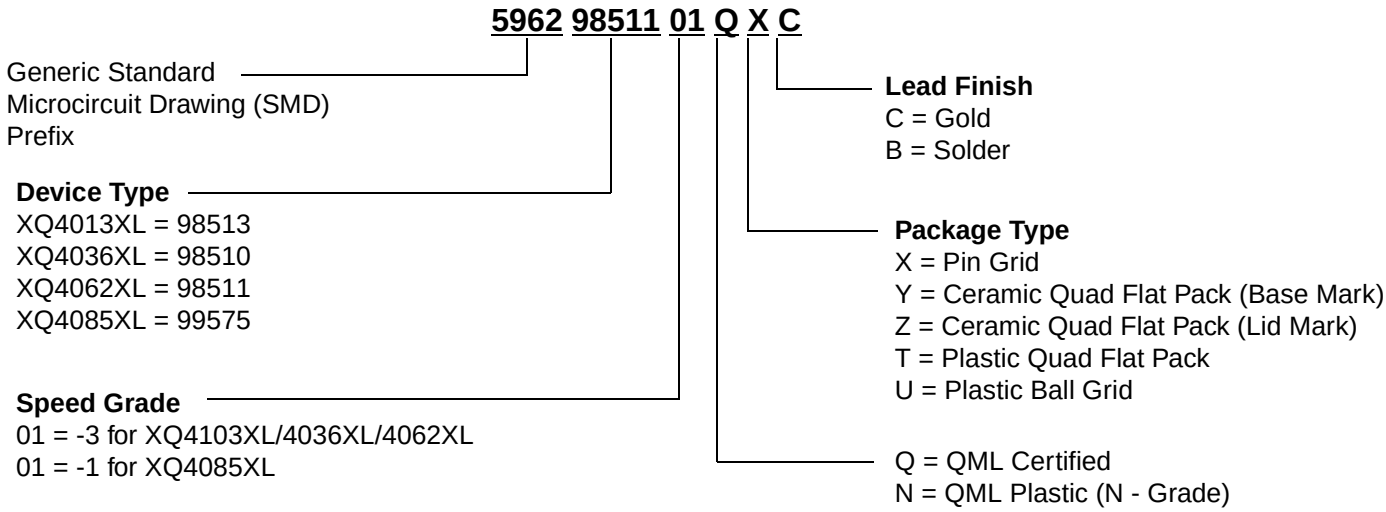
Pin Name	CB228
A7_IO	P199
GND	P200
V_{CC}	P201
A8_IO	P202
A9_IO	P203
A19_IO	P204
A18_IO	P205
IO	P206
IO	P207
A10_IO	P208
A11_IO	P209
V_{CC}	P210
IO	P211
IO	P212
IO	P213
IO	P214
GND	P215
IO	P216
IO	P217
IO	P218
IO	P219
A12_IO	P220
A13_IO	P221
IO	P222
IO	P223
IO	P224
IO	P225
A14_IO	P226
BUFGS_TL_GCK8_A15_IO	P227
V_{CC}	P228

Ordering Information

Example for QPRO™ military temperature part:



Example for SMD part:



Revision History

The following table shows the revision history for this document

Date	Version	Description
05/01/98	1.0	Original document release.
01/01/99	1.1	Addition of new packages, clarification of parameters.
02/09/00	1.2	Addition of XQ4085XL-1 speed grade part.
06/25/00	1.3	Updated timing specifications to match with commercial data sheet. Updated format.

QPRO XQR4000XL Radiation Hardened FPGAs

DS071 (v1.1) June 25, 2000 **Product Specification**

XQR4000XL Series Features

- Radiation-hardened FPGAs for space and satellite applications
- Guaranteed total ionizing dose
- Latch-up immune
- Low soft upset rate
- Guaranteed to meet full electrical specifications over –55°C to +125°C
- Available in -3 speed
- System featured FPGAs
  - SelectRAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - Eight global low-skew clock or signal distribution networks
- System performance beyond 60 MHz
- Flexible array architecture
- Low power segmented routing architecture
- Systems-oriented features
  - IEEE 1149.1-compatible boundary scan logic support
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12 mA sink current per output
- Configured by loading binary file
  - Unlimited reprogrammability
- Readback capability
  - Program verification
  - Internal node observability
- Development system runs on most common computer platforms
  - Interfaces to popular design environments
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization
- Highest capacity: over 130,000 usable gates
- Buffered interconnect for maximum speed
- New latch capability in configurable logic blocks
- Improved VersaRing™ I/O interconnect for better fixed pinout flexibility
  - Virtually unlimited number of clock signals
- Optional multiplexer or 2-input function generator on device outputs
- 5V tolerant I/Os
- Advanced 0.35µ process
- Processed on Xilinx QML line

2

Table 1: **XQR4000XL Series Radiation Hardened Field Programmable Gate Arrays**

Device	Logic Cells	Max. Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)(1)	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. User I/O	Packages
XQR4013XL	1,368	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	192	CB228
XQR4036XL	3,078	36,000	41,472	22,000 - 65,000	36 x 36	1,296	3,168	288	CB228
XQR4062XL	5,472	62,000	73,728	40,000 - 130,000	48 x 48	2,304	5,376	384	CB228

Notes:
1. Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

Radiation Specifications

Symbol	Description	Min	Max	Units
TID	Total ionizing dose	-	60K	RAD(Si)
SEL	Single event Latch-up LET> 100 MeV CM^2/mg. @ +125°C	-	0	
SEU	Single event upset galactic p+(1)	-	2.43E – 8	Upsets/ Bit-Day
SEU	Single event upset galactic heavy Ion(1)	-	9.54E – 8	Upsets/ Bit-Day
SEU	Single event upset trapped p+(1)	-	2.50E – 7	Upsets/ Bit-Day
SEU	Single event upset galactic p+(2)	-	5.62E – 8	Upsets/ Bit-Day
SEU	Single event upset galactic heavy Ion(2)	-	2.43E – 7	Upsets/ Bit-Day

Notes:
1. 680 Km LEO, 98^o Inclination, 100-mil Al Shielding
2. 35,000 Km GEO, 0^o Inclination, 100-mil Al Shielding
3. Simulations done using Space Radiation Version 2.5 code from Severn Communication Corp.

XQR4000XL Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or devicefamilies. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions.

All specifications subject to change without notice.

Additional Specifications

Except for pin-to-pin input and output parameters, the a.c. parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. For design considerations requiring more detailed timing information, see the appropriate family AC supplements available on the Xilinx web site at:

http://www.xilinx.com/partinfo/databook.htm.

Absolute Maximum Ratings(1)

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to 4.0	V
V_{IN}	Input voltage relative to GND(2)	–0.5 to 5.5	V
V_{TS}	Voltage applied to High-Z output(2)	–0.5 to 5.5	V
V_{CCt}	Longest supply voltage rise time from 1V to 3V	50	ms
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C
T_J	Junction temperature	+150	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. Maximum DC overshoot or undershoot above V_{CC} or below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0 V or overshoot to V_{CC} + 2.0V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Recommended Operating Conditions(1)

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_C = –55°C to +125°C	3.0	3.6	V
V_{IH}	High-level input voltage(2)	50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage	0	30% of V_{CC}	V
T_{IN}	Input signal transition time	-	250	ns

Notes:

1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Input and output measurement threshold is ~50% of V_{CC}.

XQR4000XL DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage at I_{OH} = –4 mA, V_{CC} min (LVTTL)	2.4	-	V
	High-level output voltage at I_{OH} = –500 µA, (LVCMOS)	90% V_{CC}	-	V
V_{OL}	Low-level output voltage at I_{OL} = 12 mA, V_{CC} min (LVTTL)(1)	-	0.4	V
	Low-level output voltage at I_{OL} = 1500 µA, (LVCMOS)	-	10% V_{CC}	V
V_{DR}	Data retention supply voltage (below which configuration data may be lost)	2.5	-	V
I_{CCO}	Quiescent FPGA supply current(2)	-	5	mA
I_L	Input or output leakage current	–10	+10	µA
C_{IN}	Input capacitance (sample tested)	-	10	pF
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V (sample tested)	0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 3.6V (sample tested)	0.02	0.15	mA
I_{RLL}	Horizontal longline pull-up (when selected) at logic Low	0.3	2.0	mA

Notes:
1. With up to 64 pins simultaneously sinking 12 mA.
2. With no output current loads, no active input or Longline pull-up resistors, all I/O pins in a High-Z state and floating.

Power-On Power Supply Requirements

Xilinx FPGAs require a minimum rated power supply current capacity to insure proper initialization, and the power supply ramp-up time does affect the current required. A fast ramp-up time requires more current than a slow ramp-up time. The slowest ramp-up time is 50 ms. Current capacity is not specified for a ramp-up time faster than 2 ms. The current capacity varies linealy with ramp-up time, *e.g.*, an XQR4036XL with a ramp-up time of 25 ms would require a capacity predicted by the point on the straight line drawn from 1A at 120 µs to 500 mA at 50 ms at the 25 ms time mark. This point is approximately 750 mA .

Product	Description	Ramp-up Time	
		Fast (120 µs)	Slow (50 ms)
XQR4013 - 36XL	Minimum required current supply	1A	500 mA
XC4062XL	Minimum required current supply	2A	500 mA

Notes:
1. Devices are guaranteed to initialize properly with the minimum current listed above. A larger capacity power supply may result in a larger initialization current.
2. This specification applies to Commercial and Industrial grade products only.
3. Ramp-up Time is measured from $0V_{DC}$ to $3.6V_{DC}$. Peak current required lasts less than 3 ms, and occurs near the internal power on reset threshold voltage. After initialization and before configuration, I_{CC} max is less than 10 mA.

XQR4000XL AC Switching Characteristic

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature)

Global Buffer Switching Characteristics

Symbol	Description	Device	-3		Units
			Min	Max	
T_{GLS}	Delay from pad through Global Low Skew buffer, to any clock K	XQR4013XL	0.6	3.6	ns
		XQR4036XL	1.1	4.8	ns
		XQR4062XL	1.4	6.3	ns

Global Early BUFGEs 1, 2, 5, and 6 to IOB Clock Characteristics

Symbol	Description	Device	-3		Units
			Min	Max	
T_{GE}	Delay from pad through Global Early buffer, to any IOB clock. Values are for BUFGEs 1, 2, 5 and 6.	XQR4013XL	0.4	2.4	ns
		XQR4036XL	0.3	3.1	ns
		XQR4062XL	0.3	4.9	ns

Global Early BUFGEs 3, 4, 7, and 8 to IOB Clock Characteristics

Symbol	Description	Device	-3		Units
			Min	Max	
T_{GE}	Delay from pad through Global Early buffer, to any IOB clock. Values are for BUFGEs 3, 4, 7 and 8.	XQR4013XL	0.7	2.4	ns
		XQR4036XL	0.9	4.7	ns
		XQR4062XL	1.2	5.9	ns

XQR4000XL CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQR4000XL devices and expressed in nanoseconds unless otherwise noted.

CLB Switching Characteristics

Symbol	Description	-3		Units
		Min	Max	
Combinatorial Delays				
T_{ILO}	F/G inputs to X/Y outputs	-	1.6	ns
T_{IHO}	F/G inputs via H' to X/Y outputs	-	2.7	ns
T_{ITO}	F/G inputs via transparent latch to Q outputs	-	2.9	ns
T_{HH0O}	C inputs via SR/H0 via H to X/Y outputs	-	2.5	ns
T_{HH1O}	C inputs via H1 via H to X/Y outputs	-	2.4	ns
T_{HH2O}	C inputs via D_{IN}/H2 via H to X/Y outputs	-	2.5	ns
T_{CBYP}	C inputs via EC, D_{IN}/H2 to YQ, XQ output (bypass)	-	1.5	ns
CLB Fast Carry Logic				
T_{OPCY}	Operand inputs (F1, F2, G1, G4) to C_{OUT}	-	2.7	ns
T_{ASCY}	Add/subtract input (F3) to C_{OUT}	-	3.3	ns
T_{INCY}	Initialization inputs (F1, F3) to C_{OUT}	-	2.0	ns
T_{SUM}	C_{IN} through function generators to X/Y outputs	-	2.8	ns
T_{BYP}	C_{IN} to C_{OUT}, bypass function generators	-	0.26	ns
T_{NET}	Carry net delay, C_{OUT} to C_{IN}	-	0.32	ns
Sequential Delays				
T_{CKO}	Clock K to flip-flop outputs Q	-	2.1	ns
T_{CKLO}	Clock K to latch outputs Q	-	2.1	ns
Setup Time Before Clock K				
T_{ICK}	F/G inputs	1.1	-	ns
T_{IHCK}	F/G inputs via H	2.2	-	ns
T_{HH0CK}	C inputs via H0 through H	2.0	-	ns
T_{HH1CK}	C inputs via H1 through H	1.9	-	ns
T_{HH2CK}	C inputs via H2 through H	2.0	-	ns
T_{DICK}	C inputs via D_{IN}	0.9	-	ns
T_{ECCK}	C inputs via EC	1.0	-	ns
T_{RCK}	C inputs via S/R, going Low (inactive)	0.6	-	ns
T_{CCK}	C_{IN} input via F/G	2.3	-	ns
T_{CHCK}	C_{IN} input via F/G and H	3.4	-	ns

CLB Switching Characteristics *(Continued)*

Symbol	Description	-3		Units
		Min	Max	
Hold Time After Clock K				
T_{CKI}	F/G inputs	0	-	ns
T_{CKIH}	F/G inputs via H	0	-	ns
T_{CKHH0}	C inputs via SR/H0 through H	0	-	ns
T_{CKHH1}	C inputs via H1 through H	0	-	ns
T_{CKHH2}	C inputs via D_{IN}/H2 through H	0	-	ns
T_{CKDI}	C inputs via D_{IN}/H2	0	-	ns
T_{CKEC}	C inputs via EC	0	-	ns
T_{CKR}	C inputs via SR, going Low (inactive)	0	-	ns
Clock				
T_{CH}	Clock High time	3.0	-	ns
T_{CL}	Clock Low time	3.0	-	ns
Set/Reset Direct				
T_{RPW}	Width (High)	3.0	-	ns
T_{RIO}	Delay from C inputs via S/R, going High to Q	-	3.7	ns
Global Set/Reset				
T_{MRW}	Minimum GSR pulse width	-	19.8	ns
T_{MRQ}	Delay from GSR input to any Q	See page 116 for T_{RRI} values per device.		
F_{TOG}	Toggle frequency (MHz) (for export control)	-	166	MHz

XQR4000XL RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQR4000XL devices and are expressed in nanoseconds unless otherwise noted.

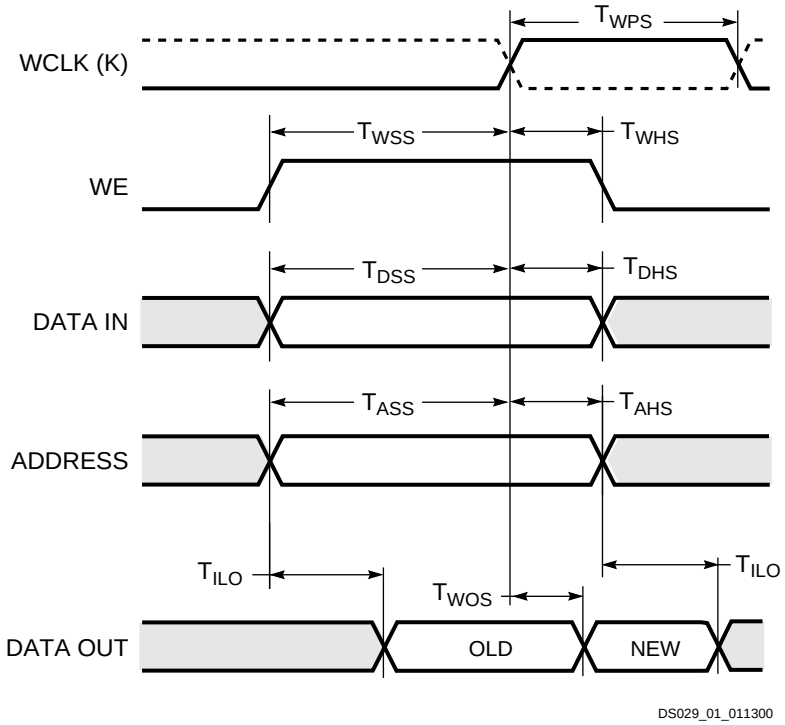
Single-Port RAM Synchronous (Edge-Triggered) Write Operation Characteristics

Symbol	Single Port RAM	Size	-3		Units
			Min	Max	
Write Operation					
T_{WCS}	Address write cycle time (clock K period)	16x2	9.0	-	ns
T_{WCTS}		32x1	9.0	-	ns
T_{WPS}	Clock K pulse width (active edge)	16x2	4.5	-	ns
T_{WPTS}		32x1	4.5	-	ns
T_{ASS}	Address setup time before clock K	16x2	2.2	-	ns
T_{ASTS}		32x1	2.2	-	ns
T_{AHS}	Address hold time after clock K	16x2	0	-	ns
T_{AHTS}		32x1	0	-	ns
T_{DSS}	D_{IN} setup time before clock K	16x2	2.0	-	ns
T_{DSTS}		32x1	2.5	-	ns
T_{DHS}	D_{IN} hold time after clock K	16x2	0	-	ns
T_{DHTS}		32x1	0	-	ns
T_{WSS}	WE setup time before clock K	16x2	2.0	-	ns
T_{WSTS}		32x1	1.8	-	ns
T_{WHS}	WE hold time after clock K	16x2	0	-	ns
T_{WHTS}		32x1	0	-	ns
T_{WOS}	Data valid after clock K	16x2	-	6.8	ns
T_{WOTS}		32x1	-	8.1	ns
Read Operation					
T_{RC}	Address read cycle time	16x2	4.5	-	ns
T_{RCT}		32x1	6.5	-	ns
T_{ILO}	Data valid after address change (no Write Enable)	16x2	-	1.6	ns
T_{IHO}		32x1	-	2.7	ns
T_{ICK}	Address setup time before clock K	16x2	1.1	-	ns
T_{IHCK}		32x1	2.2	-	ns

Dual-Port RAM Synchronous (Edge-Triggered) Write Operation Characteristics

Symbol	Dual Port RAM	Size	-3		Units
			Min	Max	
Write Operation					
T_{WCDS}	Address write cycle time (clock K period)	16x1	9.0		ns
T_{WPDS}	Clock K pulse width (active edge)	16x1	4.5	-	ns
T_{ASDS}	Address setup time before clock K	16x1	2.5	-	ns
T_{AHDS}	Address hold time after clock K	16x1	0	-	ns
T_{DSDS}	D_{IN} setup time before clock K	16x1	2.5	-	ns
T_{DHDS}	D_{IN} hold time after clock K	16x1	0	-	ns
T_{WSDS}	WE setup time before clock K	16x1	1.8	-	ns
T_{WHDS}	WE hold time after clock K	16x1	0	-	ns
T_{WODS}	Data valid after clock K	16x1	-	7.8	ns

XQR4000XL CLB Single-Port RAM Synchronous (Edge-Triggered) Write Timing



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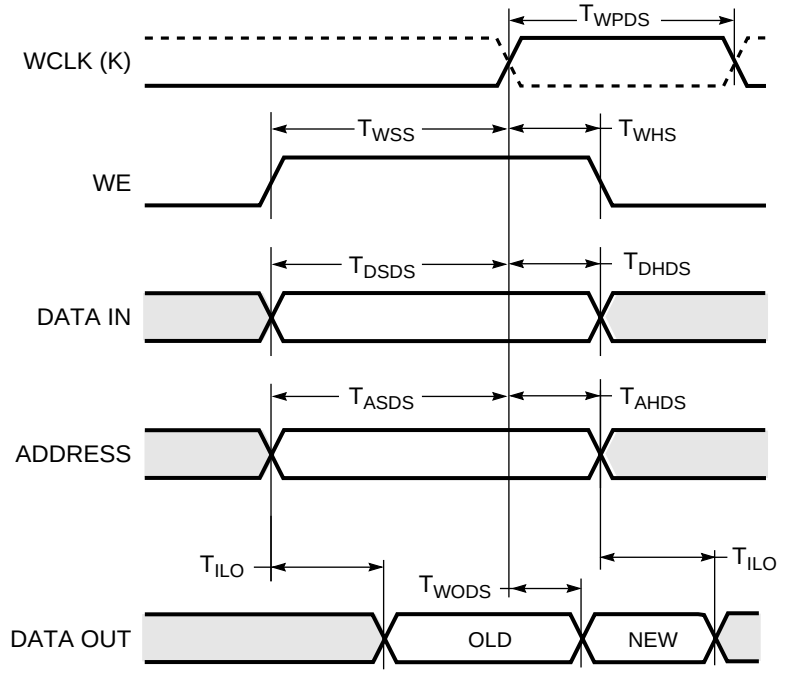
XQR4000XL CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing



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XQR4000XL Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

Output Flip-Flop, Clock to Out(1,2,3)

Symbol	Description	Device	-3		Units
			Min	Max	
T_{ICKOF}	Global low skew clock to output using OFF(4)	XQR4013XL	1.5	8.6	ns
		XQR4036XL	2.0	9.8	ns
		XQR4062XL	2.3	11.3	ns
T_{SLOW}	For output SLOW option add	All Devices	3.0	3.0	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs for FAST mode configurations.
3. Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load.
4. OFF = Output Flip-Flop

Output Flip-Flop, Clock to Out, BUFGEs 1, 2, 5, and 6

Symbol	Description	Device	-3		Units
			Min	Max	
T_{ICKEOF}	Global early clock to output using OFF Values are for BUFGEs 1, 2, 5, and 6.	XQR4013XL	1.3	7.4	ns
		XQR4036XL	1.2	8.1	ns
		XQR4062XL	1.2	9.9	ns

Notes:
1. Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter T_{OKPOF} and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs for FAST mode configurations.
2. Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load.

Output Flip-Flop, Clock to Out, BUFGEs 3, 4, 7, and 8

Symbol	Description	Device	-3		Units
			Min	Max	
T_{ICKEOF}	Global early clock to output using OFF Values are for BUFGEs 3, 4, 7, and 8.	XQR4013XL	1.8	8.8	ns
		XQR4036XL	1.8	9.7	ns
		XQR4062XL	2.0	10.9	ns

Notes:

1. Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter T_{OKPOF} and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs for FAST mode configurations.
2. Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load.

Capacitive Load Factor

Figure 1 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay.

Figure 1 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

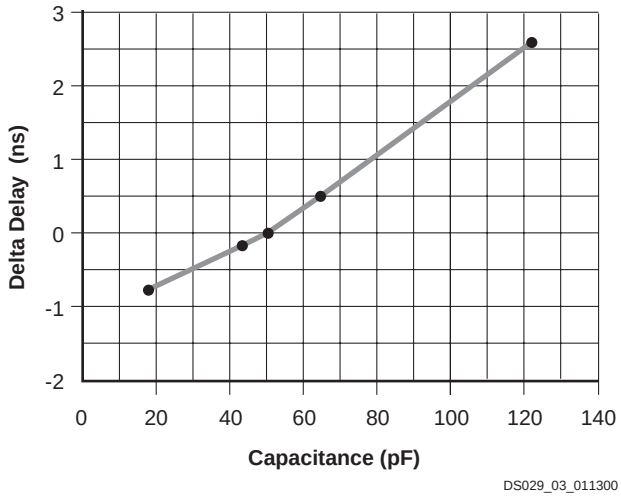


Figure 1: **Delay Factor at Various Capacitive Loads**

XQR4000XL Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

Global Low Skew Clock, Input Setup and Hold Times[1,2]

Symbol	Description	Device[1]	-3 Min	Units
No Delay				
T_{PSN}/T_{PHN}	Global early clock and IFF[3]	XQR4013XL	1.2 / 3.2	ns
	Global early clock and FCL[4]	XQR4036XL	1.2 / 5.5	ns
		XQR4062XL	1.2 / 7.0	ns
Partial Delay				
T_{PSP}/T_{PHP}	Global early clock and IFF[3]	XQR4013XL	6.1 / 0.0	ns
	Global early clock and FCL[4]	XQR4036XL	6.4 / 1.0	ns
		XQR4062XL	6.7 / 1.2	ns
Full Delay				
T_{PSD}/T_{PHD}	Global early clock and IFF[3]	XQR4013XL	6.4 / 0.0	ns
		XQR4036XL	6.6 / 0.0	ns
		XQR4062XL	6.8 / 0.0	ns

Notes:

1. The XQR4013XL, XQR4036XL, and XQR4062XL have significantly faster partial and full delay setup times than other devices.
2. Input setup time is measured with the fastest route and the lightest load. Input hold time is measured using the furthest distance and a reference load of one clock pin per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be used as a worst-case pin-to-pin no-delay input hold specification.
3. IFF = Input Flip-Flop or Latch
4. FCL = Fast Capture Latch

Global Early Clock BUFEs 1, 2, 5, and 6 Setup and Hold for IFF and FCL(1,2)

Symbol	Description	Device	-3 Min
No Delay			
T_{PSEN}/T_{PHEN}	Global early clock and IFF(3)	XQR4013XL	1.2 / 4.7
T_{PFSEN}/T_{PFHEN}	Global early clock and FCL(4)	XQR4036XL	1.2 / 6.7
		XQR4062XL	1.2 / 8.4
Partial Delay			
T_{PSEPN}/T_{PHEP}	Global early clock and IFF(3)	XQR4013XL	6.4 / 0.0
T_{PFSEP}/T_{PFHEP}	Global early clock and FCL(4)	XQR4036XL	7.0 / 0.8
		XQR4062XL	9.0 / 0.8
Full Delay			
T_{PSEPD}/T_{PHED}	Global early clock and IFF(3)	XQR4013XL	12.0 / 0.0
		XQR4036XL	13.8 / 0.0
		XQR4062XL	13.1 / 0.0

Notes:
1. The XQR4013XL, XQR4036XL, and XQR4062XL have significantly faster partial and full delay setup times than other devices.
2. Input setup time is measured with the fastest route and the lightest load. Input hold time is measured using the furthest distance and a reference load of one clock pin per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be used as a worst-case pin-to-pin no-delay input hold specification.
3. IFF = Input Flip-Flop or Latch
4. FCL = Fast Capture Latch

Global Early Clock BUFEs 3, 4, 7, and 8 Setup and Hold for IFF and FCL(1,2)

Symbol	Description	Device	-3 Min
No Delay			
T_{PSEN}/T_{PHEN}	Global early clock and IFF(3)	XQR4013XL	1.2 / 4.7
T_{PFSEN}/T_{PFHEN}	Global early clock and FCL(4)	XQR4036XL	1.2 / 6.7
		XQR4062XL	1.2 / 8.4
Partial Delay			
T_{PSEPN}/T_{PHEP}	Global early clock and IFF(3)	XQR4013XL	5.4 / 0.0
T_{PFSEP}/T_{PFHEP}	Global early clock and FCL(4)	XQR4036XL	6.4 / 0.8
		XQR4062XL	8.4 / 1.5
Full Delay			
T_{PSEPD}/T_{PHED}	Global early clock and IFF(3)	XQR4013XL	10.0 / 0.0
		XQR4036XL	12.2 / 0.0
		XQR4062XL	13.1 / 0.0

Notes:
1. The XQR4013XL, XQR4036XL, and XQR4062XL have significantly faster partial and full delay setup times than other devices.
2. Input setup time is measured with the fastest route and the lightest load. Input hold time is measured using the furthest distance and a reference load of one clock pin per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be used as a worst-case pin-to-pin no-delay input hold specification.
3. IFF = Input Flip-Flop or Latch
4. FCL = Fast Capture Latch

XQR4000XL IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Symbol	Description	Device	-3		Units
			Min	Max	
Clocks					
T_{ECIK}	Clock enable (EC) to clock (IK)	All devices	0.1	-	ns
T_{OKIK}	Delay from FCL enable (OK) active edge to IFF clock (IK) active edge	All devices	2.2	-	ns
Setup Times					
T_{PICK}	Pad to clock (IK), no delay	All devices	1.7	-	ns
T_{PICKF}	Pad to clock (IK), via transparent fast capture latch, no delay	All devices	2.3	-	ns
T_{POCK}	Pad to fast capture latch enable (OK), no delay	All devices	1.2	-	ns
Hold Times					
	All Hold Times	All devices	0	-	ns
Global Set/Reset					
T_{MRW}	Minimum GSR pulse width	All devices	-	19.8	ns
T_{RRI}	Delay from GSR input to any Q(2)	XQR4013XL	-	15.9	ns
		XQR4036XL	-	22.5	ns
		XQR4062XL	-	29.1	ns
Propagation Delays					
T_{PID}	Pad to I1, I2	All devices	-	1.6	ns
T_{PLI}	Pad to I1, I2 via transparent input latch, no delay	All devices	-	3.1	ns
T_{PFLI}	Pad to I1, I2 via transparent FCL and input latch, no delay	All devices	-	3.7	ns
T_{IKRI}	Clock (IK) to I1, I2 (flip-flop)	All devices	-	1.7	ns
T_{IKLI}	Clock (IK) to I1, I2 (latch enable, active Low)	All devices	-	1.8	ns
T_{OKLI}	FCL enable (OK) active edge to I1, I2 (via transparent standard input latch)	All devices	-	3.6	ns

Notes:
1. IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch
2. Indicates Minimum Amount of Time to Assure Valid Data.

XQR4000XL IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values are expressed in nanoseconds unless otherwise noted.

Symbol	Description	-3		Units
		Min	Max	
Clocks				
T_{CH}	Clock High	3.0	-	ns
T_{CL}	Clock Low	3.0	-	ns
Propagation Delays				
T_{OKPOF}	Clock (OK) to pad	-	5.0	ns
T_{OPF}	Output (O) to pad	-	4.1	ns
T_{TSHZ}	High-Z to pad High-Z (slew-rate independent)	-	4.4	ns
T_{TSONF}	High-Z to pad active and valid	-	4.1	ns
T_{OFPF}	Output (O) to pad via fast output MUX	-	5.5	ns
T_{OKFPF}	Select (OK) to pad via fast MUX	-	5.1	ns
Setup and Hold Times				
T_{OOK}	Output (O) to clock (OK) setup time	0.5	-	ns
T_{OKO}	Output (O) to clock (OK) hold time	0	-	ns
T_{ECOK}	Clock Enable (EC) to clock (OK) setup time	0	-	ns
T_{OKEC}	Clock Enable (EC) to clock (OK) hold time	0.3	-	ns
Global Set/Reset				
T_{MRW}	Minimum GSR pulse width	19.8	-	ns
T_{RPO}	Delay from GSR input to any pad(2)			
	XQR4013XL	-	20.5	ns
	XQR4036XL	-	27.1	ns
	XQR4062XL	-	33.7	ns
Slew Rate Adjustment				
T_{SLOW}	For output SLOW option add	-	3.0	ns

Notes:
1. Output timing is measured at ~50% V_{CC} threshold, with 50 pF external capacitive loads.
2. Indicates Minimum Amount of Time to Assure Valid Data.

Pinouts

CB228 Package for XQR4013XL/4036XL/4062XL

Pin Name	CB228
GND	P1
BUFGP_TL_A16_GCK1_IO	P2
A17_IO	P3
IO	P4
IO	P5
TDI_IO	P6
TCK_IO	P7
IO	P8
IO	P9
IO	P10
IO	P11
IO	P12
IO	P13
GND	P14
IO_FCLK1	P15
IO	P16
TMS_IO	P17
IO	P18
IO	P19
IO	P20
IO	P21
IO	P22
IO	P23
IO	P24
IO	P25
IO	P26
GND	P27
VCC	P28
IO	P29
IO	P30
IO	P31
IO	P32
IO	P33
IO	P34
IO	P35
IO	P36
VCC	P37
IO	P38

CB228 Package for XQR4013XL/4036XL/4062XL *(Continued)*

Pin Name	CB228
IO	P39
IO	P40
IO_FCKL2	P41
GND	P42
IO	P43
IO	P44
IO	P45
IO	P46
IO	P47
IO	P48
IO	P49
IO	P50
IO	P51
IO	P52
IO	P53
BUFGS_BL_GCK2_IO	P54
M1	P55
GND	P56
M0	P57
VCC	P58
M2	P59
BUFGP_BL_GCK3_IO	P60
HDC_IO	P61
IO	P62
IO	P63
IO	P64
LDC_IO	P65
IO	P66
IO	P67
IO	P68
IO	P69
IO	P70
IO	P71
GND	P72
IO	P73
IO	P74
IO	P75
IO	P76
IO	P77
IO	P78

CB228 Package for XQR4013XL/4036XL/4062XL *(Continued)*

Pin Name	CB228
IO	P79
IO	P80
IO	P81
IO	P82
IO	P83
/ERR_INIT_IO	P84
VCC	P85
GND	P86
IO	P87
IO	P88
IO	P89
IO	P90
IO	P91
IO	P92
IO	P93
IO	P94
VCC	P95
IO	P96
IO	P97
IO	P98
IO	P99
GND	P100
IO	P101
IO	P102
IO	P103
IO	P104
IO	P105
IO	P106
IO	P107
IO	P108
IO	P109
IO	P110
IO	P111
BUFGS_BR_GCK4_IO	P112
GND	P113
DONE	P114
VCC	P115
/PROG	P116
D7_IO	P117
BUFGP_BR_GCK5_IO	P118

CB228 Package for XQR4013XL/4036XL/4062XL *(Continued)*

Pin Name	CB228
IO	P119
IO	P120
IO	P121
IO	P122
D6_IO	P123
IO	P124
IO	P125
IO	P126
IO	P127
IO	P128
GND	P129
IO	P130
IO	P131
IO	P132
IO	P133
D5_IO	P134
/CS0_IO	P135
IO	P136
IO	P137
IO	P138
IO	P139
D4_IO	P140
IO	P141
VCC	P142
GND	P143
D3_IO	P144
/RS_IO	P145
IO	P146
IO	P147
IO	P148
IO	P149
D2_IO	P150
IO	P151
VCC	P152
IO	P153
IO	P154
IO	P155
IO	P156
GND	P157
IO	P158

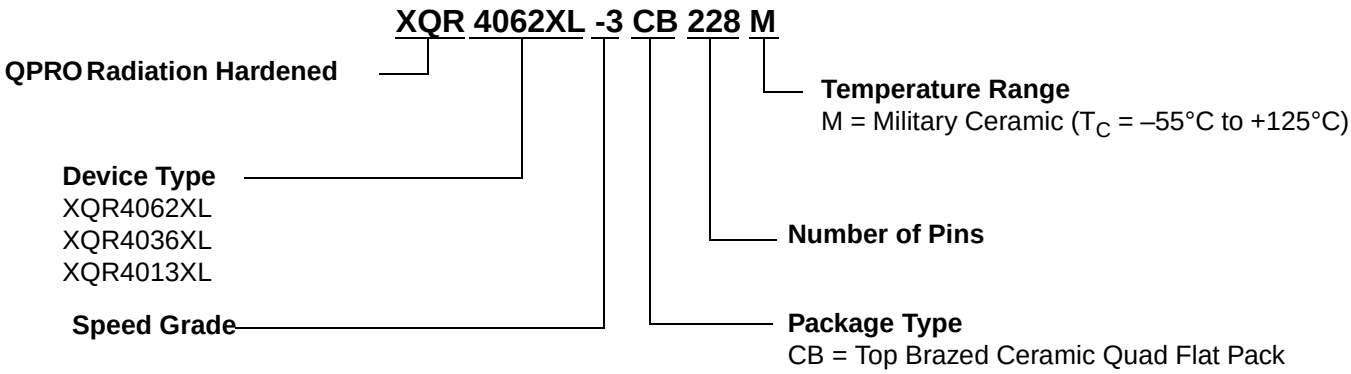
CB228 Package for XQR4013XL/4036XL/4062XL *(Continued)*

Pin Name	CB228
IO	P159
IO	P160
IO	P161
IO	P162
IO	P163
D1_IO	P164
BUSY_/RDY_RCLK_IO	P165
IO	P166
IO	P167
D0_DIN_IO	P168
BUFGS_TR_GCK6_DOUT_IO	P169
CCLK	P170
VCC	P171
TDO	P172
GND	P173
A0_/WS_IO	P174
BUFGP_TR_GCK7_A1_IO	P175
IO	P176
IO	P177
CSI_A2_IO	P178
A3_IO	P179
IO	P180
IO	P181
IO	P182
IO	P183
IO	P184
IO	P185
GND	P186
IO	P187
IO	P188
IO	P189
IO	P190
VCC	P191
A4_IO	P192
A5_IO	P193
IO	P194
IO	P195
A21_IO	P196
A20_IO	P197
A6_IO	P198

CB228 Package for XQR4013XL/4036XL/4062XL *(Continued)*

Pin Name	CB228
A7_IO	P199
GND	P200
VCC	P201
A8_IO	P202
A9_IO	P203
A19_IO	P204
A18_IO	P205
IO	P206
IO	P207
A10_IO	P208
A11_IO	P209
VCC	P210
IO	P211
IO	P212
IO	P213
IO	P214
GND	P215
IO	P216
IO	P217
IO	P218
IO	P219
A12_IO	P220
A13_IO	P221
IO	P222
IO	P223
IO	P224
IO	P225
A14_IO	P226
BUFGS_TL_GCK8_A15_IO	P227
VCC	P228

Ordering Information



Revision History

The following table shows the revision history for this document

Date	Version	Description
10/05/98	1.0	Original document release.
06/25/00	1.1	Updated format, added DS071 number. Updated timing specifications to match with commercial data sheet.

QPRO Series Configuration PROMs (XQ) including Radiation-Hardened Series (XQR)

DS062 (v2.0) June 1, 2000

Advance Product Specification

Features

- Configuration one-time programmable (OTP) read-only memory designed to store configuration bitstreams of Xilinx FPGA devices
- Simple interface to the FPGA; requires only one user I/O pin
- Cascadable for storing longer or multiple bitstreams
- Programmable reset polarity (active High or active Low) for compatibility with different FPGA solutions
- Supports XQR4000XL/Virtex fast configuration mode (15.0 MHz) (XQR1701L and XQR1704L)
- Supports XQ4000EX/XL fast configuration mode (15.0 MHz) (XQ1701L and XQ1704L)
- Fabricated on Epitaxial Silicon to improve latch performance (parts are immune to Single Event Latch-up) (XQR1701L and XQR1704L)
- QML certified
- Single Event Bit Upset immune (XQR1701L and XQR1704L)
- Total Dose tolerance in excess of 50K rads(Si) (XQR1701L and XQR1704L)
- All lots subjected to TID Lot Qualification in accordance with method 1019 (dose rate ~9.0 rads(Si)/sec) (XQR1701L and XQR1704L)
- Available in 44-pin ceramic LCC (M grade) package
- Available in 44-pin plastic chip carrier package (XQ1704L only)
- Available in 20-pin SOIC package (XQ1701L only)
- Programming support by leading programmer manufacturers.
- Design support using the Xilinx Alliance and Foundation series software packages.

Description

The QPRO™ series XQ1701L and XQ1704L are Xilinx 3.3V high-density configuration PROMs. The XQR1701L and XQR1704L are radiation hardened. These devices are manufactured on Xilinx QML certified manufacturing lines utilizing epitaxial substrates and TID lot qualification (per method 1019).

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the PROM. A short access time after the rising clock edge, data appears on the PROM DATA output pin that is connected to the FPGA D_{IN} pin. The FPGA generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the PROM. When the FPGA is in Slave Serial mode, the PROM and the FPGA must both be clocked by an incoming signal. Figure 1 shows a simplied block diagram.

Multiple devices can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the following device. The clock inputs and the DATA outputs of all PROMs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family.

For device programming, either the Xilinx Alliance or Foundation series development system compiles the FPGA design file into a standard Hex format, which is then transferred to most commercial PROM programmers.

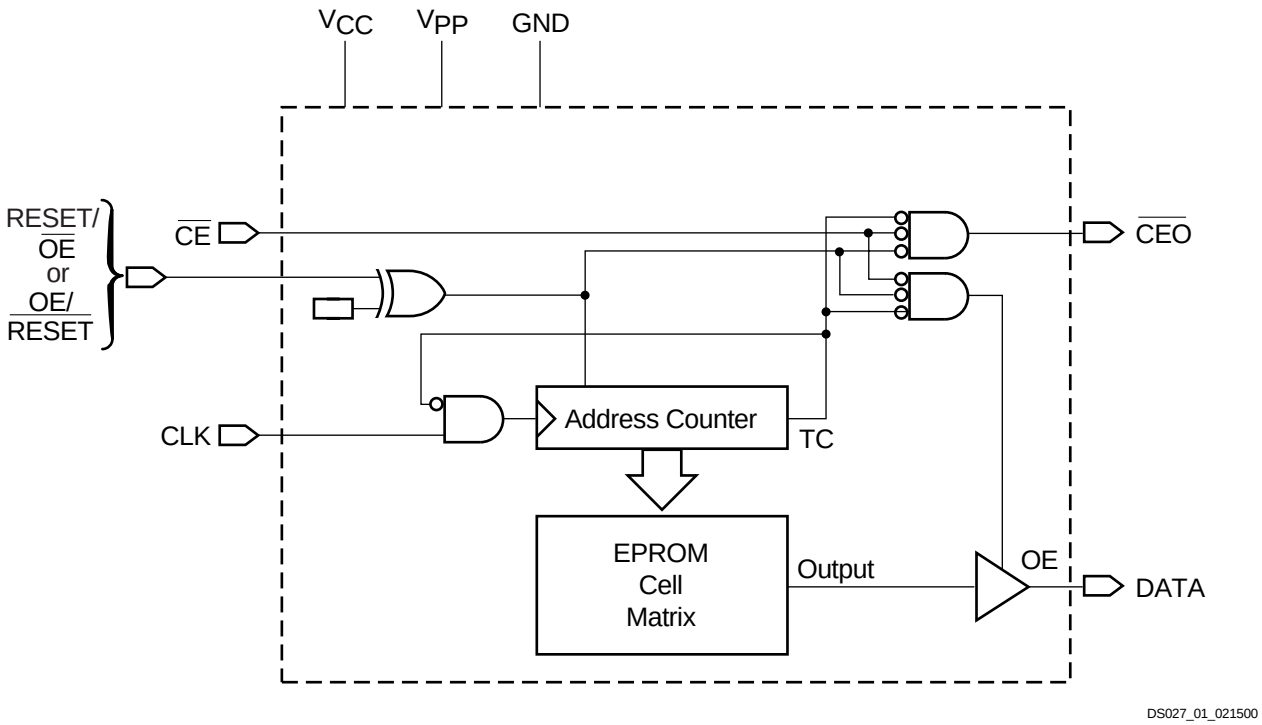


Figure 1: **Simplified Block Diagram (does not show programming circuit)**

Pin Description

DATA

Data output is in a high-impedance state when either $\overline{CE}$ or $\overline{OE}$ are inactive. During programming, the DATA pin is I/O. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

CLK

Each rising edge on the CLK input increments the internal address counter, if both $\overline{CE}$ and $\overline{OE}$ are active.

RESET/$\overline{OE}$

When High, this input holds the address counter reset and puts the DATA output in a high-impedance state. The polarity of this input pin is programmable as either RESET/$\overline{OE}$ or OE/$\overline{RESET}$. To avoid confusion, this document describes the pin as RESET/$\overline{OE}$, although the opposite polarity is possible on all devices. When RESET is active, the address counter is held at "0", and puts the DATA output in a high-impedance state. The polarity of this input is programmable. The default is active High RESET, but the preferred option is active Low $\overline{RESET}$, because it can be driven by the FPGAs $\overline{INIT}$ pin.

The polarity of this pin is controlled in the programmer interface. This input pin is easily inverted using the Xilinx HW-130 Programmer. Third-party programmers have different methods to invert this pin.

$\overline{CE}$

When High, this pin disables the internal address counter, puts the DATA output in a high-impedance state, and forces the device into low-I_{CC} standby mode.

$\overline{CEO}$

Chip Enable output, to be connected to the $\overline{CE}$ input of the next PROM in the daisy chain. This output is Low when the $\overline{CE}$ and $\overline{OE}$ inputs are both active AND the internal address counter has been incremented beyond its Terminal Count (TC) value. In other words: when the PROM has been read, $\overline{CEO}$ will follow $\overline{CE}$ as long as $\overline{OE}$ is active. When $\overline{OE}$ goes inactive, $\overline{CEO}$ stays High until the PROM is reset. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

V_{PP}

Programming voltage. No overshoot above the specified max voltage is permitted on this pin. For normal read operation, this pin must be connected to V_{CC}. Failure to do so may lead to unpredictable, temperature-dependent operation and severe problems in circuit debugging. Do not leave V_{PP} floating!

V_{CC} and GND

Positive supply and ground pins.

PROM Pinouts

Pin Name	44-Pin CLCC
DATA	2
CLK	5
RESET/$\overline{OE}$ (OE/$\overline{RESET}$)	19
$\overline{CE}$	21
GND	3, 24
$\overline{CEO}$	27
V_{PP}	41
V_{CC}	44

Capacity

Devices	Configuration Bits
XQR1704L	4,194,304
XQR1701L	1,048,576
XQ1704L	4,194,304
XQ1701L	1,048,576

Xilinx FPGAs and Compatible PROMs.

Device	Configuration Bits	PROM
XQR4013XL	393,632	XQ1701L
XQR4036XL	832,528	XQ1701L
XQR4062XL	1,433,864	XQ1704L
XQR4013XL	393,632	XQR1701L
XQR4036XL	832,528	XQR1701L
XQR4062XL	1,433,864	XQR1704L
XQVR300	1,751,840	XQR1704L
XQVR600	3,608,000	XQR1704L
XQVR1000	6,127,776	XQR1704L x 2

Controlling PROMs

Connecting the FPGA device with the PROM.

- The DATA output(s) of the of the PROM(s) drives the D_{IN} input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the PROM(s).
- The $\overline{CEO}$ output of a PROM drives the $\overline{CE}$ input of the next PROM in a daisy chain (if any).
- The $\overline{RESET}$/OE input of all PROMs is best driven by the $\overline{INIT}$ output of the lead FPGA device. This connection assures that the PROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V_{CC} glitch. Other methods—such as driving $\overline{RESET}$/OE from $\overline{LDC}$ or system reset—assume the PROM internal power-on-reset is always in step with the FPGAs internal power-on-reset. This may not be a safe assumption.
- The PROM $\overline{CE}$ input can be driven from either the $\overline{LDC}$ or DONE pins. Using $\overline{LDC}$ avoids potential contention on the D_{IN} pin.
- The $\overline{CE}$ input of the lead (or only) PROM is driven by the DONE output of the lead FPGA device, provided that DONE is not permanently grounded. Otherwise, $\overline{LDC}$ can be used to drive $\overline{CE}$, but must then be unconditionally High during user operation. $\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.

FPGA Master Serial Mode Summary

The I/O and logic functions of the Configurable Logic Block (CLB) and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Serial mode, the FPGA automatically loads the configuration program from an external memory. The Xilinx PROMs have been designed for compatibility with the Master Serial mode.

Upon power-up or reconfiguration, an FPGA enters the Master Serial mode whenever all three of the FPGA mode-select pins are Low (M0=0, M1=0, M2=0). Data is read from the PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial Mode provides a simple configuration interface. Only a serial data line and two control lines are required to configure an FPGA. Data from the PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function D_{IN} pin on the FPGA is used only for configuration, it must still be held at a defined level during normal operation. The Xilinx FPGA families take care of this automatically with an on-chip default pull-up resistor.

Programming the FPGA With Counters Unchanged Upon Completion

When multiple FPGA-configurations for a single FPGA are stored in a PROM, the $\overline{OE}$ pin should be tied Low. Upon power-up, the internal address counters are reset and configuration begins with the first program stored in memory. Since the $\overline{OE}$ pin is held Low, the address counters are left unchanged after configuration is complete. Therefore, to reprogram the FPGA with another program, the DONE line is pulled Low and configuration begins at the last value of the address counters.

This method fails if a user applies $\overline{RESET}$ during the FPGA configuration process. The FPGA aborts the configuration and then restarts a new configuration, as intended, but the PROM does not reset its address counter, since it never saw a High level on its $\overline{OE}$ input. The new configuration, therefore, reads the remaining data in the PROM and interprets it as preamble, length count etc. Since the FPGA is the master, it issues the necessary number of CCLK pulses, up to 16 million (2^{24}) and DONE goes High. However, the FPGA configuration will be completely wrong, with potential contentions inside the FPGA and on its output pins. This method must, therefore, never be used when there is any chance of external reset during configuration.

Cascading Configuration PROMs

For multiple FPGAs configured as a daisy-chain, or for future FPGAs requiring larger configuration memories, cascaded PROMs provide additional memory. After the last bit from the first PROM is read, the next clock signal to the PROM asserts its $\overline{CEO}$ output Low and disables its DATA line. The second PROM recognizes the Low level on its $\overline{CE}$ input and enables its DATA output. See Figure 2.

After configuration is complete, the address counters of all cascaded PROMs are reset if the FPGA $\overline{RESET}$ pin goes Low, assuming the PROM reset polarity option has been inverted.

To reprogram the FPGA with another program, the DONE line goes Low and configuration begins where the address counters had stopped. In this case, avoid contention between DATA and the configured I/O use of D_{IN}.

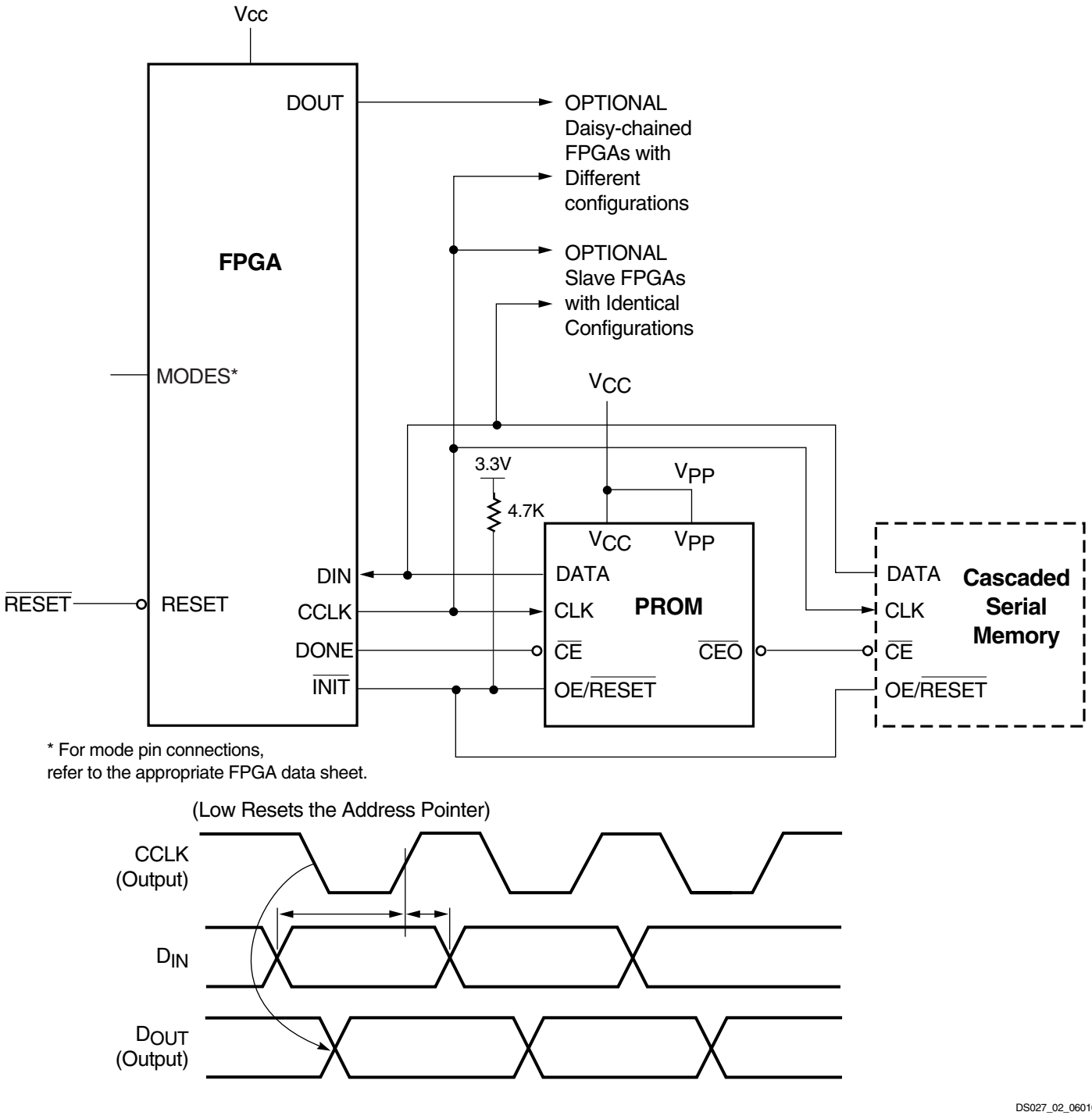


Figure 2: **Master Serial Mode.** The one-time-programmable PROM supports automatic loading of configuration programs. Multiple devices can be cascaded to support additional FPGAs. An early DONE inhibits the PROM data output one CCLK cycle before the FPGA I/Os become active.

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{CE}$ is asserted High. The output remains in a high-impedance state regardless of the state of the $\overline{OE}$ input.

Programming

The devices can be programmed on programmers supplied by Xilinx or qualified third-party vendors. The user must ensure that the appropriate programming algorithm and the latest version of the programmer software are used. The wrong choice can permanently damage the device.

Table 1: **Truth Table for Control Inputs**

Control Inputs		Internal Address	Outputs		
RESET	**$\overline{CE}$**		**DATA**	**$\overline{CEO}$**	**I_{CC}**
Inactive	Low	If address $\leq$ TC(1): increment If address > TC(1): don't change	Active High-Z	High Low	Active Reduced
Active	Low	Held reset	High-Z	High	Active
Inactive	High	Not changing	High-Z	High	Standby
Active	High	Held reset	High-Z	High	Standby

Notes:
1. The XC1700 RESET input has programmable polarity
1. TC = Terminal Count = highest address value. TC + 1 = address 0.

Radiation Characteristics (XQR1701L and XQR1704L only)

Symbol	Description	Min	Max	Units
TID	Total ionizing dose, Method 1019	50K		rads(Si)
SEL	Single event latch-up. Heavy ion saturation cross section, LET_1 > 120 MeV cm^2/mg		0	(cm^2/Device)
SEU	Single event bit upset. Heavy ion saturation cross section LET > 120 MeV cm^2/mg		0	(cm^2/Bit)
$SEFI_2$	Single event functional interupt, Heavy ion saturation cross section, 10% saturated intercept at LET = 6.0 MeV cm^2/mg		$1.2e^{-5}$	(cm^2/Device)

Notes:
1. Single Event Effects testing was performed with heavy ion to a maximum LET of 120 MeV-cm^2/mg.
2. For more information on Single Event Effects and mitigation methods refer to Xilinx Application Note XAPP185 "Space Application Design techniques for the XQR1700L QPRO Series Radiation Hardened Serial PROMs."

Absolute Maximum Ratings

Symbol	Description	Conditions	Units
V_{CC}	Supply voltage relative to GND	–0.5 to +4.0	V
V_{PP}	Supply voltage relative to GND	–0.5 to +12.5	V
V_{IN}	Input voltage relative to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to High-Z output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in.)	+260	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}(1)	Supply voltage relative to GND ceramic package (T_C = –55°C to +125°C)	Military	3.0	3.6	V

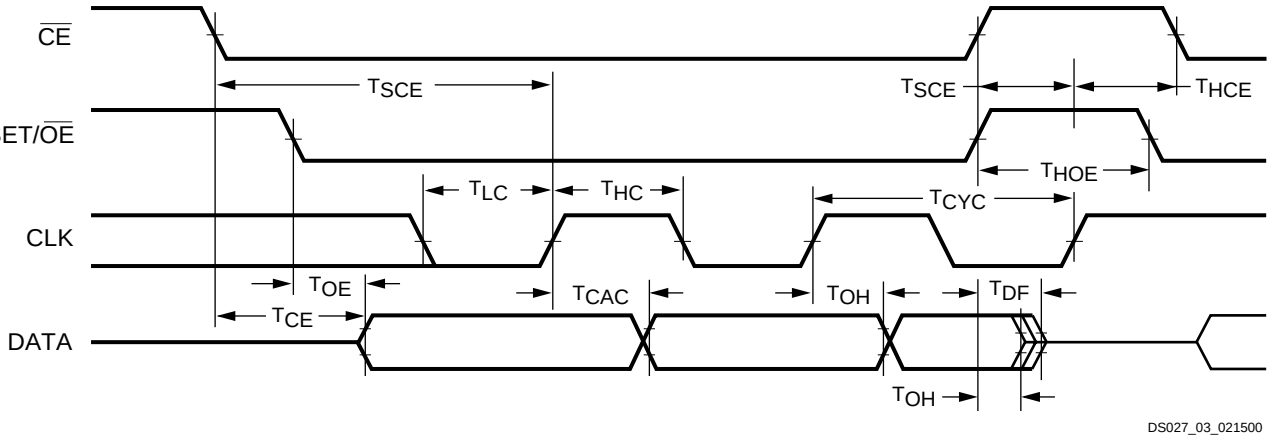
Notes:
1. During normal read operation V_{PP} MUST be connect to V_{CC}.

DC Characteristics Over Operating Condition

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = –3 mA)		2.4	-	V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)		-	0.4	V
I_{CCA}	Supply current, active mode (at maximum frequency)		-	10	mA
I_{CCS}	Supply current, standby mode (XQ1701L, XQ1704L)		-	100	µA
I_{CCS}(1)	Supply current, standby mode (XQR1701L and XQR 1704L)	Pre-rad (TID)	-	300	µA
		Post-rad (TID)	-	3	mA
I_L	Input or output leakage current		–10	10	µA
C_{IN}	Input capacitance (V_{IN} = GND, f = 1.0 MHz)		-	10	pF
C_{OUT}	Output capacitance (V_{IN} = GND, f = 1.0 MHz)		-	10	pF

Notes:
1. I_{CCS}, Standby Current is measured at +125°C for pre-radiation specifications and at room temperature for post-radiation specifications.

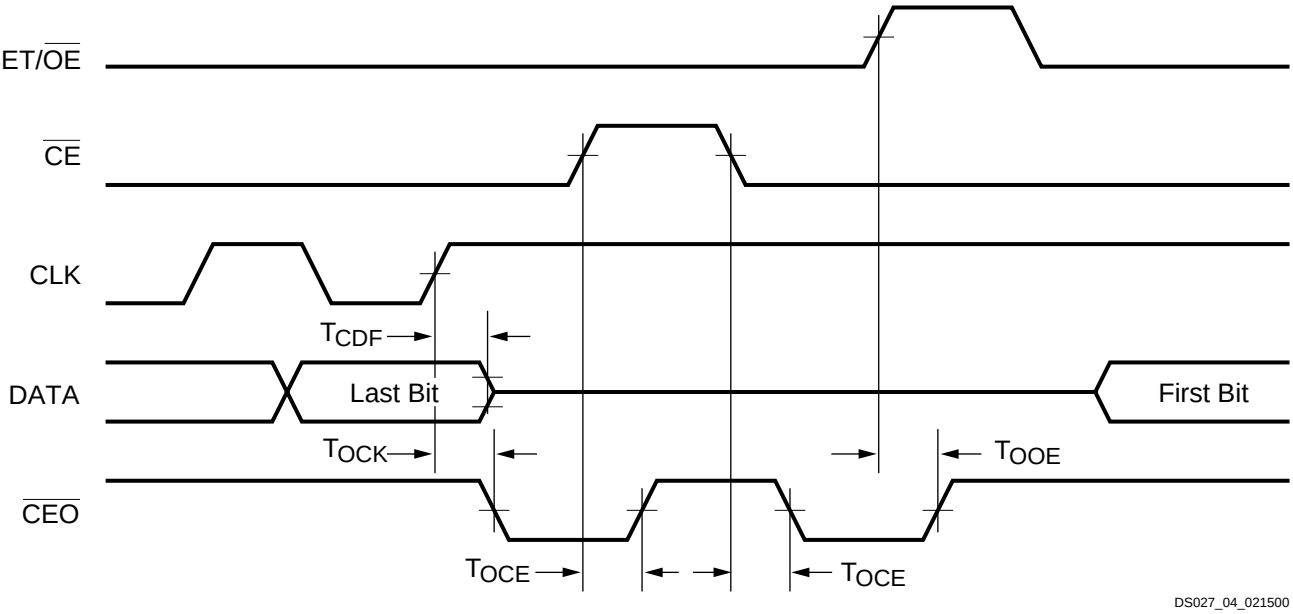
AC Characteristics Over Operating Condition



Symbol	Description	XQR1701L		XQ1701L, XQR1704L		Units
		Min	Max	Min	Max	
T_{OE}	$\overline{OE}$ to data delay	-	25	-	30	ns
T_{CE}	$\overline{CE}$ to data delay	-	45	-	45	ns
T_{CAC}	CLK to data delay	-	45	-	45	ns
T_{DF}	$\overline{CE}$ or $\overline{OE}$ to data float delay(2,3)	-	50	-	50	ns
T_{OH}	Data hold from $\overline{CE}$, $\overline{OE}$, or CLK(3)	0	-	0	-	ns
T_{CYC}	Clock periods	67	-	67	-	ns
T_{LC}	CLK Low time(3)	20	-	25	-	ns
T_{HC}	CLK High time(3)	20	-	25	-	ns
T_{SCE}	$\overline{CE}$ setup time to CLK (to guarantee proper counting)	20	-	25	-	ns
T_{HCE}	$\overline{CE}$ hold time to CLK (to guarantee proper counting)	0	-	0	-	ns
T_{HOE}	$\overline{OE}$ hold time (guarantees counters are reset)	20	-	25	-	ns

Notes:
1. AC test load = 50 pF
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.

AC Characteristics Over Operating Condition When Cascading



Symbol	Description	Min	Max	Units
T_{CDF}	CLK to data float delay(2,3)	-	50	ns
T_{OCK}	CLK to $\overline{CEO}$ delay(3)	-	30	ns
T_{OCE}	$\overline{CE}$ to $\overline{CEO}$ delay(3)	-	35	ns
T_{OOE}	RESET/$\overline{OE}$ to $\overline{CEO}$ delay(3)	-	30	ns

Notes:
1. AC test load = 50 pF
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.

Ordering Information

XQR1701L CC44 M

Device Number

XQ1704L
XQ1701L
XQR1704L
XQR1701L

Package Type

CC44 = 44-pin Ceramic Chip Carrier
SO20 = 20-pin Plastic Small Outline Package
PC44 = 44-pin Plastic Chip Carrier

Operating Range/Processing

B = Military(T_C = –55° to +125°C) QML certified to MIL-PRF-38535
M = Military (T_C = –55° to +125°C) QML certified to MIL-PRF-38535
N = Military Plastic (T_J = –55° to +125°C)

Valid Ordering Combinations

XQR1704LCC44M	XQR1701LCC44M	XQ1701LCC44M	XQ1704LCC44M
		XQ1701LCC44B	XQ1704LCC44B
		XQ1701LSO20N	XQ1704LPC44N

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/20/00	1.0	Initial Release
06/01/00	2.0	Combined XQR1700L Rad-Hard and XQ1701L devices, added XQ1704L and updated format.

QPRO Family of XC1700D QML Configuration PROMs

DS070 (v2.1) June 1, 2000

Product Specification

Features

- Certified to MIL-PRF-38535 Appendix A QML (Qualified Manufacturer Listing.)
- Also available under the following Standard Microcircuit Drawings (SMD): 5962-94717 and 5962-95617.
- Configuration one-time programmable (OTP) read-only memory designed to store configuration bitstreams of Xilinx FPGA devices
- On-chip address counter, incremented by each rising edge on the clock input
- Simple interface to the FPGA requires only one user I/O pin
- Cascadable for storing longer or multiple bitstreams
- Programmable reset polarity (active High or active Low) for compatibility with different FPGA solutions
- Low-power CMOS EPROM process
- Available in 5V version only
- Programming support by leading programmer manufacturers.
- Design support using the Xilinx Alliance and Foundation series software packages.

Description

The XC1700D QPRO™ family of configuration PROMs provide an easy-to-use, cost-effective method for storing Xilinx FPGA configuration bitstreams.

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the PROM. A short access time after the rising clock edge, data appears on the PROM DATA output pin that is connected to the FPGA D_{IN} pin. The FPGA generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the PROM. When the FPGA is in Slave Serial mode, the PROM and the FPGA must both be clocked by an incoming signal.

Multiple devices can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the following device. The clock inputs and the DATA outputs of all PROMs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family.

For device programming, either the Xilinx Alliance™ or the Foundation™ series development systems compiles the FPGA design file into a standard HEX format which is then transferred to most commercial PROM programmers.

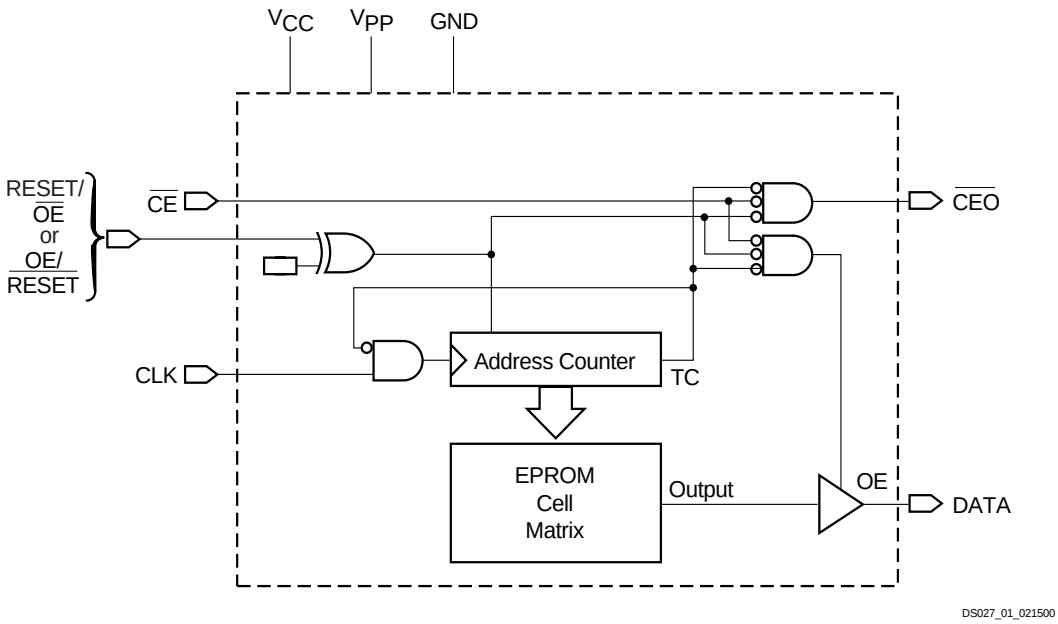


Figure 1: **Simplified Block Diagram (does not show programming circuit)**

Pin Description

DATA

Data output, 3-stated when either $\overline{CE}$ or $\overline{OE}$ are inactive. During programming, the DATA pin is I/O. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

CLK

Each rising edge on the CLK input increments the internal address counter, if both $\overline{CE}$ and $\overline{OE}$ are active.

RESET/$\overline{OE}$

When High, this input holds the address counter reset and 3-states the DATA output. The polarity of this input pin is programmable as either RESET/$\overline{OE}$ or OE/$\overline{RESET}$. To avoid confusion, this document describes the pin as RESET/$\overline{OE}$, although the opposite polarity is possible on all devices. When RESET is active, the address counter is held at zero, and the DATA output is put in a high-impedance state. The polarity of this input is programmable. The default is active High RESET, but the preferred option is active Low $\overline{RESET}$, because it can be driven by the FPGAs $\overline{INIT}$ pin.

The polarity of this pin is controlled in the programmer interface. This input pin is easily inverted using the Xilinx HW-130 programmer software. Third-party programmers have different methods to invert this pin.

CE

When High, this pin disables the internal address counter, 3-states the DATA output, and forces the device into low-I_{CC} standby mode.

CEO

Chip Enable output, to be connected to the $\overline{CE}$ input of the next PROM in the daisy chain. This output is Low when the $\overline{CE}$ and $\overline{OE}$ inputs are both active AND the internal address counter has been incremented beyond its Terminal Count (TC) value. In other words: when the PROM has been read, $\overline{CEO}$ will follow $\overline{CE}$ as long as $\overline{OE}$ is active. When $\overline{OE}$ goes inactive, $\overline{CEO}$ stays High until the PROM is reset. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

V_{PP}

Programming voltage. No overshoot above the specified max voltage is permitted on this pin. For normal read operation, this pin *must* be connected to V_{CC}. Failure to do so may lead to unpredictable, temperature-dependent operation and severe problems in circuit debugging. Do not leave V_{PP} floating!

V_{CC} and GND

V_{CC} is positive supply pin and GND is ground pin.

PROM Pinouts

Pin Name	8-pin
DATA	1
CLK	2
RESET/$\overline{OE}$ (OE/$\overline{RESET}$)	3
CE	4
GND	5
CEO	6
V_{PP}	7
V_{CC}	8

Capacity

Device	Configuration Bits
XC1736D	36,288
XC1765D	65,536
XC17128D	131,072
XC17256D	262,144

Number of Configuration Bits, Including Header for Xilinx FPGAs and Compatible PROMs

Device	Configuration Bits	PROM
XC3000/A series	14,819 to 94,984	XC1765D to XC17128D
XC4000 series	95,008 to 247,968	XC17128D to XC17256D
XQ4005E	95,008	XC17128D
XQ4010E	178,144	XC17256D
XQ4013E	247,968	XC17256D

Controlling PROMs

Connecting the FPGA device with the PROM.

- The DATA output(s) of the PROM(s) drives the D_{IN} input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the PROM(s).
- The $\overline{CEO}$ output of a PROM drives the $\overline{CE}$ input of the next PROM in a daisy chain (if any).
- The $\overline{RESET}$/OE input of all PROMs is best driven by the $\overline{INIT}$ output of the lead FPGA device. This connection assures that the PROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V_{CC} glitch. Other methods—such as driving $\overline{RESET}$/OE from $\overline{LDC}$ or system reset—assume the PROM internal power-on-reset is always in step with the FPGA's internal power-on-reset. This may not be a safe assumption.
- The PROM $\overline{CE}$ input can be driven from either the $\overline{LDC}$ or DONE pins. Using $\overline{LDC}$ avoids potential contention on the D_{IN} pin.
- The $\overline{CE}$ input of the lead (or only) PROM is driven by the DONE output of the lead FPGA device, provided that DONE is not permanently grounded. Otherwise, $\overline{LDC}$ can be used to drive $\overline{CE}$, but must then be unconditionally High during user operation. $\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.

FPGA Master Serial Mode Summary

The I/O and logic functions of the Configurable Logic Block (CLB) and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Serial mode, the FPGA automatically loads the configuration program from an external memory. The Xilinx PROMs have been designed for compatibility with the Master Serial mode.

Upon power-up or reconfiguration, an FPGA enters the Master Serial mode whenever all three of the FPGA mode-select pins are Low (M0=0, M1=0, M2=0). Data is read from the PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial Mode provides a simple configuration interface. Only a serial data line and two control lines are required to configure an FPGA. Data from the PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function D_{IN} pin on the FPGA is used only for configuration, it must still be held at a defined level during normal operation. Xilinx FPGAs take care of this automatically with an on-chip default pull-up resistor.

Programming the FPGA With Counters Unchanged Upon Completion

When multiple FPGA-configurations for a single FPGA are stored in a PROM, the $\overline{OE}$ pin should be tied Low. Upon power-up, the internal address counters are reset and configuration begins with the first program stored in memory. Since the $\overline{OE}$ pin is held Low, the address counters are left unchanged after configuration is complete. Therefore, to reprogram the FPGA with another program, the DONE line is pulled Low and configuration begins at the last value of the address counters.

This method fails if a user applies $\overline{RESET}$ during the FPGA configuration process. The FPGA aborts the configuration and then restarts a new configuration, as intended, but the PROM does not reset its address counter, since it never saw a High level on its $\overline{OE}$ input. The new configuration, therefore, reads the remaining data in the PROM and interprets it as preamble, length count etc. Since the FPGA is the master, it issues the necessary number of CCLK pulses, up to 16 million (2^{24}) and DONE goes High. However, the FPGA configuration will be completely wrong, with potential contentions inside the FPGA and on its output pins. This method must, therefore, never be used when there is any chance of external reset during configuration.

Cascading Configuration PROMs

For multiple FPGAs configured as a daisy-chain, or for future FPGAs requiring larger configuration memories, cascaded PROMs provide additional memory. After the last bit from the first PROM is read, the next clock signal to the PROM asserts its $\overline{CEO}$ output Low and disables its DATA line. The second PROM recognizes the Low level on its $\overline{CE}$ input and enables its DATA output. See Figure 2.

After configuration is complete, the address counters of all cascaded PROMs are reset if the FPGA $\overline{RESET}$ pin goes Low, assuming the PROM reset polarity option has been inverted.

To reprogram the FPGA with another program, the DONE line goes Low and configuration begins where the address counters had stopped. In this case, avoid contention between DATA and the configured I/O use of D_{IN}.

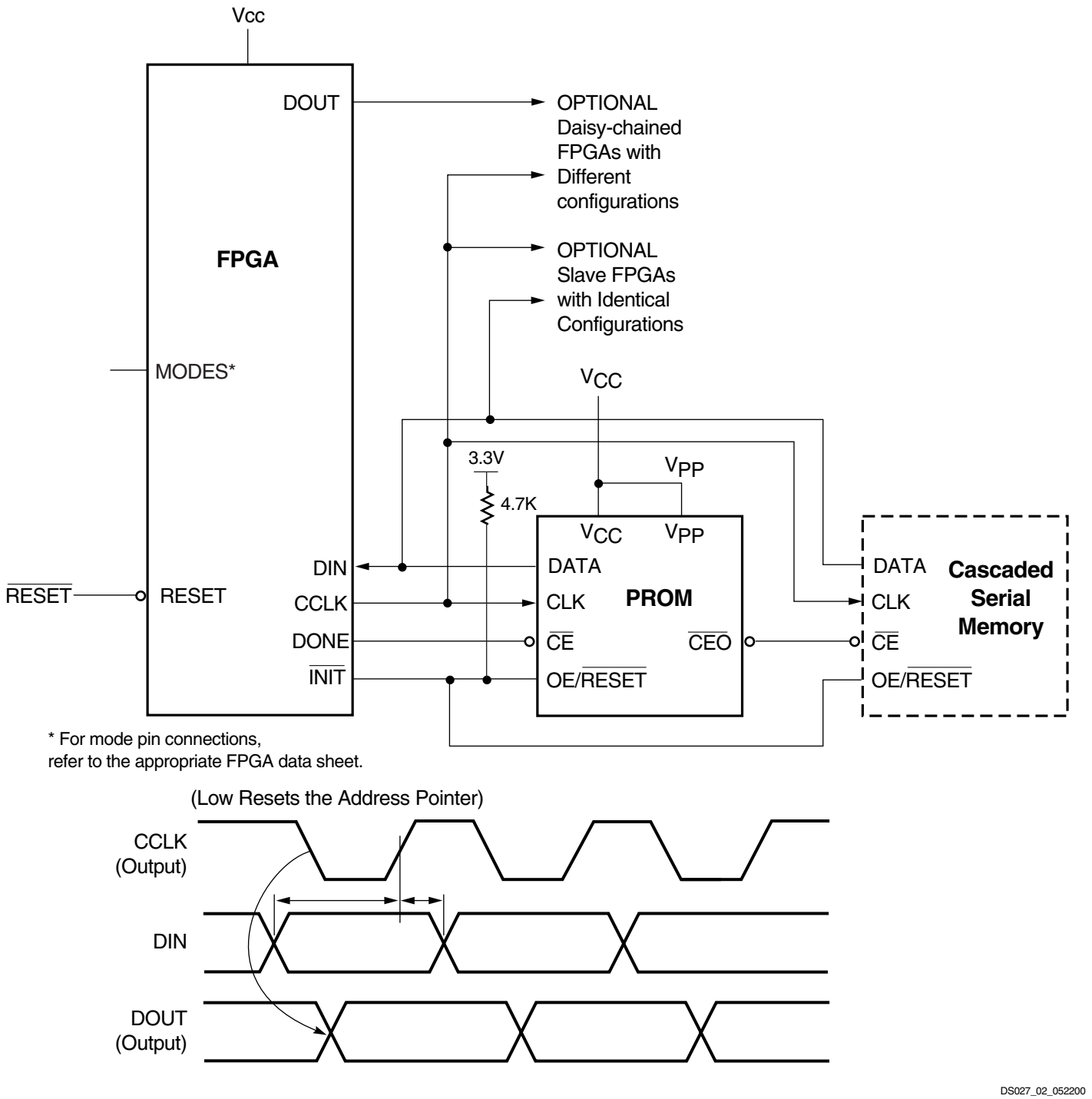


Figure 2: **Master Serial Mode.** The one-time-programmable PROM supports automatic loading of configuration programs. Multiple devices can be cascaded to support additional FPGAs. An early DONE inhibits the PROM data output one CCLK cycle before the FPGA I/Os become active.

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{CE}$ is asserted High. The output remains in a high impedance state regardless of the state of the $\overline{OE}$ input.

Programming

The devices can be programmed on programmers supplied by Xilinx or qualified third-party vendors. The user must ensure that the appropriate programming algorithm and the latest version of the programmer software are used. The wrong choice can permanently damage the device.

Table 1: **Truth Table for XC1700 Control Inputs**

Control Inputs		Internal Address	Outputs		
RESET	**CE**		**DATA**	**CEO**	**I_{CC}**
Inactive	Low	If address ≤ TC: increment If address > TC: don't change	Active High-Z	High Low	Active reduced
Active	Low	Held reset	High-Z	High	Active
Inactive	High	Not changing	High-Z	High	Standby
Active	High	Held reset	High-Z	High	Standby

Notes:
1. The XC1700 RESET input has programmable polarity
2. TC = Terminal Count = highest address value. TC + 1 = address 0.

Important: Always tie the V_{PP} pin to V_{CC} in your application. Never leave V_{PP} floating.

XC1736D, XC1765D, XC17128D and XC17256D

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{PP}	Supply voltage relative to GND	–0.5 to +12.5	V
V_{IN}	Input voltage relative to GND	–0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to High-Z output	–0.5 to V_{CC} + 0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in.)	+260	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

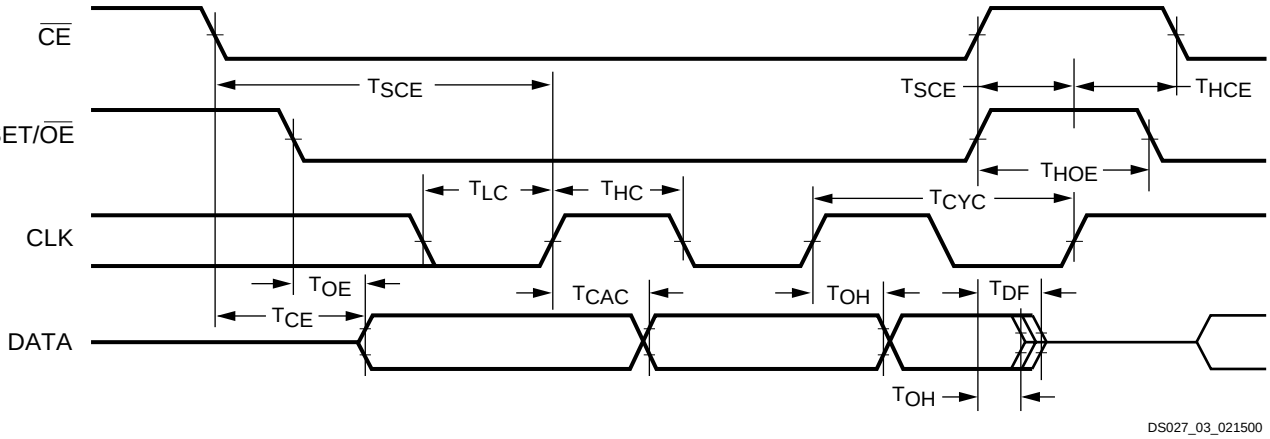
Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND (T_C = –55°C to +125°C)	Military	4.50	5.50	V

Note: During normal read operation V_{PP} *must* be connected to V_{CC}

DC Characteristics Over Operating Condition

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = –4 mA)	Military	3.7	-	V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)		-	0.4	V
I_{CCA}	Supply current, active mode (at maximum frequency)		-	10	mA
I_{CCS}	Supply current, standby mode	XC17128D, XC17256D	-	50	µA
		XC1736D, XC1765D	-	1.5	mA
I_L	Input or output leakage current		–10	10	µA
C_{IN}	Input capacitance (V_{IN} = GND, f = 1.0 MHz) sample tested		-	10	pF
C_{OUT}	Output capacitance (V_{IN} = GND, f = 1.0 MHz) sample tested		-	10	pF

AC Characteristics Over Operating Condition[1,2]

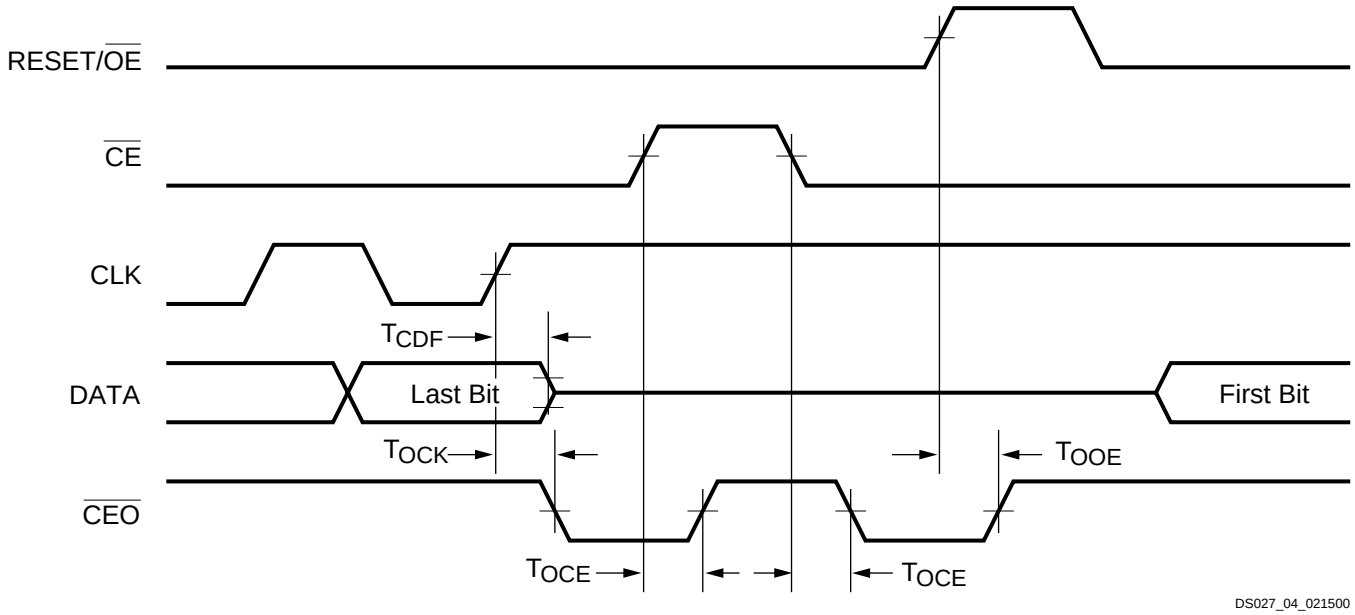


2

Symbol	Description	XC1736D XC1765D		XC17128D XC17256D		Units
		Min	Max	Min	Max	
T_{OE}	$\overline{OE}$ to data delay	-	45	-	25	ns
T_{CE}	$\overline{CE}$ to data delay	-	60	-	45	ns
T_{CAC}	CLK to data delay	-	150	-	50	ns
T_{OH}	Data hold from $\overline{CE}$, $\overline{OE}$, or CLK(3)	0	-	0	-	ns
T_{DF}	$\overline{CE}$ or $\overline{OE}$ to data float delay(3,4)	-	50	-	50	ns
T_{CYC}	Clock periods	200	-	80	-	ns
T_{LC}	CLK Low time(3)	100	-	20	-	ns
T_{HC}	CLK High time(3)	100	-	20	-	ns
T_{SCE}	$\overline{CE}$ setup time to CLK (to guarantee proper counting)	25	-	20	-	ns
T_{HCE}	$\overline{CE}$ hold time to CLK (to guarantee proper counting)	0	-	0	-	ns
T_{HOE}	$\overline{OE}$ hold time (guarantees counters are reset)	100	-	20	-	ns

Notes:
1. AC test load = 50 pF
2. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
3. Guaranteed by design, not tested.
4. Float delays are measured with 5 pF AC loads. Transition is measured at ±200mV from steady state active levels.

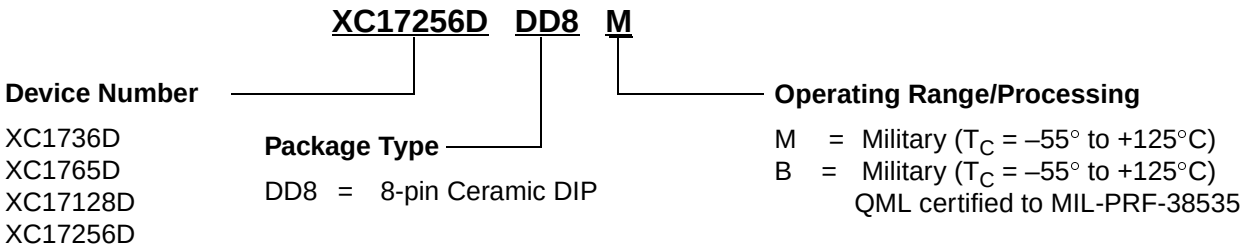
AC Characteristics Over Operating Condition When Cascading(1,2)



Symbol	Description	XC1736D XC1765D		XC17128D XC17256D		Units
		Min	Max	Min	Max	
T_{CDF}	CLK to data float delay(3,4)	-	50	-	50	ns
T_{OCK}	CLK to $\overline{CEO}$ delay(3)	-	65	-	30	ns
T_{OCE}	CE to $\overline{CEO}$ delay(3)	-	45	-	35	ns
T_{OOE}	RESET/$\overline{OE}$ to $\overline{CEO}$ delay(3)	-	40	-	30	ns

Notes:
1. AC test load = 50 pF
2. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
3. Guaranteed by design, not tested.
4. Float delays are measured with 5 pF AC loads. Transition is measured at ±200mV from steady state active levels.

Ordering Information

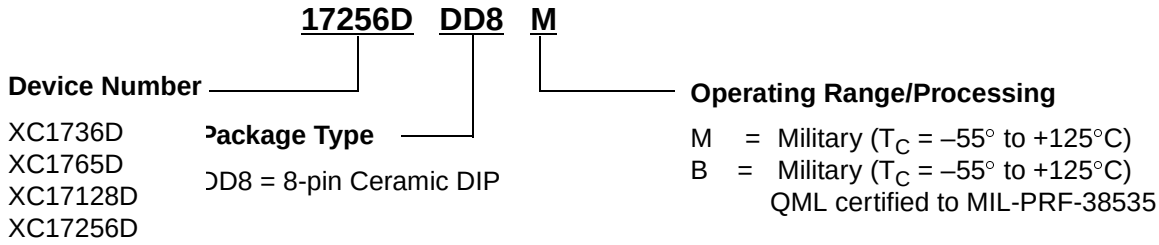


Valid Ordering Combinations

XC17128DDD8M	XC17256DDD8M	XC1736DDD8M	XC1765DDD8M
	5962-9561701MPA		5962-9471701MPA

Marking Information

Due to the small size of the PROM package, the complete ordering part number cannot be marked on the package. The XC prefix is deleted and the package code is simplified. Device marking is as follows.



Revision History

The following table shows the revision history for this document

Date	Version	Revision
02/08/99	2.0	Removed the now obsolete Commercial and Industrial Grade part numbers and design support.
06/01/00	2.1	Updated format and assigned data sheet number (DS070).

QPRO Application Notes Table of Contents

XAPP151 (v1.4) June 15, 2000

Virtex Series Configuration Architecture User Guide

Summary

The Virtex™ architecture supports powerful new configuration modes, including partial reconfiguration. These mechanisms are designed to give advanced applications access to and manipulation of on-chip data through the configuration interfaces.

This document is an overview of the Virtex architecture, emphasizing data bit location in the configuration bitstream. Knowing bit locations is the basis for accessing and altering on-chip data. FPGA applications can be built that change or examine the functionality of the operating circuit without stopping the circuit loaded in the device. A glossary is included to explain some of the terminology used in this application note.

3

Introduction

CLBs, IOBs, and Configurations

Each Virtex device contains configurable logic blocks (CLBs), input-output blocks (IOBs), block RAMs, clock resources, programmable routing, and configuration circuitry (Figure 1). These logic functions are configurable through the configuration bitstream. Configuration bitstreams contain a mix of commands and data. Configuration bitstreams can be read and written through one of the configuration interfaces on the device.

The Virtex, Virtex-E, and Virtex-E Extended Memory (Virtex-EM) families differ primarily in the amount of block RAM available.

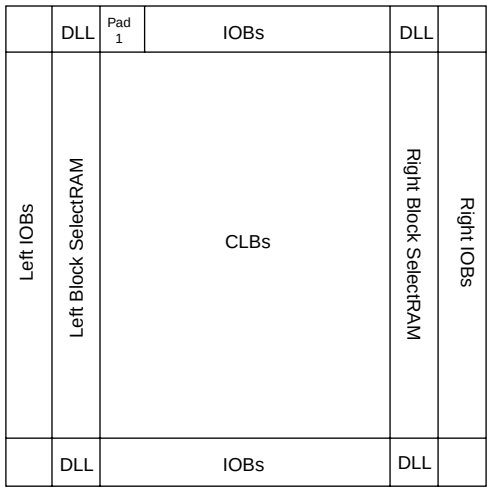


Figure 1: **Virtex Architecture Overview**

Configuring Virtex Devices

Virtex devices can be configured through the SelectMAP™ interface, master/slave serial interfaces, or the Boundary-Scan interface. The collection of configuration bits is called a configuration bitstream. The bitstream is a series of configuration commands and configuration data, as shown in Figure 2. Bitstream architecture is discussed in "Configuration Logic Basics" on page 16.

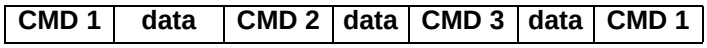


Figure 2: **Bitstream Example**

Warning! This document discusses mechanisms for manipulating the configuration bits for the Virtex devices. If portions of the bitstream other than those described here are altered, the device may be damaged. Xilinx is not liable for any consequences of misprogramming a device.

Writing some or all of a configuration is done by issuing configuration commands to the desired interface followed by the configuration data.

The SelectMAP interface is an 8-bit interface on the device with data pins labeled D[7:0]. The configuration bitstream can be written eight bits per clock cycle. Virtex devices can be configured to retain the (D[7:0], BUSY/DOUT, $\overline{\text{INIT}}$, $\overline{\text{WRITE}}$, and $\overline{\text{CS}}$) SelectMAP pins, allowing further re-configuration via those pins. If further re-configuration is not required, those pins can be configured as user I/O.

When the master/slave serial or Boundary Scan interface is used for configuration or re-onfiguration, the configuration bitstream is transmitted one bit per clock cycle.

Timing relationships for the configuration interfaces are discussed in the Virtex series data sheets located at **http://www.xilinx.com/products/virtex.htm**.

Reading Configuration Bits From a Virtex Device

Configuration data can be read using the SelectMAP interface or the Boundary Scan interface. The master/slave serial interfaces can not be used to read a configuration. Reading all or some of a configuration is done by issuing configuration read commands to the desired interface, then reading the data from the same interface. Configuration commands and data formats are discussed in "Configuration Logic Basics" on page 16.

The SelectMAP interface has an 8-bit data port. To use the SelectMAP interface after configuration, all 12 SelectMAP pins must remain as SelectMAP as opposed to user I/O (using the BitGen option: `-g Persist:Yes`).

The Boundary Scan (JTAG) interface allows bit-serial access to the configuration. It is a permanent interface that is always present.

Configuration Columns

The Virtex configuration memory can be visualized as a rectangular array of bits. The bits are grouped into vertical *frames* that are one-bit wide and extend from the top of the array to the bottom. A frame is the atomic unit of configuration - it is the smallest portion of the configuration memory that can be written to or read from.

Frames are grouped together into larger units called columns. In Virtex, Virtex-E, and Virtex-EM devices, there are several different types of columns:

Table 1: **Configuration Column Type**

Column Type	# of Frames	# per Device
Center	8	1
CLB	48	# of CLB columns
IOB	54	2
Block SelectRAM Interconnect	27	# of Block SelectRAM columns
Block SelectRAM Content	64	# of Block SelectRAM columns

Each device contains one center column that includes configuration for the four global clock pins. Two IOB columns represent configuration for all of the IOBs on the left and right edges of the device. The majority of columns are CLB columns which each contain one column of CLBs and the two IOBs above and below those CLBs. The remaining two column types involve the block RAM: one for content and the other for interconnect. For each RAM column, one of each type is present (for values for all Virtex devices, see Table 3, "Virtex Series Devices," on page 6).

The columns for an sample Virtex device are shown below:

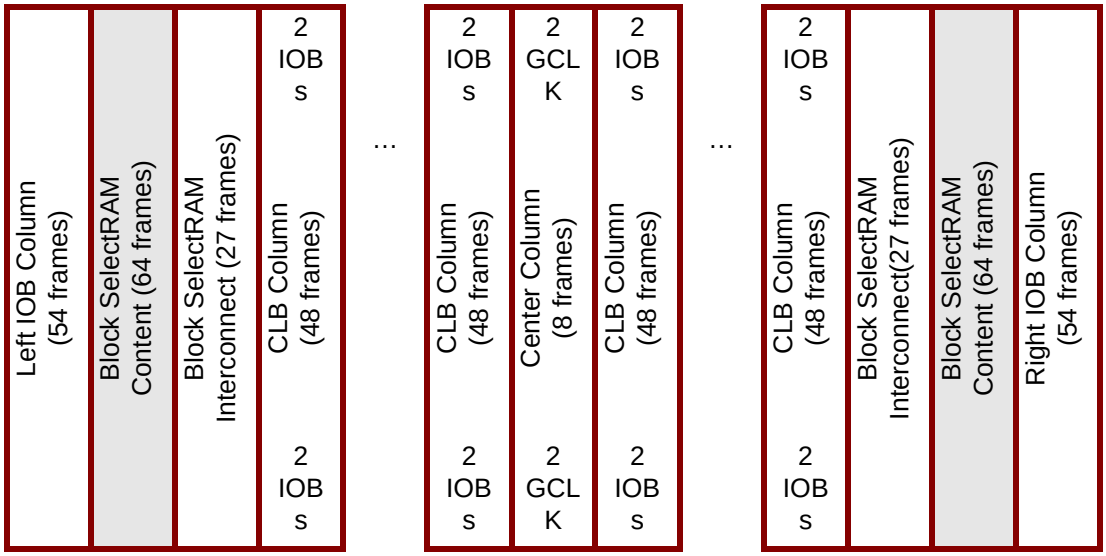


Figure 3: **Configuration Column Example (XCV50)**

Configuration Addressing

Block Type, Major Address, Minor Address

The total address space is divided into block types. There are two block types: RAM and CLB. The RAM type contains only the block SelectRAM content columns (not interconnect). The CLB type contains all other column types.

Both the RAM and CLB address spaces are subdivided into major and minor addresses. Each configuration column has a unique major address within the RAM or CLB space. Each configuration frame has a unique minor address within its column.

The numbering schemes for the block type and minor address are identical between Virtex, Virtex-E, and Virtex-EM devices. The major address numbering scheme differs between families and is encapsulated in Table 2. But in both families, even major addresses are on the left half of the device while the odd major addresses are on the right half of the device.

Table 2: **Major Addressing Scheme by Family**

Column Type	Block Type	Virtex	Virtex-E	Virtex-EM
First MJA	CLB	0	0	0
	RAM	0	1	1
MJA Order	CLB	1: Center 2: CLB 3: IOB 4: BRAM Interconnect	1: Center 2: CLB / BRAM Interconnect 3: IOB	1: Center 2: CLB 3: IOB 4: BRAM Interconnect
	RAM	BRAM Content	BRAM Content	BRAM Content

Virtex Major Addresses

The CLB address space begins with "0" for the center column and alternates between the right and left halves of the device for all the CLB columns, then IOB columns, and finally block SelectRAM interconnect columns.

The RAM address space has "0" for the left block SelectRAM content column and "1" for the right column.

A XCV50 is shown in Figure 4. The shaded columns are in the RAM address space.

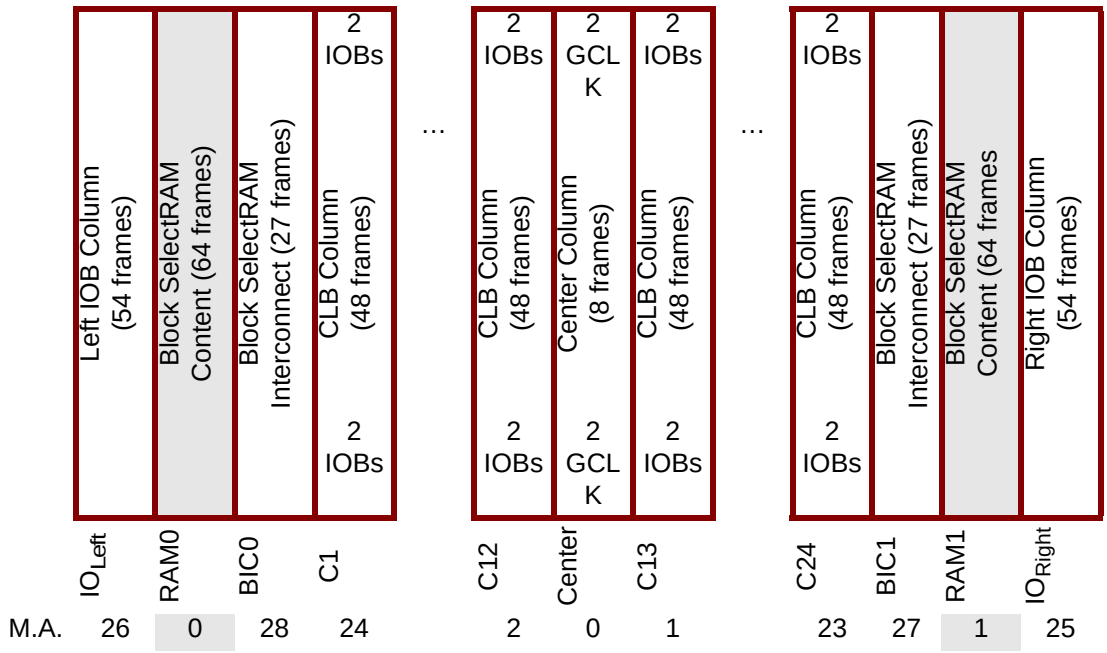


Figure 4: **Virtex Family: Allocation of Frames to Device Resources (XCV50)**

Virtex-EM Major Addresses

The Virtex-EM family has the same numbering as the Virtex family but the block SelectRAM content columns begin with "1".

Virtex-E Major Addresses

The Virtex-E family has block SelectRAM interspersed between CLB columns. Both the CLB and RAM major addressing have been changed to allow for this.

The CLB address space again begins with "0" for the center column and alternates between the right and left sides of the device for CLB columns *and* block SelectRAM interconnect columns and finally IOB columns. The difference is that in Virtex-E devices, the block

SelectRAM interconnect appear in the middle of the CLB addresses while in the Virtex and Virtex-EM families, they appear at the very end after the IOB columns. Also, note that the block SelectRAM content columns begin with "1" (Virtex devices begin with "0").

A XCV50E is shown in Figure 5. The shaded columns are in the RAM address space.

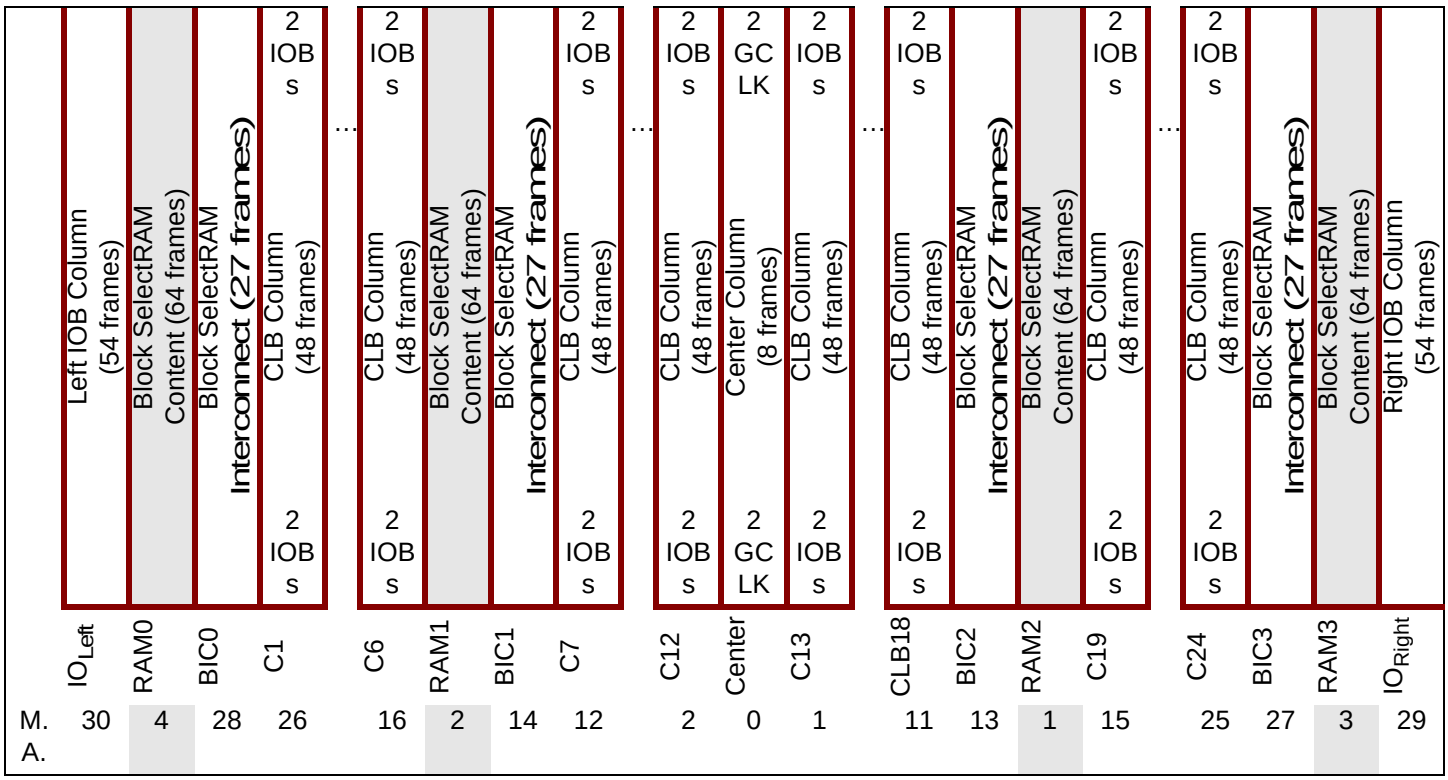


Figure 5: **Virtex-E Family: Allocation of Frames to Device Resources (XCV50E)**

Frames

Frames are read and written sequentially with ascending addresses for each operation. Multiple consecutive frames can be read or written with a single configuration command. The smallest amount of data that can be read or written with a single command is a single frame. The entire CLB array plus the IOBs and block SelectRAM interconnect can be read or written with a single command. Each block SelectRAM Content must be read or written separately.

Frame Sizes

Frame size depends on the number of rows in the device. The number of configuration bits in a frame is 18 × (# CLB_rows+2) and is padded with zeroes on the right (bottom) to fit in 32-bit words. <Link>"Frame Organization" for more details. An additional padding word is needed at the end of each frame for pipelining. Table 3 shows the frame sizes for all Virtex devices. This table also shows the size, in words, of the bitstream for the CLB address space and the number of words in each RAM block.

Table 3: **Virtex Series Devices**

Device	Row × Col.	Bits/ Frame	Words/ Frame	Virtex			Virtex-E			
					# of 32-bit Read-back Words (1)				# of 32-bit Read-back Words (1)	
				RAM Cols	CLB (all)	RAM (1 col)	RAM Cols	RAM Space	CLB (all)	RAM (1 col)
XCV50	16 × 24	384	12	2	15,876	780	-	-	-	-
XCV50E	16 × 24	384	12	-	-	-	4	6	16,524	780
XCV100	20 × 30	448	14	2	22,554	910	-	-	-	-
XCV100E	20 × 30	448	14	-	-	-	4	12	23,310	910
XCV150	24 × 36	512	16	2	30,384	1,040	-	-	-	-
XCV200	28 × 42	576	18	2	39,366	1,170	-	-	-	-
XCV200E	28 × 42	576	18	-	-	-	4	12	40,338	1,170
XCV300	32 × 48	672	21	2	51,975	1,365	-	-	-	-
XCV300E	32 × 48	672	21	-	-	-	4	12	53,109	1,365
XCV400	40 × 60	800	25	2	76,275	1,625	-	-	-	-
XCV400E	40 × 60	800	25	-	-	-	4	12	77,625	1,625
XCV405E	40 × 60	800	25	-	-	-	14	4	84,375	1,625
XCV600	48 × 72	960	30	2	108,810	1,950	-	-	-	-
XCV600E	48 × 72	960	30	-	-	-	6	12	112,050	1,950
XCV800	56 × 84	1088	34	2	142,902	2,210	-	-	-	-
XCV812E	56 × 84	1088	34	-	-	-	20	4	159,426	2,210
XCV1000	64 × 96	1248	39	2	186,381	2,535	-	-	-	-
XCV1000E	64 × 96	1248	39	-	-	-	6	12	190,593	2,535
XCV1600E	72 × 108	1376	43	-	-	-	8	12	237,231	2,795
XCV2000E	80 × 120	1536	48	-	-	-	8	12	292,464	3,120
XCV2600E	92 × 138	1728	54	-	-	-	8	12	375,678	3,510
XCV3200E	104 × 156	1952	61	-	-	-	8	12	477,081	3,965

Notes:
1. Includes pad frame in calculation.

Frame Organization

Each frame sits vertically in the device, with the “front” of the frame at the top. As shown in Figure 6, it is convenient to consider the frame horizontally when it is viewed as part of a bitstream. The top IOBs are shown on the left followed by the CLBs in the column and the bottom IOBs on the right. Bits in frames are allocated as follows.

For CLB columns, the first 18 bits control the two IOBs at the top of the column; then 18 bits are allocated for each CLB row; finally, the next 18 bits control the two IOBs at the bottom of the

CLB column. The frame then contains enough “pad” bits to make it an integral multiple of 32 bits.

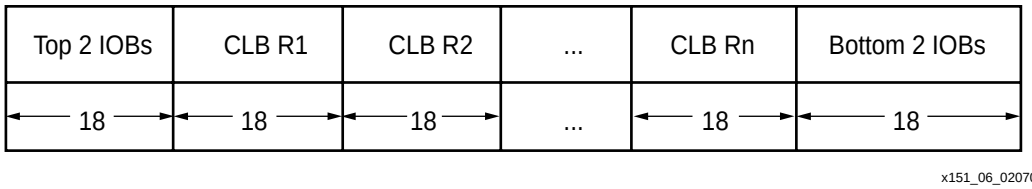


Figure 6: **CLB Column Frame Organization**

For IOB columns, the frame allocates 18 bits per three IOB rows, Figure 7. When reading and writing frames, bits are grouped into 32-bit words, starting on the left (corresponding to the top of the device). If the last word does not completely fill a 32-bit word, it is padded on the right with zeroes.

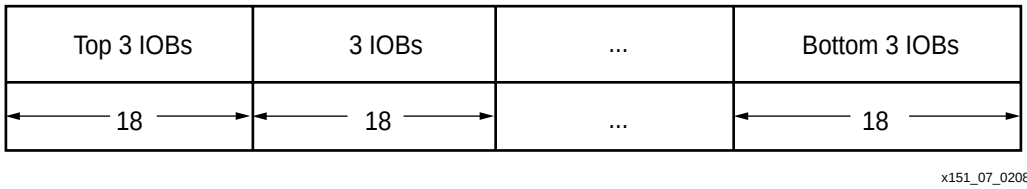


Figure 7: **IOB Column Frame Organization**

For block SelectRAM content columns (Figure 8), the first 18 bits are pad bits; then 72 bits are allocated for each RAM row; finally, there are another 18 pad bits. The frame then adds enough “pad” bits to make it an integral multiple of 32 bits.

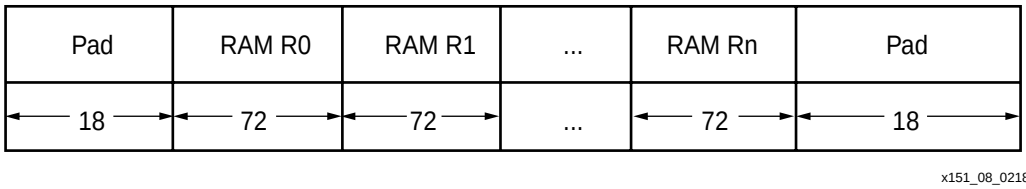


Figure 8: **Block SelectRAM Content Column Frame Organization**

Location of LUT SelectRAM Bits

With respect to the beginning of a configuration frame, relative locations of LUT SelectRAM bits within the bitstream are the same for every CLB slice. The bits of a LUT SelectRAM are spread across 16 consecutive frame Minor Addresses. Each frame Minor Address contains all instances of a single bit index for that column. These 16 frames contain all 16 bits of the LUT SelectRAM for a column of CLB slices. You must read or write the 16 frames containing those bits to read or write the entire LUT SelectRAM.

Note: LUT SelectRAM bits are stored inverted. Flip-Flop data are stored in their true sense. When reading or writing LUT SelectRAM data from the bitstream, it is negated from the logic sense of the data. For example, a 4-input AND gate has the truth table LUT[15:0] = 1000000000000000.

This truth table is stored internally in the LUT SelectRAM as $\overline{\text{LUT}}$[15:0] = 0111111111111111. Of course, user logic reading the data from the LUT SelectRAM would read the correct logic value, LUT[15:0] = 1000000000000000.

Configuration Data Operations

Reading Configuration Data

Configuration information can be read from the Virtex devices if readback is enabled in the current configuration. (See the description of the Control Register field SBITS on page 21.) CLB and IOB configuration data can be read while the device is operating.

When reading data from a Virtex device, a pad frame is read before any of the data frames. This is in addition to the pad word in each data frame. The pad frame must be included in the word count to be read from the device.

Each frame read from the device consists of the number of words shown in Table 3.

For example, the XCV150 has 16-word frames. When reading frames, the first word of a frame is a pad word. Including the pad frame, the XCV150 has 1,899 (30,384/16) frames. (See Figure 9.)

Pad Frame (16 words)	
Pad Word	Data Frame 0 (15 words)
⋮	⋮
Pad Word	Data Frame n (15 words)

Figure 9: **XCV150 Frame Padding for Device Read**

Writing Configuration Data

Configuration information can be written to a Virtex device while the device is running if writing is enabled in the current configuration. (See the Control Register field SBITS in Table 23.) Re-writing the same configuration data does not generate any transient signals.

Changing configuration data may generate transient signals, especially if LUT values or signal routing is changed. For this case, all the logic cells and routing can be placed in a non-contentious state by asserting the GHIGH_B signal. See the description for the "Command Register (CMD)" on page 18,

When writing configuration data to the Virtex device, whether from the SelectMAP or JTAG interfaces, the data frames are written to the device with each frame followed by a pad word. After all the data frames are written, a pad frame must be written (to flush internal pipelines). The pad words and pad frame must be included in the number of words to be written to the device. (Table 3.)

For example, the XCV1000 has 39-word frames. When writing frames, the last word of the frame is a pad word. Including the pad frame, the XCV1000 has 4,779 (186,381/39) frames. See Figure 10.)

Data Frame 0 (38 words)	Pad Word
	⋮
Data Frame n (38 words)	Pad Word
Pad Frame (39 words)	

Figure 10: **XCV1000 Frame Padding for Device Write**

Altering Configuration Data

Virtex devices support the Read-Modify-Write (RMW) method of changing LUT SelectRAM data. Therefore, it is possible to read or alter the contents of one or more LUT SelectRAMs through the JTAG or SelectMAP interfaces. *When writing data to one or more LUT SelectRAMs, all the bits in the frame* ***must*** *have valid configuration information.* This can be assured by altering valid configurations from bitstream files or from frames read from a properly configured Virtex device. When using the RMW method, it may be expeditious to read the data, ignoring the pad frame and the pad word of only the first frame. This aligns the remaining

configuration data in the Device Write format. After modifying the configuration, the altered data can be written to the Virtex device followed by a pad word and a pad frame.

It is not necessary to retain the contents of the pad frame or pad words. However, pad words and pad frames **are** included in the CRC calculation.

Note: Frames span an entire column of CLB slices (or IOBs). Thus, when changing LUT SelectRAM bit 0 for a single CLB slice (*e.g.*, R3C4.S1), LUT SelectRAM bit 0 for *all* slices in that column (*i.e.*, R*C4.S1) is written with the same command. One must ensure that either all other data in the slice is constant or changed externally through partial configurations.

LUT SelectRAMs not configured externally should not lie in the same slice with LUTs or LUT SelectRAMs that are re-configured externally. Such a mixture can cause the unrelated LUT SelectRAM data to be re-configured when the frames are written to the device. Figure 11 shows what can happen if this restriction is not observed.

In this example, it is the objective to perform a Read-Modify-Write on the LUT SelectRAM in R2C3.S1 in column 3, which is shown in the first column in the figure. Row 2 contains a LUT containing the value `AB`. Row 3 contains a SelectRAM containing the value `C3`. Because the Read and Write operations operate on an entire frame, the RAM in R3C3.S1 is also read and written when R2C3.S1 is read and written. Performing the Readback operation reads all the LUT and SelectRAM values for the column. Before the new value for the LUT is written, it is possible for the on-chip circuitry to write a new value, such as `14`, into the SelectRAM. When the new value, `BD`, is written via the configuration interface into LUT R2C3.S1, the value `C3` is also written into RAM R3C3.S1. This may not always be desirable (It is design-dependent).

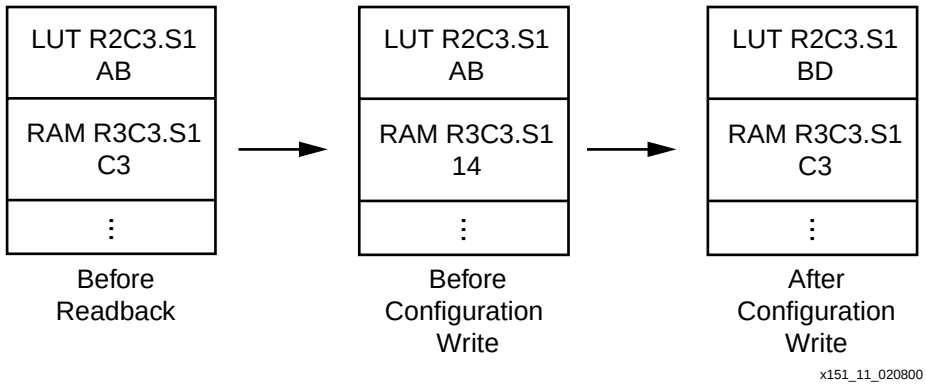


Figure 11: **Potential Write Conflicts**

Definitions

Two sets of variables are defined to determine where a desired bit is in the configuration data. The first is a set of “independent” variables, or design attributes, namely characteristics of the design that are known, i.e., the device size and which CLB and bit(s) within the CLB to locate, Table 4. The second set is a set of “dependent” variables or design variables, namely values that must be calculated to find the bit(s) of interest listed in Table 5.

Table 4: **Design Attributes (Independent Variables)**

Term	Definition
Chip_Cols	# of CLB columns on the Virtex device
Chip_Rows	# of CLB rows on the Virtex device
Chip_Rams	# of block SelectRAM columns on the Virtex device
RAM_Space	Spacing of block SelectRAM columns (in terms of CLB columns)
FL	# of 32-bit words in the frame.

Table 4: **Design Attributes (Independent Variables) *(Continued)***

Term	Definition
RW	1 for Read, 0 for Write
CLB_Col	Column number of the desired CLB
CLB_Row	Row number of the desired CLB
Slice	0 or 1
FG	0 for the F-LUT, 1 for the G-LUT
lut_bit	The desired bit from the given LUT. Bits in the LUT are indexed from 0 to 15.
XY	0 for the X Flip-Flop, 1 for the Y Flip-Flop
RAM_Col	Column number of the desired block SelectRAM
RAM_Row	Row number of the desired block SelectRAM
ram_bit	The desired bit from the given block SelectRAM. Bits are indexed from 0 to 4095.

Table 5: **Design Variables (Dependent Variables)**

Term	Definition
MJA	Frame Major Address
MNA	Frame Minor Address
fm_st_wd	The index of the word within a full configuration segment that corresponds to the starting word of the desired frame. A full configuration segment is defined as the following: 1) for CLB/IOB, all CLB, IOB, and RAM interconnect frames beginning at MJA=0, MNA=0 and 2) for block SelectRAM, all RAM content frames for the given RAM column. Words are numbered starting at 0.
fm_wd	The index of the 32-bit word within a frame that contains the desired bit. Words in a frame are numbered starting at 0.
fm_wd_bit_idx	The bit index of the desired bit within frame word fm_wd. Words are indexed in “big-endian” style, with bit 31 on the left and bit 0 on the right.
fm_bit_idx	Bit index within a frame of the desired bit. Numbered starting with 0 as the left-most (first) bit. Bit numbering within a frame continues across all the words in the frame.

Table 6: **Functions used in Equations**

Functions	Definition
floor(x)	The largest integer not larger than *x*. *E.g.*, floor(3.1) = 3, because the next largest integer, 4, is larger than 3.1, floor(3)=3.
ceiling(x)	The smallest integer greater than or equal to *x*. For example, ceiling(3.2) = 4, because 4 is greater than 3.2, and 3 is not, ceiling (4) = 4.
%	The modulus operation. 5 % 2 = 1, 5 % 3 = 2, 5 % 5 = 0.

CLB LUT SelectRAM Dependent Variables

Table 7 shows equations for the LUT SelectRAM "Dependent Variables" that were defined in Table 5.

Table 7: **Virtex Equations for LUT SelectRAM Dependent Variables**

Term	Definition
MJA	if (CLB_Col ≤ Chip_Cols/2), then Chip_Cols – CLB_Col × 2 + 2 else 2 × CLB_Col – Chip_Cols – 1
MNA	lut_bit + 32 – Slice × (2 × lut_bit + 17)
fm_bit_idx	3 + 18 × CLB_Row – FG + RW × 32
fm_st_wd	FL × (8 + (MJA –1) × 48 + MNA) + RW × FL
fm_wd	floor(fm_bit_idx/32)
fm_wd_bit_idx	31 + 32 × fm_wd – fm_bit_idx

3

Virtex-E CLB LUT SelectRAM Dependent Variables

The additional block SelectRAM columns in Virtex-E devices require an adjustment to the MJA. The following equations calculate the adjustment necessary for each of the affected dependent variables. For each variable, calculate the base value based upon the Virtex equations only and then add the resulting Virtex adjustment.

Notes:

- Do NOT input the final results back into the original Virtex equations (e.g. do not use MJA_{final} value to calculate fm_st_wd).
- MJA_{final} = MJA + MJA_adj
- $fm\_st\_wd_{final}$ = fm_st_wd + fm_st_wd_adj

The left and right sides of the device are treated differently:

Table 8: **CLB Location**

CLB Location	CLB Column
Left	CLB_Col ≤ Chip_Cols/2
Right	CLB_Col > Chip_Cols/2

Table 9: **Virtex-E Families Adjustments for LUT SelectRAM Dependent Variables**

Term		Definition
MJA_adj	Left	RAM_Bound = (Chip_Rams/2 - 1) x RAM_Space MJA_adj = 2 x ceiling((RAM_Bound - CLB_Col + 1) / RAM_Space)
	Right	RAM_Bound = Chip_Cols - (Chip_Rams/2 - 1) x RAM_Space + 1 MJA_adj = 2 x ceiling((CLB_Col - RAM_Bound + 1) / RAM_Space)
fm_st_wd_adj		FL × (27 x MJA_adj)

LUT SelectRAM Examples

See "Examples" on page 27 for several examples of reading and evaluating configuration data. The examples illustrate how to make use of these equations to find the desired data in a bitstream.

CLB Flip-Flop Dependent Variables

Equations for the CLB flip-flops can be found in Table 10. Their locations are calculated similarly to the LUT SelectRAM locations. Equations for the CLB FF Dependent Variables are defined in Table 5.

Table 10: **Virtex Equations for CLB FF Dependent Variables**

Term	Definition
MJA	if (CLB_Col ≤ Chip_Cols/2) then Chip_Cols – CLB_Col × 2 + 2 else 2 × CLB_Col – Chip_Cols – 1
MNA	Slice × (12 × XY – 43) – 6 × XY + 45
fm_bit_idx	(18 × CLB_Row) + 1 + (32 × RW)
fm_st_wd	FL × (8 + (MJA –1) × 48 + MNA) + RW × FL
fm_wd	floor(fm_bit_idx/32)
fm_wd_bit_idx	31 + 32 × fm_wd – fm_bit_idx

Virtex-E CLB Flip-Flop Dependent Variables

Apply the adjustments given in Table 8 and Table 9.

IOB Dependent Variables

Each IOB contains four values that can be captured into special registers. These values are:

- I — the input flip-flop
- O — the output flip-flop
- T — the flip-flop for the tri-state control
- P — the value of the I/O pad

These values are captured by utilizing the CAPTURE_VIRTEX symbol in your design. The Libraries Guide has more details on the use of this symbol. The following registers will be read as part of the readback data.

Access to the IOB flip-flops is different for the top and bottom IOBs versus the left and right IOBs.

The top and bottom IOBs are part of the CLB column frames. There are two IOBs at the top and bottom of each CLB column.

The left and right IOBs are in columns by themselves. There are three IOBs per CLB row.

IOBs are numbered clockwise around the die. Pad 1 is located at the left side of the top edge, above CLB column 1. The equations for where to find IOB flip-flops in the bitstream are based on the ***pad number*** *which is the same for a given size device****,*** *not the package pin name, which varies from package to package*. The mapping from package pin names to pad numbers can be found in *EPIC* or *fpga_editor*.

Table 11 contains the numeric pad indices for the pads on all four edges of the device in terms of the number of CLB columns and rows on the device.

Table 11: **IOB Pad Indices**

Pad Location	Pad Index i
Top	$1 \le i \le Chip\_Cols \times 2$
Right	$Chip\_Cols \times 2 + 1 \le i \le Chip\_Cols \times 2 + Chip\_Rows \times 3$
Bottom	$Chip\_Cols \times 2 + Chip\_Rows \times 3 + 1 \le i \le Chip\_Cols \times 4 + Chip\_Rows \times 3$
Left	$Chip\_Cols \times 4 + Chip\_Rows \times 3 + 1 \le i \le Chip\_Cols \times 4 + Chip\_Rows \times 6$

Table 12 shows the equations for the dependent variables for the IOB flip-flops. The variable ***i*** in this table refers to the index of pad ***i***.

Table 12: **Equations for IOB Dependent Variables**

Term			Definition
MJA	Top		if ($i \le Chip\_Cols$) then $Chip\_Cols - ceiling(i/2) \times 2 + 2$ else $2 \times ceiling\ (i/2) - Chip\_Cols - 1$
	Right		$Chip\_Cols + 1$
	Bottom		if ($i > 3 \times (Chip\_Cols + Chip\_Rows)$) then $2 \times ceiling((i - 3 \times Chip\_Cols - 3 \times Chip\_Rows)/2)$ else $Chip\_Cols - 2 \times floor((i - 2 \times Chip\_Cols - 3 \times Chip\_Rows - 1)/2) - 1$
	Left		$Chip\_Cols + 2$
MNA	Top	I	$-25 \times (i\%2) + 45$
		O	$-13 \times (i\%2) + 39$
		T	$-5 \times (i\%2) + 35$
		P	$-4 \times (i\%2) + 25$
	Right	I	$t = (i - 2 \times Chip\_Cols)\ \%\ 3;\ MNA = 27.5 \times t^2 - 57.5 \times t + 32$
		O	$t = (i - 2 \times Chip\_Cols)\ \%\ 3;\ MNA = 21.5 \times t^2 - 51.5 \times t + 38$
		T	$t = (i - 2 \times Chip\_Cols)\ \%\ 3;\ MNA = 17.5 \times t^2 - 47.5 \times t + 42$
		P	50
	Bottom	I	$25 \times ((i - 2 \times Chip\_Cols - 3 \times Chip\_Rows)\%2) + 20$
		O	$13 \times ((i - 2 \times Chip\_Cols - 3 \times Chip\_Rows)\%2) + 26$
		T	$5 \times ((i - 2 \times Chip\_Cols - 3 \times Chip\_Rows)\%2) + 30$
		P	$4 \times ((i - 2 \times Chip\_Cols - 3 \times Chip\_Rows)\%2) + 21$
	Left	I	$t = (i - 4 \times Chip\_Cols - 3 \times Chip\_Rows)\%3;\ MNA = 17.5 \times t^2 - 47.5 \times t + 45$
		O	$t = (i - 4 \times Chip\_Cols - 3 \times Chip\_Rows)\%3;\ MNA = 23.5 \times t^2 - 53.5 \times t + 39$
		T	$t = (i - 4 \times Chip\_Cols - 3 \times Chip\_Rows)\%3;\ MNA = 27.5 \times t^2 - 57.5 \times t + 35$
		P	50

Table 12: **Equations for IOB Dependent Variables *(Continued)***

Term			Definition
fm_bit_idx	Top		32 × RW
	Right	I, O, &T	18 × (1 + floor ((i – 2 × Chip_Cols – 1)/3)) + 32 × RW
		P	t = (i – 2 × Chip_Cols) % 3; fm_bit_idx = 18 × (1 + floor ((i – 2 × Chip_Cols – 1)/3)) + 6 × t^2 – 17 × t + 15 + 32 × RW
	Bottom		18 × (Chip_Rows + 1)+ 32 × RW
	Left	I, O, &T	18 × (Chip_Rows – floor((i – 4 × Chip_Cols – 3 × Chip_Rows – 1)/3)) + 32 × RW
		P	t = (i – 4 × Chip_Cols – 3 × Chip_Rows)%3; fm_bit_idx = 18 × (Chip_Rows – floor ((i – 4 × Chip_Cols – 3 × Chip_Rows – 1)/3)) – 10.5 × t^2 + 21.5 × t + 4 + 32 × RW
fm_st_wd			if (MJA > Chip_Cols + 1) then FL × (54 × MJA – 46 + MNA – 6 × Chip_Cols) + RW × FL else FL × (8 + (MJA –1) × 48 + MNA) + RW × FL
fm_wd			floor (fm_bit_idx/32)
fm_wd_bit_idx			31 + 32 × fm_wd – fm_bit_idx

Virtex-E IOB Dependent Variables

Similar to CLB dependent variables, only the variables affected by the major address are different in Virtex-E and Virtex-EM devices versus Virtex devices. A simple way to account for the change is to determine the CLB column where the pad resides (only true for top and bottom). Then, the adjustment calculated for the CLB column can be applied. The conversion to CLB columns is found in Table 13:

Table 13: **Pad -> CLB Column**

Term		Definition
CLB_Col	Top	ceiling(i/2)
	Bottom	ceiling((4 x Chip_Cols + 3 x Chip_Rows + 1 - i)/2)

Table 14: **Virtex-E Families Adjustments for IOB Dependent Variables**

Term		Definition
MJA_adj	Top	use Table 8 and Table 9
	Right	Chip_Rams
	Bottom	use Table 8 and Table 9
	Left	Chip_Rams
fm_st_wd_adj		FL × (27 x MJA_adj)

Block SelectRAM Dependent Variables

The equations for the block SelectRAM dependent variables are given in Table 15. The relationship of a particular memory cell index in the context of a given configuration is described in XAPP130 "Using the Virtex Block SelectRAM+ Resource".

Table 15: **Virtex Equations for Block SelectRAM Dependent Variables**

Term	Definition
MJA	if (RAM_Col < Chip_Rams/2) then 2 x (Chip_Rams/2 - 1 - RAM_Col) else 2 x (RAM_Col - Chip_Rams/2) + 1
MNA	1 x floor(((ram_bit / 64) % 64)/32) + 2 x floor(((ram_bit / 64) % 32)/16) + 4 x floor(((ram_bit / 64) % 16)/8) + 8 x floor(((ram_bit / 64) % 8)/4) + 16 x floor(((ram_bit / 64) % 4)/2) + 32 x floor(((ram_bit / 64) % 2)/1) equivalent to MNA = div64[0:5] where div64[5:0] = floor(ram_bit/64)
fm_bit_idx	obtain value for bitpos from Table 16 fm_bit_idx = 18 + 72 x RAM_Row + bitpos
fm_st_wd	FL × MNA + RW × FL
fm_wd	floor(fm_bit_idx/32)
fm_wd_bit_idx	31 + 32 × fm_wd – fm_bit_idx

Table 16: **Virtex Block SelectRAM Bit Position Within a Given Block SelectRAM**

ram_bit % 64	bitpos	ram_bit % 64	bitpos	ram_bit % 64	bitpos	ram_bit % 64	bitpos	ram_bit % 64	bitpos	ram_bit % 64	bitpos	ram_bit % 64	bitpos	ram_bit % 64	bitpos
0	42	8	45	16	29	24	26	32	43	40	44	48	28	56	27
1	58	9	61	17	13	25	10	33	59	41	60	49	12	57	11
2	41	10	46	18	30	26	25	34	40	42	47	50	31	58	24
3	57	11	62	19	14	27	9	35	56	43	63	51	15	59	8
4	50	12	53	20	21	28	18	36	51	44	52	52	20	60	19
5	49	13	54	21	22	29	17	37	48	45	55	53	23	61	16
6	66	14	69	22	5	30	2	38	67	46	68	54	4	62	3
7	65	15	70	23	6	31	1	39	64	47	71	55	7	63	0

Virtex-E Block SelectRAM Dependent Variables

The RAM major address numbering scheme changed slightly such that the lowest MJA on the left side is now "2" instead of "0". As in the case for the CLB equations, the adjustments below should be applied after the Virtex equations.

Table 17: **Virtex-E and Virtex-EM Adjustments for Block SelectRAM Dependent Variables**

Term	Definition
MJA_adj	if (RAM_Col < Chip_Rams/2) MJA_adj = 2

Configuration Logic Basics

Configuration Data

Configuration data is organized as 32-bit words. There are two major commands that the configuration data can contain; Read and Write. A configuration command is executed when the configuration command is read or written to the appropriate command register.

The OP field contains 01 for a Read operation, and 10 for a Write operation. (See Figure 12).

OP	CODE
Read	01
Write	10

Figure 12: **OP Field Code**

A command is organized as a packet with a header word and optional data words. The header word is the first word written to the appropriate command register for a read or write operation. The header word contains a type field (001), an operand field, a register address field, and a word count field. The format for the command header is shown in Figure 13 on page 17.

The Register Address field defines the target of this command, as defined in Table 18 on page 17.

The header word count field contains an integer between 0 and 2,047 and indicates the number of words that follow the header. Larger word counts (between 2,048 and 1,048,575 words) are achieved by setting the header word count to 0. The Extension header word has a type field = 010, an OP field that must match the OP field in the preceding Command Header word, and a 20-bit word count, this format is shown Figure 14 on page 17.

Configuration Flow

Virtex devices are configured by presenting configuration data to the SelectMAP or JTAG interfaces in a specific sequence.

For Initial Configuration

1. Issue one or more pad words (SelectMAP only).
2. Issue Sync word (SelectMAP only).
3. Reset CRC.
4. Set FLR.
5. Set COR.
6. Set MASK.
7. Set CTL. (Set PERSIST if you want to keep SelectMAP active after this configuration.)
8. Issue a SWITCH (switch CCLK frequency) command to the CMD register. This is necessary only in Master Serial configuration mode.

Reading Configuration

These commands can be issued to read a full configuration or for a partial configuration after the device has been completely configured.

1. Issue a Sync word (SelectMAP only) if the previous configuration command was aborted.
2. Set the FAR to the starting address.
3. Issue a RCFG (read configuration) command to the CMD register.
4. Write the number of words to be read to the FDRO register.
5. Flush the command pipeline with a pad word.
6. Read data frames.

Writing Configuration

These commands can be issued either as part of an initial configuration or for a partial configuration after the device has been configured.

1. Issue a Sync word (SelectMAP only) if the previous configuration command was aborted.
2. If the frames being written can cause contention, then assert the GHIGH_B signal.
3. Set the FAR to the starting address.
4. Issue a WCFG (write configuration) command to the CMD register.
5. Write the number of words to be written to the FDRI register.
6. Write data frames.
7. If the GHIGH_B signal was asserted, de-assert it by writing the LFRM (Last Frame) command to the CMD register and write one pad frame.

Type			OP		Register Address													RSV		Word Count									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	x	x	0	0	0	0	0	0	0	0	0	0	x	x	x	x	0	0	x	x	x	x	x	x	x	x	x	x	x

Notes:
1. Locations within fields containing a zero or one must have these values. An X in a bit field indicates that the value is variable and must be set.
2. Heavy vertical lines are used to separate fields. Light vertical lines separate nibbles in the word.

Figure 13: **Command Header Format**

Type			OP		Word Count																								
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	x	x	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Notes:
1. Locations within fields containing a zero or one must have these values. An X in a bit field indicates that the value is variable and must be set.
2. Heavy vertical lines are used to separate fields. Light vertical lines separate nibbles in the word.

Figure 14: **Large Block Count Header Extension Format**

Configuration Registers

Configuration logic is accessed and controlled via a collection of 32-bit registers called the configuration registers (see Table 18). Registers are described in the following sections.

Table 18: **Configuration Register Addresses**

Register Name	Mnemonic	R/W	Binary Address
CRC	CRC	R/W	0000
Frame Address	FAR	R/W	0001
Frame Data Input	FDRI	W	0010
Frame Data Output	FDRO	R	0011
Command	CMD	R/W	0100
Control	CTL	R/W	0101
Control Mask	MASK	R/W	0110
Status	STAT	R	0111
Legacy Output	LOUT	W	1000

Table 18: **Configuration Register Addresses *(Continued)***

Register Name	Mnemonic	R/W	Binary Address
Configuration Option	COR	R/W	1001
Reserved	-	-	1010
Frame Length	FLR	R/W	1011
Reserved	-	-	1100
Reserved	-	-	1101
Reserved	-	-	1110
Reserved	-	-	1111

Command Register (CMD)

The content of the Command Register (CMD) is interpreted by the configuration state machine. Configuration commands control the operation of the configuration state machine, the Frame Data Register (FDR), and some of the global signals. The command in the Command Register is executed each time the FAR is loaded with a new value. The effect of each command is defined in Table 19.

Table 19: **Configuration Commands**

Cmd	Code	Description
Rsvd	0000	Reserved
WCFG	0001	**Write Configuration Data —** Used prior to writing configuration data to the FDRI. It takes the internal configuration state machine through a sequence of states that control the shifting of the FDR and the writing of the configuration memory. (See "Frame Data Input Register (FDRI)" on page 24).
Rsvd	0010	Reserved
LFRM	0011	**Last Frame —** This command is loaded prior to writing the last (pad) data frame if the GHIGH_B signal was asserted. This command is not necessary if the GHIGH_B signal was not asserted. This allows overlap of the last frame write with the release of the GHIGH_B signal.
RCFG	0100	**Read Configuration Data —** Used prior to reading frame data from the FDRO. Similar to the WCFG command in its effect on the FDR (see "Frame Data Output Register (FDRO)" on page 24).
START	0101	**Begin Startup Sequence —** Starts the startup sequence. This command is also used to start a shutdown sequence prior to partial re-configuration. The Startup Sequence begins with the next successful CRC check (see "Cyclic Redundancy Check (CRC)" on page 22).
RCAP	0110	**Reset Capture —** Used when performing capture in single-shot mode. This command must be used to reset the capture signal if single-shot capture has been selected.
RCRC	0111	**Reset CRC —** Used to reset CRC register (see "Cyclic Redundancy Check (CRC)" on page 22).
AGHIGH	1000	**Assert GHIGH_B Signal —** Used prior to re-configuration to prevent contention while writing new configuration data. All CLB outputs and signals are forced to a one.
SWITCH	1001	**Switch CCLK Frequency —** Used to change (increase) the frequency of the Master CCLK. The new frequency is specified in Table 21.
Rsvd	1010	Reserved
Rsvd	1011	Reserved
Rsvd	1100	Reserved

Table 19: **Configuration Commands *(Continued)***

Cmd	Code	Description
Rsvd	1101	Reserved
Rsvd	1110	Reserved
Rsvd	1111	Reserved

Configuration Option Register (COR)

The Configuration Option Register (COR) is used to select configuration options that are illustrated in Figure 15 and defined in Table 20. Entries in this table are further explained in the following tables:.

	DONE_PIPE	DRIVE_DONE	SINGLE	OSCFSEL				SSCLKSRC		LOCK_WAIT				SHUTDOWN	DONE_CYCLE			LCK_CYCLE				GTS_CYCLE				GWE_CYCLE				GSR_CYCLE			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Notes:

1. Locations within fields containing a zero or one must have these values. An *X* in a bit field indicates that the value is variable and must be set.
2. Heavy vertical lines are used to separate fields. Light vertical lines separate nibbles in the word.

Figure 15: **COR (Configuration of Option Register) Fields**

Table 20: **Configuration Option Register Fields**

Field	Bit Indices	Description	Bitgen Default
DONE_PIPE	30	0: No pipeline stage for DONEIN. 1: Add pipeline stage to DONEIN. FPGA waits on DONE that is delayed by one (1) cycle of the StartupClk rather than the pin itself. Use this option when StartupClk is running at high speeds.	0
DRIVE_DONE	29	0: DONE pin is open drain. 1: DONE pin is actively driven high.	0
SINGLE	28	Readback capture is one-shot.	0
OSCFSEL	27:22	Select CCLK frequency in Master Serial configuration mode.	2
SSCLKSRC	21:20	Startup sequence clock source 00: Cclk 01: UserClk 1x: JTAGClk	0
LOCK_WAIT	19:16	4-bit mask indicating which DLL lock signals to wait for during LCK cycle. The 4 bits (from MSB to LSB) correspond to DLLs TL=3, TR=2, BL=1, BR=0 (top-left, top-right, etc.). In Virtex-E devices where there are 8 DLLs, each mask bit applies to the 2 DLLs in that quadrant of the device. The default is not to wait for any DLL lock signals.	0
SHUTDOWN	15	Indicate whether doing a startup or shutdown sequence. 0: Startup 1: Shutdown sequence	0
DONE_CYCLE	14:12	Startup phase in which DONE pin is released	3
LCK_CYCLE	11:9	Stall in this startup phase until DLL locks are asserted.	7
GTS_CYCLE	8:6	Startup phase in which I/Os switch from tri-state to user design	4
GWE_CYCLE	5:3	Startup phase in which the global write-enable is asserted	5
GSR_CYCLE	2:0	Startup phase in which the global set/reset is negated	5

Table 21 shows the allowed values for the OSCFSEL field of the COR. Setting OSCFSEL to one of these values will set the Master CCLK frequency to the specified value.

Table 21: **OSCFSEL-Specified Master CCLK Frequencies**

CCLK (MHz)	OSCFSEL	CCLK (MHz)	OSCFSEL	CCLK (MHz)	OSCFSEL
4.3	000010	13	001010	41	100111
5.4	010001	15	001101	45	110011
6.9	000100	20	010111	51	101010
8.1	000101	26	011010	55	110100

Table 21: **OSCFSEL-Specified Master CCLK Frequencies *(Continued)***

CCLK (MHz)	OSCFSEL	CCLK (MHz)	OSCFSEL	CCLK (MHz)	OSCFSEL
9.2	000110	30	011101	60	101101
10.0	000111	34	110010	—	—

Notes:
1. These values are accurate to +45%, – 30%.

Table 22 shows the values of the DONE_CYCLE, LCK_CYCLE, GTS_CYCLE, GWE_CYCLE, and GSR_CYCLE fields in COR. This table shows the step in the start-up sequence when each of these signals becomes active.

Table 22: **COR Startup Cycle Fields**

Field Value	DONE_CYCLE (DONE Active)	GTS_CYCLE (GTS_CFG Inactive)	GSR_CYCLE (GSR Inactive)	GWE_CYCLE (GWE Active)	LCK_CYCLE
000	1	1	1	1	0
001	2	2	2	2	1
010	3	3	3	3	2
011	4 (default)	4	4	4	3
100	5	5 (default)	5	5	4
101	6	6	6 (default)	6 (default)	5
110	-	DoneIn†	DoneIn†	DoneIn†	6
111	Keep State	Keep State	Keep State	Keep State	Don't Wait (default)

Notes:
1. † DONE if DonePipe = No, else the delayed version of DONE.

Control Register (CTL)

The Control Register (CTL) fields are illustrated in Figure 16 on page 21 and defined in Table 23.

																					SBITS	PERSIST						GTS_USR_B
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	0	0	0	0	0	x

Notes:
1. Locations within fields containing a zero or one must have these values. An *X* in a bit field indicates that the value is variable and must be set.
2. Heavy vertical lines are used to separate fields. Light vertical lines separate nibbles in the word.

Figure 16: **Control Register Fields**

Name	Bit Indices	Description
SBITS	8:7	Security level: 0: Read/Write OK (default) 1: Readback disabled. 2,3: Readback disabled, Writing disabled except CRC register.
PERSIST	6	Configuration interface remains after configuration. 0: No (default) 1: Yes
GTS_USR_B	0	Active-low global tristate I/Os. Turn off pull-ups if GTS_CFG_B is also asserted.

Table 23: **Control Register Bits**

Cyclic Redundancy Check (CRC)

A data input error checking mechanism is provided through the Cyclic Redundancy Check (CRC) register. When data is written to any configuration register (except LOUT) a 16-bit CRC value is calculated using both the register data and the address. This value is saved in the CRC register. At the end of any series of writes a pre-calculated CRC block-check value may be written to the CRC register. If the resulting value is non-zero, an error is indicated. The CRC_ERROR bit is accessible through the status register. If a CRC error is detected, configuration logic is put in the ERROR mode. The following section is an algorithm for computing CRC.

CRC Algorithm

```
/* Initialization */
bcc = 0;
skip_pad = true;
more_words = true;
/* Check for write operation. */
do {
  w = next_word;
  if (w[31:27] == '00101') {
    /* A Read OP. Don't use in CRC*/
    wc = w[10:0];
    if (wc == 0) {
      w = next_word;
      wc = w[19:0];
    }
    while (wc--  > 0) {
      w = next_word;
    }
  }
  elsif (w[31:27] == '00110') {
    /* A Write OP. Use in CRC. */
    addr = w[16:13];
    if (addr Œ {0,1,2,4,5,6,9,D,B}) {
      wc = w[10:0];
      if (wc == 0) {
          /* wc is in next word. */
        w = next_word;
        wc = w[19:0];
      }
      while (wc--  > 0) {
        w = next_word;
        sw[35:0] = addr, word;
        for (i=0; i<36; i++) {
          x16 = bcc[15] XOR sw[i];
          x15 = bcc[14] XOR x16;
```

```
            x2 = bcc[1] XOR x16;
            bcc[15:0] =
                x15,bcc[13:2],x2,bcc[0],x16;
          }
          /* Note the bit order */
          crc[15:0] = bcc[0:15];
        }
      }
    }
    else {
      /* Pad word - ignore */
    }
} while (more_words)
```

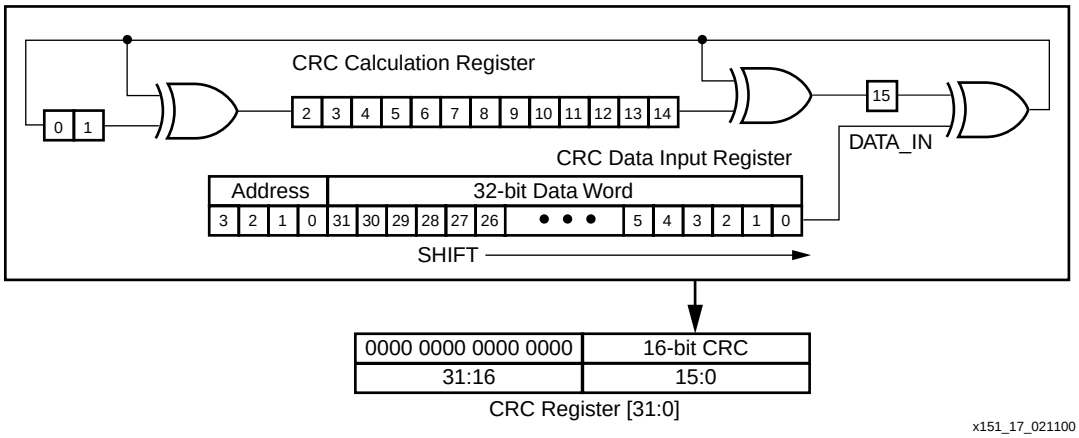


Figure 17: **CRC Calculation Register**

Frame Address Register (FAR)

The Frame Address Register (FAR) holds the address of the current frame. The address is divided into three parts, the block type, the major address, and the minor address. The block type field indicates whether the CLB or block RAM address space is used. The command in the command register is executed each time the FAR is loaded with a new value.

The major address selects the CLB or RAM column, the minor address selects the frame within the column. The minor address is incremented each time a full data frame is read from or written to the frame data register. If the last frame within the CLB column is selected when the increment occurs, the major address is incremented and the minor address is reset to zero, otherwise the minor address is incremented. However, the block RAM major address is not incremented automatically.

Note: the Block RAM Major Address is not incremented automatically. To address a different Block RAM Content column, the FAR must be loaded with the new Major Address.

See Figure 18 for the definitions of valid values for the block type field. The FAR field definitions are shown in Figure 19.

Type	Codes
CLB	00
RAM	01

Figure 18: **Block Type Codes**

				Block Type			Major Address (Column Address)								Minor Address (Frame Address)															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0

Notes:

1. Locations within fields containing a zero or one must have these values. An *X* in a bit field indicates that the value is variable and must be set.
2. Heavy vertical lines are used to separate fields. Light vertical lines separate nibbles in the word.

Figure 19: **Frame Address Fields (FAR)**

Frame Data Input Register (FDRI)

The Frame Data Input Register (FDRI) is used to load configuration frame data into a Virtex device.

The Frame Data Register (FDR) is a shift register into which data is loaded prior to transfer to the configuration memory. Configuration data is written to the Virtex device by loading the command register with the WCFG command and then loading the FDR with at least two frames of 32-bit words.

The write operation is pipelined such that the first frame of data is written to the configuration memory while the second frame is being shifted in. The last frame (the pad frame) is always dummy data which is not actually written to the configuration memory. Each frame write must include enough 32 bit data words to load the frame fully. There is one pad word at the end of each frame which is required for the pipelining hardware.

Frame Data Output Register (FDRO)

The Frame Data Output Register (FDRO) is for reading configuration data or captured data from the Virtex device, a process called readback. Readback is performed by loading the command register with the RCFG command and then addressing the FDRO with a read command.

Frame Length Register (FLR)

Near the beginning of the configuration bitstream the Frame Length Register (FLR) is written with the length of a frame, as measured in 32-bit words. This length count is used to provide sequencing information for the configuration read and write operations. Note that the FLR must be written before any FDR operation works. It is not necessary to set the FLR more than once. If the number of bits in a frame is not evenly divisible by 32, the length count of the frame must be rounded up to the next highest integer. The values for the FLR for all the current Virtex series devices are given in Table 24.

Note: The FLR contains a value that is one less than the number of words that are read from or written to a given frame. This is because the extra word needed for pipelining is not counted.

Table 24: **Frame Length Register Value**

Device	Row × Col	Frame Length	# Words per Frame	FLR Value
XCV50/E	16 × 24	384	12	11
XCV100/E	20 × 30	448	14	13
XCV150	24 × 36	512	16	15
XCV200/E	28 × 42	576	18	17
XCV300/E	32 × 48	672	21	20
XCV400/E	40 × 60	800	25	24

Table 24: **Frame Length Register Value *(Continued)***

Device	Row × Col	Frame Length	# Words per Frame	FLR Value
XCV405E	40 × 60	800	25	24
XCV600/E	48 × 72	960	30	29
XCV800	56 × 84	1088	34	33
XCV812E	56 × 84	1088	34	33
XCV1000/E	64 × 96	1248	39	38
XCV1600E	72 × 108	1376	43	42
XCV2000E	80 × 120	1536	48	47
XCV2600E	92 × 138	1728	54	53
XCV3200E	104 × 156	1952	61	60

Legacy Output Register (LOUT)

The Legacy Output Register (LOUT) is used for daisy chaining the configuration bitstream to other Xilinx devices. Data written to the LOUT is serialized and appears on the DOUT pin.

Mask Register (MASK)

The Mask Register (MASK) is a mask register for writes to the CTL register. A "1" in bit N of the mask allows that bit position to be written in the CTL register. The default value of the mask is all "0"s.

Status Register (STAT)

The Status Register (STAT) is loaded with current values of several control or status signals. The register can be read via the re-configuration block or via JTAG. The fields in the Status register are illustrated in Figure 20. The values of the signals given in Table 25 on page 26 can be read from the status register.

																DONE	INIT	MODE			GHIGH_B	GSR_B	GWE_B	GTS_CFG	IN_ERROR	LOCK				CRC_ERROR
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Notes:

1. An *X* in a bit field indicates that the value is variable.
2. Heavy vertical lines are used to separate fields. Light vertical lines separate nibbles in the word.

Figure 20: **Status Register Fields**

Configuration Interface

Table 25: **Status Register Bits**

Name	Bit Indices	Description
DONE	14	Input from DONE pin
INIT	13	Value of $\overline{\text{INIT}}$
MODE	12:10	Value of M2, M1, M0 mode pins
GHIGH_B	9	0 = GHIGH_B asserted
GSR_B	8	0 = all flip-flops are Reset/Set
GWE_B	7	1 = flip-flops and block RAM are write disabled
GTS_CFG	6	0 = I/Os are tri-stated
IN_ERROR	5	Legacy input error
LOCK	4:1	Output from DLL lock signals. 1 = DLL is locked.
CRC_ERROR	0	Indicates that a CRC error has occurred.

There are two configuration interfaces to the Virtex devices — the bit-serial Boundary Scan interface and the 8-bit byte-serial SelectMAP interface. Conceptually, XCV50 configuration data appears as in Figure 21.

Data Frame 0 (11 words)	Pad Word
⋮	
Data Frame *n* (11 words)	Pad Word
Pad Frame (12 words)	

Figure 21: **XCV50 Frame Padding for Reads**

Frames and words within frames are written in the same order in both configuration interfaces, starting with Frame 0, word 0 (the left-most in the picture), followed by word 1, etc. Bits within each word are written from left to right (*MSB first*) in the bit-serial configuration interfaces.

Within the SelectMAP interface, data is written a byte at a time. A sample word is shown in Figure 22. The top row indicates the device pin names. The bottom row indicates the bit indices within a configuration word. Byte 0 loads first, followed by byte 1, *et cetera*. The MSB of each byte (*i.e.*, bits 31, 23, 15, and 7) is loaded on pin D0. The LSB of each byte (*i.e.*, bits 24, 16, 8, and 0) is loaded on pin D7.

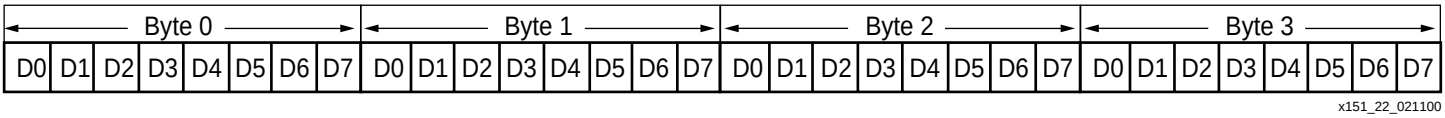


Figure 22: **SelectMAP Byte and Bit Ordering**

Examples

Several examples of reading and evaluating configuration data are provided to illustrate the following.

Example 1: Read and Write Semaphores in an XCV100 at CLB R1 C1, Slice 0.

Semaphores are a useful communication mechanism documented in XAPP 153, “Status and Control Semaphore Registers using Partial Reconfiguration.” Figure 23 shows an abstraction of a microprocessor writing control information to an FPGA and reading status information. One convention for implementing semaphores in Virtex devices is to use two bits of a 16-bit, dual-port RAM, as illustrated in Figure 24. This occupies one CLB slice with the F-LUT implementing the control semaphore and the status semaphore implemented in the G-LUT. Address 15 of the G-LUT is used for on-chip writes to the semaphore and address 14 of the F-LUT is used for on-chip reads. Conversely, the off-chip microprocessor is reading the G-LUT[15], and writing F-LUT[14].

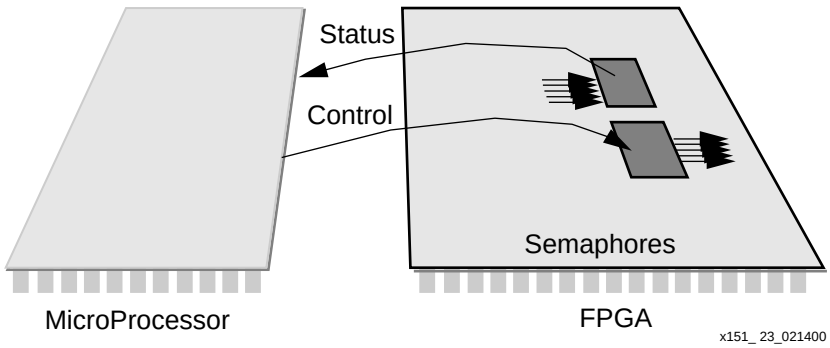


Figure 23: **Semaphore Abstraction**

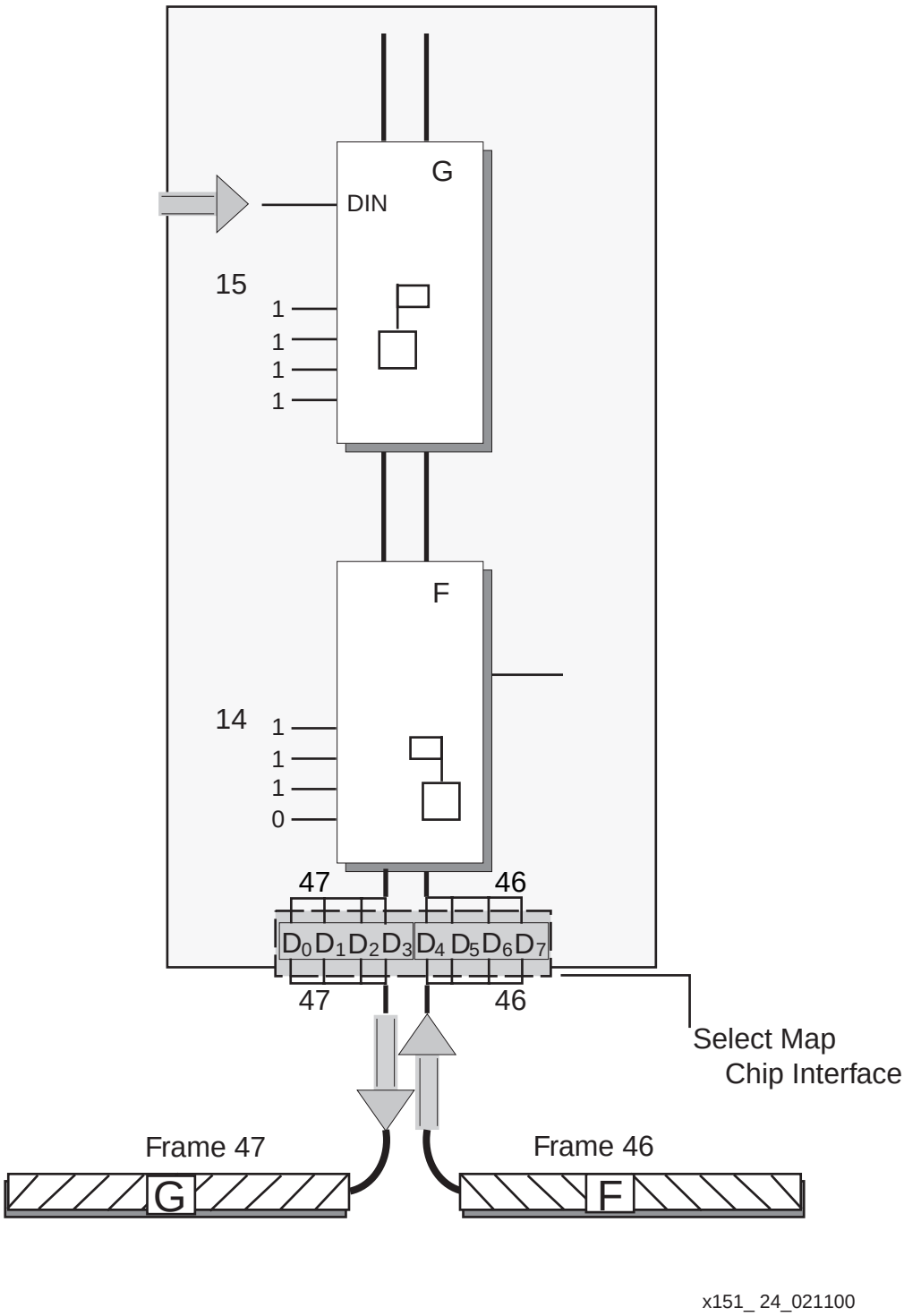


Figure 24: **Semaphore Read/Write Implementation**

Using a Semaphore Abstraction dual-port RAM ensures that the LUT SelectRAMs are placed in the CLB in a predictable manner. *When writing data to one or more LUT SelectRAMs or flip-flops on the device, all bits in the frame **must** have valid configuration information.* This is assured by altering valid configurations from bitstream files or from frames read from a properly configured Virtex device. The latter approach is used in this example.

Attributes for this design are summarized in Table 26.

Table 26: **Design Attributes for Example 1**

Attribute	G-LUT [15]	F-LUT [14]	
	Read	Read	Write
Chip_Rows	20		
Chip_Cols	30		
FL	14		
CLB_Row	1		
CLB_Col	1		
Slice	0		
FG	1	0	
lut_bit	15	14	
RW	1	1	0

From the equations in Table 7 on page 11, the values shown in Table 27 can be calculated.

Table 27: **Semaphore Example Variables, Equations, and Values**

Variable	Equation	Value(s)		
		G-LUT[15]	F-LUT[14]	
		Read	Read	Write
MJA	$1 \le 30/2 \Rightarrow 30 - 1 \times 2 + 2$	30		
MNA	lut_bit + 32– 0 × (...)	47	46	
fm_bit_idx	3 + 18 × 1 – FG + RW × 32	52	53	21
fm_st_wd	14 × (8 + (30 – 1) × 48 + {46,47}) +RW × (14 +1) = 14 × (1,400 + {46,47}) + 14 × RW = 19,600 + 14 × {46,47} + 14 × RW	20,272	20,258	20,244
fm_wd	floor (20/32)	1	1	0
fm_wd_bit_idx	31 + 32 × {1,1,0} – {52,53,21}	11	10	10

From off-chip, for reading the G-LUT[15] bit, read one frame (MNA=47). For writing the F-LUT[14] bit, we show how to read then write one frame (MNA=46), as opposed to modifying data from a bitstream file (both are valid methods). The frames on the XCV100 contain 13 32-bit words and one pad word. Remember that fm_st_wd is calculated assuming the entire configuration has been read. However, only the pad frame and then frames 46 and 47 from Major Address 30 are being read. The desired bit is in Frame 1, word #1, which is word 15.

The commands for reading both frames (and the pad frame) are given in Figure 25.

Instruction	Hex	Data																													
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sync Word	AA99 5566	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	0	1	0	1	0	1	0	1	0	1	1	0	0	1	1	0
Write next (1) word to FAR	3000 2001	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
CLB MJA=30, MNA=46	003C 5800	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
Write next word to CMD	3000 8001	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Register value for RCFG	0000 0004	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Read from FDRO	2800 602A	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0	1	0	1	0
Flush pipe	0000 0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
(read 42 words)																																	

Notes:

1. Binary data is grouped in two ways for ease of interpretation. Thin vertical lines separate nibble boundaries. Heavy vertical lines separate field boundaries.

Figure 25: **Commands to Read Two Data Frames**

The 42 words read are shown in Figure 26. F-LUT[14] is in the second frame (frame=1, word=1) at bit 10. The value read is a "1", but because the LUT bits are inverted, the logic value is zero. G-LUT[15] is in word one of the third data frame (frame=2, word=1) at bit 11.The value read is a "1", which is a logic zero.

Frame	Word	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	3	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	5	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	6	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	7	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	8	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	9	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	10	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	11	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	12	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	13	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	F[14]
	2	1	1	1	1	1	0	1	1	0	0	0	0	1	1	1	1	0	0	1	1	1	1	1	0	1	1	0	0	0	0	0	0	
	3	0	0	0	0	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	0	0	
	4	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	
	5	1	1	0	0	1	1	0	0	0	0	0	0	1	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	
	6	1	1	1	0	1	1	0	0	0	0	0	0	1	1	1	0	1	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	
	7	0	0	1	1	1	1	1	0	1	1	0	0	0	0	1	1	0	0	0	0	1	1	1	1	1	0	1	1	0	0	0	0	
	8	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	
	9	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	
	10	1	0	1	1	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	
	11	1	1	1	1	1	0	1	1	0	0	0	0	1	1	1	1	0	0	1	1	1	1	1	0	1	1	0	0	0	0	0	0	
	12	0	0	0	0	1	1	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	
	13	0	0	0	0	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1	1	0	1	0	0	0	0	0	0	0	0	1	1	0	1	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	G[15]
	2	1	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	
	3	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	
	4	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	
	5	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	1	1	
	6	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
	7	0	0	1	1	1	1	1	1	1	1	0	0	0	0	1	1	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	
	8	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
	9	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	
	10	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	
	11	1	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	
	12	0	0	0	0	1	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	
	13	0	0	0	0	0	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Figure 26: **Three Frames Containing the Semaphores**

To write to the F-LUT semaphore, start with the second data frame (frame=1) that was just read. Words 1 - 13 of that frame will become words 0 - 12 of the frame to be written. Word 13 of this new frame is a pad word and can have any value (typically 0 is chosen). In this new frame, set bit 11 of word 0 (zero) to the desired value of the semaphore. A pad frame must follow the data frame. The commands from Figure 27 write these two frames into the device at the proper location.

Instruction	Hex	Data (31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0)
Sync Word	AA99 5566	1 0 1 0 | 1 0 1 0 | 1 0 0 1 | 1 0 0 1 | 0 1 0 1 | 0 1 0 1 | 0 1 1 0 | 0 1 1 0
Write next (1) word to FAR	3000 2001	0 0 1 | 1 | 0 | 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 1 | 0 | 0 | 0 0 0 | 0 0 0 0 | 0 0 0 1
MJA=30, MNA=46	003C 5C00	0 0 0 0 | 0 | 0 0 | 0 | 0 0 1 1 | 1 1 0 | 0 | 0 1 0 | 1 | 1 1 0 | 0 | 0 0 0 0 | 0 0 0 0
Write next word to CMD	3000 8001	0 0 1 | 1 | 0 | 0 0 0 | 0 0 0 0 | 0 0 0 0 | 1 0 0 | 0 | 0 | 0 0 0 | 0 0 0 0 | 0 0 0 1
Register value for WCFG	0000 0001	0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 1
Write 28 words to FDRI	3000 401C	0 0 1 | 1 | 0 | 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 1 0 | 0 | 0 | 0 0 0 | 0 0 0 1 | 1 1 0 0
Data Word 0	A01A EC00	1 0 1 0 | 0 0 0 0 | 0 0 0 1 | 1 0 1 0 | 1 1 1 0 | 1 1 0 0 | 0 0 0 0 | 0 0 0 0
Data Word 1	FF0F 3FC0	1 1 1 1 | 1 1 1 1 | 0 0 0 0 | 1 1 1 1 | 0 0 1 1 | 1 1 1 1 | 1 1 0 0 | 0 0 0 0
Data Word 2	0FF0 02FC	0 0 0 0 | 1 1 1 1 | 1 1 1 1 | 0 0 0 0 | 0 0 0 0 | 0 0 1 0 | 1 1 1 1 | 1 1 0 0
⋮	⋮	⋮
Data Word 27	0000 0000	0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0

Notes:

1. Binary data is grouped in two ways for ease of interpretation. Thin vertical lines separate nibble boundaries. Heavy vertical lines separate field boundaries.

Figure 27: **Commands to Write a Semaphore Value**

Example 2: Reading the Complete Configuration from an XCV50.

Steps:

1. If flip-flop values are needed, clock the on-chip signal, CAPTURE, to capture flip-flop values. See the Xilinx Libraries Guide for use of the CAPTURE_VIRTEX cell.
2. Write the starting frame address (CLB MJA=0 MNA=0) into the FAR.
3. Write the RCFG command to the CMD register.
4. Address the FDRO register with a READ operation and word count equal to the number of 32-bit words in the CLB frames plus one pad frame.
5. Read the data following the timing diagrams in the SelectMAP interface section.
6. Write the address for RAM block 0 to the FAR.
7. Address the FDRO register with a read operation and word count equal to the number of 32-bit words in the RAM block plus one pad frame.
8. Read the data.
9. Write the address for RAM block 1 to the FAR.
10. Address the FDRO register with a read operation and word count equal to the number of 32-bit words in the RAM block plus one pad frame.
11. Read the data.

When using SelectMAP mode to read data words from the Virtex device, de-assert $\overline{CS}$, de-assert $\overline{WRITE}$, assert $\overline{CS}$, then clock the data out. When using JTAG, load the JTAG IR

(instruction register) with the CFG_OUT instruction. Then go to the SDR (Shift-DR) state and shift the data out. (See Figure 28).

Instruction	Hex	Data 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sync Word	AA99 5566	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	0	1	0	1	0	1	0	1	0	1	1	0	0	1	1	0
Write next word to FAR.	3000 2001	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
CLB MJA=0, MNA=0	0000 0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Write next word to CMD register.	3000 8001	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Register value for RCFG	0000 0004	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Read from FDRO register.	2800 6000	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
15876 words	4800 3E04	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	1	0	0
Flush pipe	0000 0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
(Read 15876 words.)																																	
Write to FAR register.	3000 2001	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
RAM MJA=0, MNA=0	0200 0000	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read 780 words from FDRO reg.	2800 630C	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	1	1	0	0
Flush pipe	0000 0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
(Read 780 words.)																																	
Write to FAR register.	3000 2001	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
RAM MJA=1, MNA=0	0202 0000	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read 780 words from FDRO reg.	2800 630C	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	1	1	0	0
Flush pipe.	0000 0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
(Read 780 words.)																																	

Figure 28: **Example 2 - Read Complete Configuration for XCV50**

Example 3: Read the Slice 0 G-LUT from CLB R1 C1 from the Complete Configuration of an XCV50.

The commands for reading the bitstream from the Virtex device are given in "Example 1: Read and Write Semaphores in an XCV100 at CLB R1 C1, Slice 0." on page 27. Using an XCV50 device, the independent attributes are show in Table 28:

Table 28: **XCV50 Independent Attributes**

Independent Attributes	Values
Chip_Rows	16
Chip_Cols	24
FL	12
CLB_Row	1
CLB_Col	1
FG	1
Slice	0
RW	1

From the equations given earlier in Table 7, calculating the range of values for fm_st_wd indicates that the word 13740 of the configuration is the starting word of the 12-word (FL=12) frame containing bit 0 of the G-LUT in Slice 0 of CLB R1C1 (Table 29).

Table 29: **Variables, Equations and Values for Slice 0 G-LUT**

Variables	Equations	Values			
MJA	$1 \le 24/2 \Rightarrow 24 - 1 \times 2 + 2$	24			
MNA	$0 \times (\ldots)$ + lut_bit + 32	0: 32 1: 33 2: 34 3: 35	4: 36 5: 37 6: 38 7: 39	8: 40 9: 41 10: 42 11: 43	12: 44 13: 45 14: 46 15: 47
fm_bit_idx	$3 + 18 \times 1 - 1 + RW \times 32$	52			
fm_st_wd	$12 \times (8 + (24 - 1) \times 48 + [32:47]) + 1 \times 12$ $= 12 \times (1112 + [32:47]) + 12$ $= 13,356 + 12 \times 32:47]$	13,740:13,920			
fm_wd	floor(52/32)	1			
fm_wd_bit_idx	31 + 32 – 52	11			

The configuration bits for the given frame are as follows. G-LUT[0] is in fm_wd=0, at bit #11.

Bitstream Word	Frame 32-bit Word																														Frame Word
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
13740	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13741	0	0	1	0	1	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	1
13742	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	2
13743	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	3
13744	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	4
13745	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	5
13746	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	6
13747	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	7
13748	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	8
13749	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	9
13750	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	10
13751	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	11

Figure 29: **Configuration Bits for Slice 0, CLB R1C1 G-LUT [0]**

All 16 LUT SelectRAM bits are in the following words at the same bit index, 11.

Bitstream Word	Frame 32-bit Word																															LUT Bit
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
13741	0	0	1	0	1	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
13753	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1
13765	1	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	2
13777	0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	3
13789	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	4
13801	1	0	1	0	1	0	0	0	0	0	0	1	0	0	0	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	5
13813	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	6
13825	0	1	1	0	1	0	0	0	0	0	0	1	0	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	7
13837	1	0	1	1	1	0	0	0	0	0	0	1	0	1	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	8
13849	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	9
13861	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	10
13873	1	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	11
13885	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	12
13897	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	13
13909	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	14
13921	1	0	1	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	15

Figure 30: **Location of all 16 LUT SelectRAM Bits**

The 16 bits are $\overline{\text{LUT}}$[15:0]=0111111111111111. The LUT SelectRAM bits are inverted from their logic values. The “logical” contents are LUT[15:0]=1000000000000000. Thus, this G-LUT implements a 4-input AND function.

Example 4: Read the Slice 1 F-LUT from CLB R19 C16 from an XCV100.

Commands for reading the bitstream from the Virtex device are given in Figure 31. Use the following independent attributes to find the given F-LUT.

Table 30: **Virtex Bitstream Command Attributes**

Independent Attributes	Values
Chip_Rows	20
Chip_Cols	30
FL	14
CLB_Row	19
CLB_Col	16
FG	0
Slice	1
RW	1

From the equations in Table 7 on page 11, calculating fm_st_wd indicates the starting word with respect to a configuration that starts at MJA=0, MNA=0. Because the frames we are interested

in start at MJA=1, MNA=0, which is fm_st_wd = 126, so the first 126 words are not needed (0–125). Therefore, to find the given Slice 1 F-LUT, see Table 31.

Table 31: **Variables, Equations, and Values for Slice 1 F-LUT**

Variables	Equations	Values			
MJA	16 > 30/2 ⇒ 2×16 – 30 –1	1			
MNA	lut_bit + 32 – Slice × (2 × lut_bit +17) = [0:15] + 32 – (2 × [0:15] + 17) = 15 – [0:15]	0: 15 1: 14 2: 13 3: 12	4: 11 5: 10 6: 9 7: 8	8: 7 9: 6 10: 5 11: 4	12: 3 13: 2 14: 1 15: 0
fm_bit_idx	3 + 18 × 19 – 0+ 32	377			
fm_st_wd	14 × (8 + (1– 1) × 48 + [15:0]) +1 × 14 = 14 × (8 + [15:0]) +14 = 126 + 14 × [15:0]	= 336:126			
fm_wd	floor(377/32)	11			
fm_wd_bit_idx	31 + 32 × 11 – 377	6			

Sixteen frames need to be read, one for each bit in the LUT SelectRAM. The bits in LUT SelectRAMs in Slice 1 occur in the opposite order that they do for Slice 0 LUT SelectRAMs.

Frames are read sequentially with ascending addresses. If read in LUT bit order, LUT[0], LUT[1], …, LUT[15]. These are stored in descending addresses which require 16 separate read operations each reading one data frame and one pad frame. However, if read in ascending address order, LUT[15], LUT[14], …, LUT[0], all 16 data frames are read with a single read operation. This requires only one pad frame for all 16 frames. Thus, it takes less time to read ascending frames starting at MJA=1, MNA=0 and finishing with frame MJA=1, MNA=15. The frames in the XCV100 contain 14 32-bit words and a single pad word. Commands for reading only the F-LUT data are given in Figure 31.

Instruction	Hex	Data 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sync Word	AA99 5566	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	0	1	0	1	0	1	0	1	0	1	1	0	0	1	1	0
Write next (1) word to FAR.	3000 2001	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
CLB MJA = 1, MNA = 0	0002 0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Write next word to CMD.	3000 8001	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Register value for RCFG	0000 0004	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Read from FDRO.	2800 60EE	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	1	0	1	1	1	0
Flush pipe.	0000 0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
(Read 238 words.)																																	

Figure 31: **Commands to read Slice 1 F-LUT**

The 377th bit of each frame is the bit in the F-LUT. This LUT SelectRAM bit is in the frame's word index 11, bit index 6.

The configuration bits for the given frame in Figure 32 are as follows: LUT Bit 15 is in MJA=1, MNA=0, fm_wd=11, at bit #6.

Frame Word	Frame 32-bit Word																													
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
2	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0
3	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0
4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
5	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1
6	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
7	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
8	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
9	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1
10	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
11	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0
12	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
13	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0

Figure 32: **Frame Containing F-LUT[15]**

LUT bit 0 is in MJA=1, MNA=15, fm_wd=11, at bit #6.

Bit stream Word	Frame 32-bit Word																														FmWd
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
336	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
337	0	1	0	0	1	0	0	0	0	0	0	1	0	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1
338	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	2
339	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	3
340	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	4
341	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	5
342	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	6
343	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	7
344	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	8
345	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	9
346	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	10
347	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	1	1	0	1	0	0	0	0	11
348	0	0	0	0	1	1	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	12
349	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	13

Figure 33: **Frame Containing F-LUT [0]**

For the sake of brevity, here are the sixteen 11th words in the order they appear in the bitstream.

Bitstream Word	Frame 32-bit Word																																LUT Bit
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
137	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	15
151	1	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	1	1	0	0	0	0	0	0	14
165	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	1	1	0	0	0	0	0	0	13
179	1	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	1	1	0	0	0	0	0	0	12
193	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	0	0	0	0	0	0	11
207	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	0	0	0	10
221	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	0	0	0	0	0	0	9
235	1	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	1	1	0	0	0	0	0	0	8
249	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	7
263	1	0	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	1	1	0	0	0	0	0	0	6
277	1	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0	0	0	0	0	5
291	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	4
305	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	0	0	0	0	0	0	3
319	1	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	1	1	0	0	0	0	0	0	2
333	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	1
347	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	1	1	0	1	0	0	0	0	0

Figure 34: **Sixteen Words Containing the F-LUT bit**

The bits are $\overline{\text{LUT}}$[15:0]=0111111111111111. The LUT SelectRAM bits are inverted from the logic sense. The logical contents are LUT[15:0]=1000000000000000. Thus, this F-LUT implements a 4-input AND gate.

Example 5: Read All Bits in Slice 0 G-LUTs from CLB C2 and XCV50.

Given the following attributes, the necessary values to find the G-LUT data can be computed.

Table 32: **All Bits: Slice 0 G–LUTs from CLB C2 and XCV50**

Independent Attributes	Values
Chip_Rows	16
Chip_Cols	24
FL	12
CLB_Row	1:16
CLB_Col	2
FG	1
Slice	0
lut_bit	0:15
RW	1

From the equations in Table 7, the dependent variables can be calculated.

Table 33: **Dependent Variables, Equations, and Values**

Variables	Equations	Values			
MJA	$2 \le 24/2 \Rightarrow 24 - 2\times 2 + 2$	22			
MNA	lut_bit + 32 – Slice × (2 × lut_bit + 17) = lut_bit + 32 – 0 × (2 × lut_bit + 17) = [0:15] + 32	0:32	4:36	8:40	12:44
		1:33	5:37	9:41	13:45
		2:34	6:38	10:42	14:56
		3:35	7:39	11:43	15:47
fm_bit_idx	3 + 18 × CLB_Row – 1+ 32 = 34 + 18 × [1:16]	1:52	5:124	9:196	13:268
		2:70	6:142	10:214	14:286
		3:88	7:160	11:232	15:304
		4:106	8:178	12:250	16:322
fm_st_wd	12 × (8 + (22 –1) × 48 + MNA) + 1 × 12 = 12 × (1,016 + MNA) + 12 = 12,204 + 12 × MNA	0: 12,588	4: 12,636	8: 12,684	12: 12,732
		1: 12,600	5: 12,648	9: 12,696	13: 12,744
		2: 12,612	6: 12,660	10: 12,708	14: 12,756
		3: 12,624	7: 12,672	11: 12,720	15: 12,768
fm_wd	floor (fm_bit_idx/32)	1:1	5:3	9:6	13:8
		2:2	6:4	10:6	14:8
		3:2	7:5	11:7	15:9
		4:3	8:5	12:7	16:10
fm_wd_bit_idx	31 + 32 × fm_wd – fm_bit_idx	1:11	5:3	9:27	13:19
		2:25	6:17	10:9	14:1
		3:7	7: 31	11:23	15:15
		4:21	8:13	12:5	16:29

Note that fm_bit_idx, fm_wd, and fm_wd_bit_idx have 16 values, one for each row on the XCV50. Figure 36 shows where the data lies in the first frame, which contains G[0] for the entire column. The process is the same for the other 15 frames. The commands for reading the LUT SelectRAM data are given in Figure 35.

From the calculation for fm_st_wd, Frame 0 would start at word 12,588 reading the whole configuration. The instructions in Figure 35 start at that word, so word 0 (ignoring the 12 words in the pad frame) is the same as word 12,588 of the entire CLB configuration. The 12 words in the frame are shown in Figure 36.

The LUT SelectRAM bits have been shaded for ease of identification. It can be seen from the calculation of fm_bit_idx that the LUT SelectRAM bits are in the order 1:16. For example, from the above calculations for fm_wd and fm_wd_bit_idx, G-LUT[0] in R1C2 is in fm_wd 1,

fm_wd_bit_idx 11. This bit is the shaded bit in word 1 at bit index 11. Similarly, the G-LUT[0] for the other 15 CLB rows are also shaded in this table.

Instruction	Hex	Data 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sync Word	AA99 5566	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	0	1	0	1	0	1	0	1	0	1	1	0	0	1	1	0
Write next (1) word to FAR.	3000 2001	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
CLB MJA=22, MNA=32	002C 4000	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Write next word to CMD.	3000 8001	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Register value for RCFG	0000 0004	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Read from FDRO.	2800 60CC	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	0	0	1	1	0	0
Flush pipe.	0000 0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
(Read 204 words.)																																	

Figure 35: **Commands to read R*C2.S0 G-LUT**

Word	Frame 32-bit Word 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	CLB Row
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1
2	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	2, 3
3	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	4, 5
4	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	6
5	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	7, 8
6	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	9, 10
7	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	11, 12
8	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	13, 14
9	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	15
10	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	16
11	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Figure 36: **Frame for R*C2.S0 G-LUTs, Bit G[0]**

Example 6: Read Block SelectRAM index 387 of RAM R2 C0 from an XCV100E.

Commands for reading the bitstream from the Virtex device are given in Figure 37. Use the following independent attributes to find the given F-LUT.

Table 34: **Virtex Bitstream Command Attributes**

Independent Attributes	Values
Chip_Rams	4
FL	14
RAM_Row	2
RAM_Col	0
ram_bit	387
RW	1

Since we are attempting to read only one bit location, only one frame is necessary to be read. We use the equations of Table 15, Table 16, and Table 17 to determine the dependent variables.

Table 35: **Variables, Equations, and Values for Slice 1 F-LUT**

Variables	Equations	Values
MJA_virtex	0 <4/2 ⇒ 2×(4/2 -1 -0)	2
MJA_adj	0 <4/2 ⇒ 2	2
MJA	MJA_virtex + MJA_adj	4
MNA	floor(((387/64)%64)/32)+ 2 x floor(((387/64)%32)/16) + 4 x floor(((387/64)%16)/8) + 8 x floor(((387/64)%8)/4) + 16 x floor(((387/64)%4)/2) + 32 x floor(((387/64)%2)/1)	24
fm_bit_idx	3 + 18 × 19 – 0 + 32	219
fm_st_wd	14 x 24 + 1 x 14	350
fm_wd	floor(219/32)	6
fm_wd_bit_idx	31 + 32 × 6 – 219	4

Commands for reading this memory index are given in Figure 37.

Instruction	Hex	Data 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sync Word	AA99 5566	1	0	1	0	1	0	1	0	1	0	0	1	1	0	0	1	0	1	0	1	0	1	0	1	0	1	1	0	0	1	1	0
Write next (1) word to FAR.	3000 2001	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
CLB MJA = 4, MNA = 24	0208 3000	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Write next word to CMD.	3000 8001	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Register value for RCFG	0000 0004	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Read from FDRO.	2800 601C	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	0
Flush pipe.	0000 0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
(Read 28 words.)																																	

Figure 37: **Commands to read Block SelectRAM index 387**

RAM bit 387 is at fm_wd=6, bit #4.

Frame Word	Frame 32-bit Word																													
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
2	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0
3	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0
4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
5	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1
6	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
7	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
8	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
9	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1
10	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
11	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0
12	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
13	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0

Figure 38: **Frame MNA=24**

Glossary

Block SelectRAM Resource

One of several large, fully-synchronous, dual-port memories in the Virtex FPGAs. Each of these memories contain 4,096 bits. The organization of each memory is configurable. The block SelectRAM resource complements the smaller, distributed, LUT SelectRAMs.

Boundary Scan Interface

One of the configuration interfaces on the Virtex device. This is a bit-serial interface. The Boundary Scan interface is also known as the JTAG port. Also see the SelectMAP interface.

Capture Data

The flip-flop and pad data saved from the logic cells and I/O blocks into the bitstream. Use the CAPTURE_VIRTEX primitive in your HDL code to specify the trigger and clock for the capture operation.

Configurable Logic Block (CLB)

The functional elements for constructing logic circuits. The Virtex CLB is made up of Slices, which contain Logic Cells.

Configuration Bitstream

Configuration commands, optionally with configuration data.

Configuration Commands

Instructions for the Virtex device. There are two classes of Configuration Command — Major and Minor. The Major Commands read and write data to configuration registers in the Virtex device. The Minor commands instruct the Virtex configuration logic to perform specific functions. See "Command Register (CMD)" on page 18.

Configuration Data

Bits that directly define the state of programmable logic. These are written to a Virtex device in a configuration bitstream, and read as Readback Data from a Virtex device.

Configuration Frame

The configuration bits in a Virtex device are organized in columns. A column of CLBs with the I/O blocks above and below the CLBs contain 48 frames of configuration bits. The smallest number of bits that can be read or written through the configuration interfaces is one frame.

Configuration Interface

A logical interface on the Virtex device through which configuration commands and data can be read and written. A interface consists of one or more physical Device Pins.

Configuration Readback

The operation of reading Configuration Data (also known as Readback Data) from a Virtex device.

Device Pin

One of the electrical connections on the package containing the Virtex device.

Frame

See Configuration Frame.

Logic Cell (LC)

The basic building block of the Virtex CLB. An LC includes a 4-input function generator, carry logic, and a storage element.

LUT SelectRAMs

Shallow RAM structures implemented in CLB Lookup Tables (LUTs). See also block SelectRAM section.

Pad

Pad bits are extra bits used to make the total number of bits in a frame an integral multiple of 32, the number of bits in a configuration word. A Pad Word is an extra word used at the end of a Configuration Frame for pipelining. A Pad Frame is an extra Configuration Frame used at the beginning of a Configuration Readback and at the end of a Configuration Write for pipelining.

Readback Data

Configuration data read from a Virtex device. The data is organized as Configuration Frames.

SelectMAP Interface

One of the configuration interfaces on the Virtex device. This is a byte-serial interface. The pins in the SelectMAP interface may be used as user I/O after configuration has been completed or remain configured as a configuration interface.

Slice

A subdivision of the Virtex CLB. There are two, vertical, slices in a Virtex CLB. Each slice contains two Logic Cells.

Sync Word

A 32-bit word with a value that is used to synchronize the configuration logic.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
6/17/99	1.0	Initial Release
7/27/99	1.1	Updated the following tables: Table 5: equation for MNA; Table 7: equations for MJA & fm_bit_idx.
9/20/99	1.2	Changes in page 5. Most formulae in Table 7 have been revised. Documented pad capture value P. Corrected bit locations in Examples.
2/22/00	1.3	Updated to include Virtex-E block SelectRAM. Corrected fm_bit_idx (Right IOB) equations in Table 12 and fm_st_wd definition. Corrected CRC algorithm. Various corrections in Examples. Reformatted and edited document and figures.
6/15/00	1.4	Updated to include Virtex-EM devices in Table 3 and Table 24.

XAPP138 (v2.1) June 15, 2000

Virtex FPGA Series Configuration and Readback

Summary

This application note is offered as complementary text to the configuration section of the Virtex™ data sheet. It is strongly recommended that the Virtex data sheets be reviewed prior to reading this note. Virtex FPGAs offer a broader range of configuration and readback capabilities than previous generations of Xilinx FPGAs. This note first provides a comparison of how Virtex configuration is different from previous Xilinx FPGAs, followed by a complete description of the configuration process and flow. Each of the configuration modes are outlined and discussed in detail, concluding with a complete description of data stream formats, and readback functions and operations.

Introduction

Configuration is the process of loading a design bitstream into the FPGA internal configuration memory. Readback is the process of reading that data.

Virtex configuration logic is significantly different from that of the XC4000 series, but maintains a great deal of compatibility to all Xilinx FPGA families. This information was prepared with the XC4000 series user in mind, but the new user of Xilinx FPGAs need not review XC4000 series configuration-related material.

Virtex Series vs. XC4000 Series Configuration

This section discusses the major configuration differences between the Virtex series and previous Xilinx FPGA families.

Configuration Modes and Daisy-Chains

Virtex FPGAs may be configured in eight different modes, shown in Table 1. There are four primary modes (Master Serial, Slave Serial, SelectMAP, and Boundary Scan), each with the option of having I/Os asserted or floating during configuration.

If pull-ups are selected for configuration, they are only active during configuration. After configuration, unused I/Os are de-asserted.

Serial Modes

The Master and Slave Serial modes perform essentially the same as those of previous FPGA families. For a detailed description, see "Master/Slave Serial Modes" on page 56.

Table 1: **Virtex Configuration Modes**

Configuration Mode	M2	M1	M0	Pull-ups
Master Serial	0	0	0	No
Slave Serial	1	1	1	No
SelectMAP	1	1	0	No
Boundary Scan	1	0	1	No
Master Serial (w/pull-ups)	1	0	0	Yes
Slave Serial (w/pull-ups)	0	1	1	Yes
SelectMAP (w/pull-ups)	0	1	0	Yes
Boundary Scan (w/pull-ups)	0	0	1	Yes

Parallel Modes

The SelectMAP mode is the 8-bit parallel mode for Virtex devices that is similar to Express mode in XC4000XLA and Spartan®-XL. As with these other Xilinx device families, D0 is considered the MSB. For a detailed description, see "SelectMAP Mode" on page 57. Previous users of peripheral modes should find the transition to SelectMAP fairly straight-forward.

Virtex devices do not have a Master Parallel mode. Users who prefer to store configuration data on parallel EPROMs should read the Xilinx application note XAPP137 "Configuring Virtex FPGAs from Parallel EPROMs".

Daisy-Chaining

Virtex FPGAs can be serially daisy-chained for configuration just as all previous Xilinx FPGAs, see "Master/Slave Serial Modes" on page 56. All devices in the chain must be in one of the serial modes. The SelectMAP mode does not support any serial daisy-chaining. Multiple Virtex devices can, however, be configured through the SelectMAP interface in a parallel fashion, see "SelectMAP Mode" on page 57. An example of this is also demonstrated in application note XAPP137 "Configuring Virtex FPGAs from Parallel EPROMs".

Boundary Scan Interface

The Boundary Scan interface is always active from the moment of power-up; before, during, and after configuration. When resetting the configuration memory, $\overline{\text{PROGRAM}}$ going Low also resets the JTAG TAP controller. Boundary Scan modes select the optional pull-ups and prevent configuration in any other modes.

Configuring Virtex devices through the Boundary Scan interface is not described in this note. For more information on the Virtex Boundary Scan interface, refer to application note XAPP139 "Configuration and Readback of Virtex FPGAs Using (JTAG) Boundary Scan".

Initialization and Timing

The initialization sequence for Virtex devices is somewhat simpler than for previous FPGAs. Upon power-up, the $\overline{\text{INIT}}$ signal is held Low while the FPGA initializes the internal circuitry and clears the internal configuration memory. Configuration may not commence until this cycle is complete, indicated by the positive transition of $\overline{\text{INIT}}$. Previous FPGA families required an additional waiting period after $\overline{\text{INIT}}$ went High before configuration could begin, Virtex devices do not. As soon as $\overline{\text{INIT}}$ transitions High after power-up, configuration may start. The Virtex configuration logic does, however, require several CCLK transitions to initialize itself. For this purpose, the Virtex bitstream is padded with several dummy data words at the beginning of the configuration stream. See "Bitstream Format" on page 61.

Mixed Voltage Environments

Virtex devices have separate voltage sources for the internal core circuitry (V_{CORE} = 2.5V) and the I/O circuitry (SelectI/O). The SelectI/O resource is separated into eight banks of I/O groups. Each bank may be configured with one of several I/O standards. Refer to the Virtex data sheets for I/O banking rules and available I/O standards. Before and during configuration, all I/O banks are set for the LVTTL standard, which requires an output voltage (V_{CCO}) of 3.3V for normal operation.

All configuration pins are located within banks 2 and 3. Therefore, only V_{CCO_2} and V_{CCO_3} pins need a 3.3V supply for output configuration pins to operate normally. This is a requirement for Master Serial configuration and readback through the SelectMAP ports.

If the FPGA is being configured in Master Serial mode, and banks 2 and 3 are being configured for an I/O standard that requires a V_{CCO} other than 3.3V, then V_{CCO_2} and V_{CCO_3} need to be switched from the 3.3V used during configuration to the voltage required after configuration.

If readback is performed through the SelectMAP mode after configuration, then V_{CCO_2} and V_{CCO_3} require a 3.3V supply after configuration as well.

For Serial Slave and SelectMAP configuration modes, V_{CCO} can be any voltage (as long as it is ≥ 1.8V ≤ 3.3V) provided one meets the V_{IH}/V_{IL} levels of the resulting input buffer (see data sheet). Any pin that is a shared I/O, such as INIT, DOUT/BUSY, and DONE should have an added pull-up resistor or utilize the internal pull-up resistors. The dedicated CONFIG and JTAG pins should be pulled up to at least V_{CCINT} (1.8V). Additionally, V_{CCO_2} must be pulled to a value above 1.0V during power-up of the FPGA.

JTAG inputs are independent of V_{CCO} and work between 2.5V and 3.3V TTL levels. TDO is sourced from V_{CCO_2} and should be 1.8V, 2.5V, or 3.3V depending on what the TDI of the next device accepts.

BitGen Switches and Options

This section describes new optional settings for bitstream generation that pertain only to Virtex devices. The new BitGen options are listed in Table 2 and described below.

Table 2: **Virtex-Specific BitGen Options**

Switch	Default Setting	Optional Setting
Readback	N/A	N/A
ConfigRate MHz (nominal)	4	4, 5, 7, 8, 9, 10, 13, 15, 20, 26, 30, 34, 41, 45, 51, 55, 60
StartupClk	CCLK	UserClk, JtagClk
DONE_cycle	4	1, 2, 3, 5, 6
GTS_cycle	5	1, 2, 3, 4, 6, DONE
GSR_cycle	6	1, 2, 3, 4, 5, DONE
GWE_cycle	6	1, 2, 3, 4, 5, DONE
LCK_cycle	NoWait	0, 1, 2, 3, 4, 5, 6
Persist	No	X1, X8
DriveDONE	No	Yes
DonePipe	No	Yes
Security	None	Level1, Level2
UserID	N/A	<hex string> (32-bit)
Gclkdel0	N/A	<binary string>
Gclkdel1	N/A	<binary string>
Gclkdel2	N/A	<binary string>
Gclkdel3	N/A	<binary string>

Readback

The Readback option causes BitGen to write out a readback command file `<design>.rbb`. For more information, see "Readback" on page 70.

ConfigRate

The ConfigRate is the internally generated frequency of CCLK in Master Serial mode. The initial frequency is 2.5 MHz. The CCLK changes to the selected frequency after the first 60 bytes of the bitstream have been loaded. For details, see "Bitstream Format" on page 61. It should also be noted that the CCLK periods have a variance of – 30% to +45% from the specified value.

StartupClk

The StartupClk option selects a clock source to synchronize the Start-up Sequence. The default is CCLK which is standard for most configuration schemes. However, some applications require that the Start-up Sequence be synchronized to another clock source (UserClk) which must be specified in the user design. If configuring in Boundary Scan, select the JTAGClk option. For more information on Boundary Scan, refer to application note XAPP139 "Configuration and Readback of Virtex FPGAs Using (JTAG) Boundary Scan".

DONE_cycle

The DONE_cycle specifies which state of the Start-up Sequence releases the DONE pin. For more information on the Start-up Sequence, see "Start-up Sequence" on page 51.

GSR_cycle

The GSR_cycle specifies which state of the Start-up Sequence releases the internal GlobalSetReset signal. The GSR signal holds all internal flip-flops in their configured initial state. The DONE setting asserts the GSR asynchronously as DONE transitions High unless the DonePipe option is used. If the DonePipe option is used, it releases GSR on the first rising edge of the StartupClk after DONE transitions High.

GWE_cycle

The GWE_cycle specifies which state in the Start-up Sequence releases the internal GlobalWriteEnable signal. This signal is not accessible to the user. It keeps all flip-flops, and RAM from changing state. However, DLL is not affected by GWE. The DONE setting asserts GWE asynchronously as DONE transitions High unless the DonePipe option is used. If the DonePipe option is used, it releases GWE on the first rising edge of the StartupClk after DONE transitions High.

GTS_cycle

The GTS_cycle specifies which cycle of the Start-up Sequence releases the internal Global 3-state signal. The GTS signal holds all outputs disabled. The DONE setting asserts the GTS asynchronously as DONE transitions High unless the DonePipe option is used. If the DonePipe option is used, it releases GSR on the first rising edge of the StartupClk after DONE transitions High.

LCK_cycle

The LCK_cycle specifies in which state the Start-up Sequence should stay until a DLL has established a Lock. The default setting of *NoWait* is used whenever a DLL is not used in a design. When a DLL is used, the Start-up Sequence should not be delayed for a DLL lock. If a wait state is specified by this option, the Start-up Sequence proceeds to the specified state, but then waits in that state until DLL lock occurs.

Since there are four DLLs per device, the LCK_cycle option must be used with a DLL attribute in the design. For more information on DLL attributes, see application note XAPP132 "Using the Virtex Delay-Locked Loop".

Persist

If the Persist option is unspecified, or specified with a default setting of *No*, then all configuration pins other than CCLK, $\overline{\text{PROGRAM}}$, and DONE become user I/O after configuration. The Persist switch causes the configuration pins to retain their configuration function even after configuration. The *X1* setting is reserved for future use and should not be used. The *X8* setting applies to the SelectMAP interface and *X8* setting must be selected if readback is to be performed through the SelectMAP interface. The Persist switch does not affect Boundary Scan ports.

DriveDONE

By default, the DONE pin is an open-drain driver. However, if the DriveDONE option is set to *Yes*, then DONE becomes an active driver, and no external pull-up is needed.

DonePipe

Independent of the DONE_cycle setting, after releasing DONE, the Start-up Sequence waits for DONE to be externally asserted High before continuing. The rise time of DONE depends on its external capacitive loading and is less than one CCLK period.

The DonePipe option adds a pipeline register stage between the DONE pin and the start-up circuitry. Useful for high configuration speeds when the rise time for DONE cannot be faster than one CCLK period.

Security

Security level settings restrict access to configuration and readback operations. If the Persistence option is not set, then configuration ports are not available after configuration. However, the Boundary Scan ports are always active and have access to configuration and readback.

Setting security *Level 1* disables all readback functions from either the SelectMAP or Boundary Scan ports.

Setting security *Level 2* disables all configuration and readback functions from all configuration and Boundary Scan ports.

The only way to remove a security level in a configured device is to de-configure it by asserting $\overline{\text{PROGRAM}}$ or recycling power.

UserID

The UserID is a 32-bit data word accessible through the Boundary Scan USERCODE command. The data word can be any arbitrary 32-bit value. To include a UserID in a bitstream, set the UserID option to the HEX representation of the desired data word <XXXXXXXX>h.

Gclkdel

The Gclkdel option adds delay to one of the four global clock buffers. This option is only used in PCI applications.

CCLK and LengthCount

Previously, Xilinx FPGA families used a LengthCount number embedded in the bitstream. This LengthCount number indicated to the FPGA how many CCLK cycles should be observed before activating the Start-up Sequence to activate the FPGA. This method also requires the FPGA not to receive any CCLK transitions prior to the loading of the bitstream. Otherwise, the LengthCount would be wrong and the Start-up Sequence would not activate at the appropriate time. Thus, free-running oscillators can not be used to generate the CCLK for configuration.

Virtex FPGAs do not use any such lengthcount number in configuration bitstreams. The Start-up Sequence for Virtex devices is controlled by a set of configuration commands that are embedded near the end of the configuration bitstream. See "Bitstream Format" on page 61. Therefore, Virtex FPGAs may have a free running oscillator driving the CCLK pin.

Start-up Sequence

Start-up is the transition from the configuration state to the operational state. The Start-up Sequence activates an FPGA upon the successful completion of configuration. The Start-up Sequencer is an 8-phase sequential state machine that transitions from phase 0 to phase 7. See Figure 1.

The Start-up Sequencer performs the following tasks:

1. Releases the DONE pin.

2. Negates GTS, activating all the I/Os.
3. Asserts GWE, allowing all RAMs and flip-flops to change state (flip-flops cannot change state while GSR is asserted).
4. Negates GSR, allowing all flip-flops to change state.
5. Asserts EOS. The End-Of-Start-up flag is always set in phase 7. This is an internal flag that is not user accessible.

The order of the Start-up Sequence is controlled by BitGen options. The default Start-up Sequence is the bold line shown in Figure 1. The Start-up Sequence may also be stalled at any phase until either DONE has been externally forced High, or a specified DLL has established LOCK. For details, See "BitGen Switches and Options" on page 49.

At the cycle selected for the DONE to be released, the sequencer always waits in that state until the DONE is externally released. This is similar to the SyncToDONE behavior in the XC4000 FPGAs. However, this does not hold off the GTS, GSR, or GWE if they are selected to be released prior to DONE. Therefore, DONE is selected first in the sequence for default settings.

For a true SyncToDONE behavior, set the GTS, GSR, and GWE cycles to a value of DONE in the BitGen options. This causes these signals to transition as DONE externally transitions High.

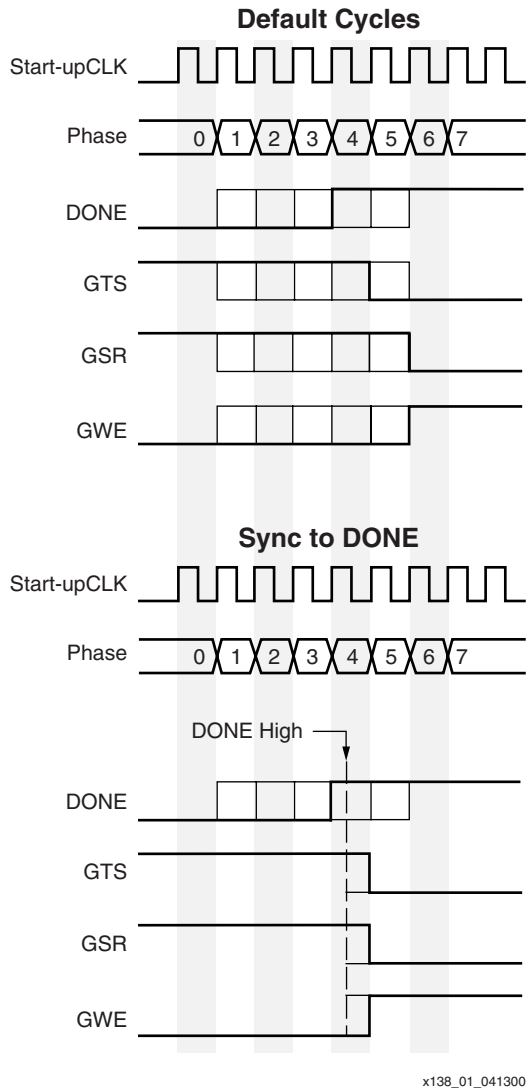


Figure 1: **Default Start-up Sequence**

Configuration Process and Flow

The external configuration process is simply a matter of loading the configuration bitstream into the FPGA using the selected configuration mode. The configuration process follows the flow illustrated in Figure 2.

Power-Up

The V_{CCint} power pins must be supplied with a 2.5V source. The rise time for the core voltage should be a maximum of 50 ms to rise from 1.0V to 2.4V. The IOB output voltage input for Bank 2 (V_{CCO_2}) is also used as a logic input to the Power-On-Reset (POR) circuitry. This value must be greater than 1.0V for power-up to continue. If this bank is not being used, a pull-up should be added to V_{CCO_2}.

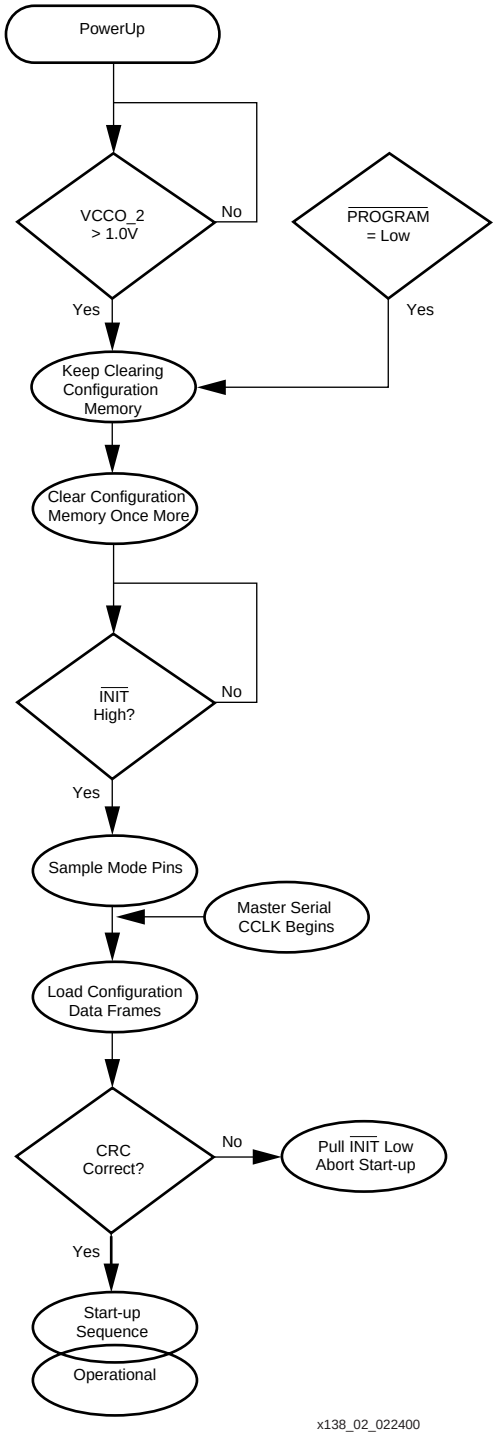


Figure 2: **Configuration Flow Diagram**

Clearing Configuration Memory

After power-up, the configuration memory is automatically cleared. The $\overline{\text{INIT}}$ pin transitions High when the clearing of configuration memory is complete. A logic Low on the $\overline{\text{PROGRAM}}$ input resets the configuration logic and holds the FPGA in the clear configuration memory state. As long as the $\overline{\text{PROGRAM}}$ pin is held Low, the FPGA continues to clear its configuration memory while holding $\overline{\text{INIT}}$ Low to indicate the configuration memory is being cleared. When $\overline{\text{PROGRAM}}$ is released, the FPGA continues to hold $\overline{\text{INIT}}$ Low until it has completed clearing all

the configuration memory. The minimum Low pulse time for $\overline{\text{PROGRAM}}$ is 300 ns. There is no maximum value.

Delaying Configuration

The $\overline{\text{INIT}}$ pin may also be held Low externally to delay configuration of the FPGA. The FPGA samples its mode pins on the rising edge of $\overline{\text{INIT}}$. After $\overline{\text{INIT}}$ has gone High, configuration may begin. No additional time-out or waiting periods are required, but configuration does not need to commence immediately after the transition of $\overline{\text{INIT}}$. The configuration logic does not begin processing data until the synchronization word from the bitstream is loaded.

Loading Configuration Data

The details of loading the configuration data are discussed in the following sections of the configuration modes, see "Master/Slave Serial Modes" on page 56 and "SelectMAP Mode" on page 57.

CRC Error Checking

Twice during the loading of configuration data, an embedded CRC value is checked against an internally calculated CRC value. The first check is just before the last configuration frame is loaded, and the second is at the very end of configuration. If the CRC values do not match, $\overline{\text{INIT}}$ is asserted Low to indicate that a CRC error has occurred. Start-up is aborted, and the FPGA does not become active.

To reconfigure the device, the $\overline{\text{PROGRAM}}$ pin should be asserted to reset the configuration logic. Recycling power also resets the FPGA for configuration. For more information on CRC calculation, see "Cyclic Redundancy Checking Algorithm" on page 69.

Start-up and Operational States

Upon successful completion of the final CRC check, the FPGA enters the Start-up Sequence. This sequence releases DONE (it goes High), activates the I/Os, de-asserts GSR, and asserts GWE. At this point, the FPGA becomes active and functional with the loaded design. For more information on start-up, see "Start-up Sequence" on page 51.

Configuration Pins

Certain pins in the FPGA are designated for configuration and are listed in Table 3. Some pins are dedicated to the configuration function and others are dual-function pins that can be user I/O after configuration.

Table 3: **List of Configuration Pins**

Name	Direction	Driver Type	Description
Dedicated Pins			
CCLK	Input/Output	Active	Configuration clock. Output in Master mode.
PROGRAM	Input		Asynchronous reset to configuration logic.
DONE	Input/Output	Active/ Open-Drain	Configuration status and start-up control.
M2, M1, M0	Input		Configuration mode selection.
TMS	Input		Boundary Scan mode select.
TCK	Input		Boundary Scan clock.
TDI	Input		Boundary Scan data input.
TDO	Output	Active	Boundary Scan data output.

Table 3: **List of Configuration Pins *(Continued)***

Name	Direction	Driver Type	Description
Dual Function Pins			
DIN (D0)	Input		Serial configuration data input.
D1:D7	Input/Output	Active Bidirectional	SelectMAP configuration data input, readback data output.
CS	Input		Chip Select (SelectMAP mode only).
WRITE	Input		Active Low write select, read select (SelectMAP only).
BUSY/DOUT	Output	Open-Drain/Active	Busy/Ready status for SelectMAP mode (open-drain). Serial configuration data output for serial daisy-chains (active).
INIT	Input/Output	Open-Drain	Delay configuration, indicate configuration error.

Master/Slave Serial Modes

In serial configuration mode, the FPGA is configured by loading one bit per CCLK cycle. In Master Serial mode, the FPGA drives the CCLK pin. In Slave Serial mode, the FPGAs CCLK pin is driven by an external source. In both serial configuration modes, the MSB of each data byte is always written to the DIN pin first.

The Master Serial mode is designed so the FPGA can be configured from a Serial PROM (Figure 3). The speed of the CCLK is selectable by BitGen options, see "BitGen Switches and Options" on page 49. Be sure to select a CCLK speed supported by the SPROM.

The Slave Serial configuration mode allows for FPGAs to be configured from other logic devices, such as microprocessors, or in a daisy-chain fashion. Figure 3 shows a Master Serial FPGA configuring from an SPROM with a Slave Serial FPGA in a daisy-chain with the Master.

Daisy-Chain Configuration

Virtex FPGAs may only be daisy-chained with XC4000X, SpartanXL, Spartan-II or other Virtex FPGAs for configuration. There are no restrictions on the order of the chain. However, if a Virtex FPGA is placed as the Master and a non-Virtex FPGA is placed as a slave, select a configuration CCLK speed supported by all devices in the chain.

The separate bitstreams for the FPGAs in a daisy-chain are required to be combined into a single PROM file by using either the PROM File Formatter or the PROMgen utility. Separate PROM files may not be simply concatenated together to form a daisy-chain bitstream.

The first device in the chain is the first to be configured. No data is passed onto the DOUT pin until all the data frames, start-up command, and CRC check have been loaded. CRC checks only include the data for the current device, not for any others in the chain. After finishing the first stream, data for the next device is loaded. The data for the downstream device appears on DOUT typically about 40 CCLK cycles after being loaded into DIN. This is due to internal packet processing. Each daisy-chained bitstream carries its own synchronization word. Nothing of the first bitstream is passed to the next device in the chain other than the daisy-chained configuration data.

The DONE_cycle must be set before GTS and GSR, or the GTS_cycle and GSR_cycle must be set to the value DONE for the Start-up Sequence of each Virtex device not to begin until all of the DONE pins have been released. When daisy-chaining multiple Virtex devices, either set the last device in the chain to DriveDONE, or add external pull-up resistors to counteract the combined capacitive loading on DONE. If non-Virtex devices are included in the daisy-chain, it

is important to set their bitstreams to SyncToDONE with BitGen options. For more information on Virtex BitGen options, see "BitGen Switches and Options" on page 49.

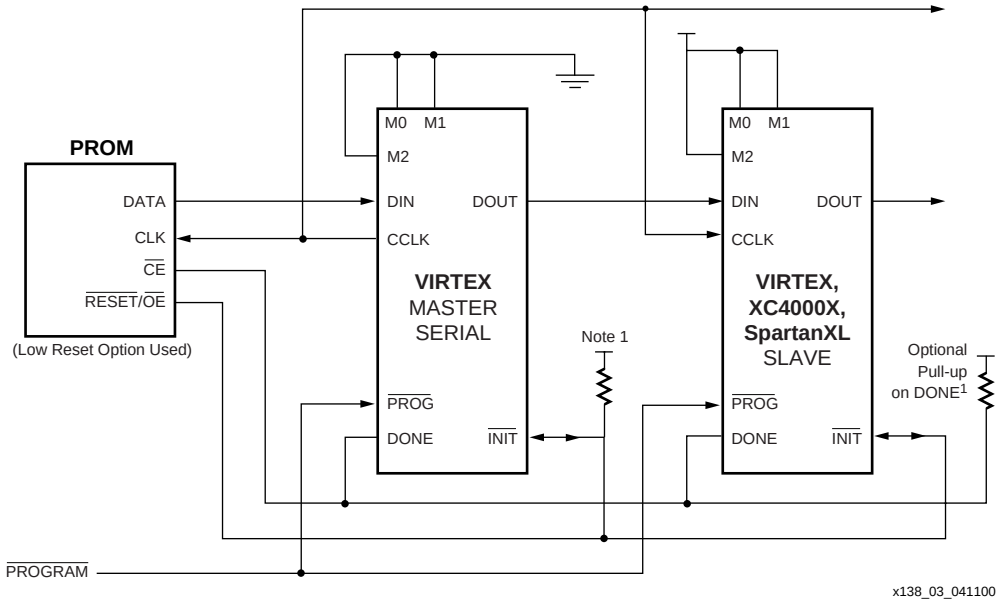


Figure 3: **Master/Slave Serial Mode Circuit Diagram**

Notes:

1. If no Virtex device is selected to DriveDONE, an external pull-up of 330Ω should be added to the common DONE line. With SpartanXL devices a 4.7KΩ pull-up resistor should be added to the common DONE line. This pull-up is not needed if DriveDONE is selected. DriveDONE should only be selected for the last device in the configuration chain.

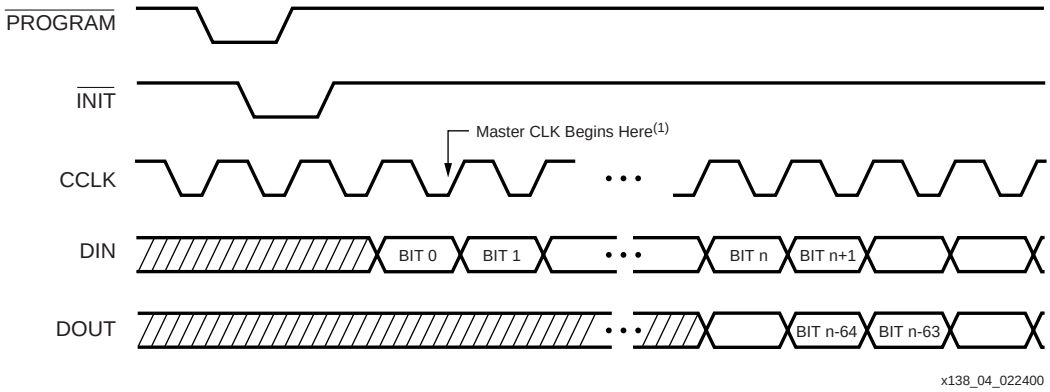


Figure 4: **Serial Configuration Clocking Sequence**

Notes:

1. For Slave configurations a free running CCLK may be used as indicated in Figure 4. For Master configurations, the CCLK does not transition until after initialization as indicated by the arrow.

SelectMAP Mode

The SelectMAP mode provides an 8-bit bidirectional data bus interface to the Virtex configuration logic that may be used for both configuration and readback. Virtex devices may not be serially daisy-chained when the SelectMAP interface is used. However, they may be connected in a parallel-chain as shown in Figure 5. The DATA pins (D0:D7), CCLK, WRITE, BUSY, PROGRAM, DONE, and INIT may be connected in common between all of the devices.

$\overline{CS}$ inputs should be kept separate so each device may be accessed individually. If all devices are to be configured with the same bitstream, readback is not being used, and CCLK is less than 50 MHz, the $\overline{CS}$ pins may be connected to a common line so the devices are configured simultaneously.

Although Figure 5 does not show a control module for the SelectMAP interface, the SelectMAP interface is typically driven by a processor, micro controller, or some other logic device such as an FPGA or a CPLD.

DATA Pins (D[0:7])

The D0 through D7 pins function as a bidirectional data bus in the SelectMAP mode. Configuration data is written to the bus, and readback data is read from the bus. The bus direction is controlled by the $\overline{WRITE}$ signal. See "Bitstream Format" on page 61. The D0 pin is considered the MSB bit of each byte.

$\overline{WRITE}$

When asserted Low, the $\overline{WRITE}$ signal indicates that data is being written to the data bus. When asserted High, the $\overline{WRITE}$ signal indicates that data is being read from the data bus.

$\overline{CS}$

The Chip Select input ($\overline{CS}$) enables the SelectMAP data bus. To write or read data onto or from the bus, the $\overline{CS}$ signal must be asserted Low. When $\overline{CS}$ is High, Virtex devices do not drive onto or read from the bus.

BUSY

When $\overline{CS}$ is asserted, the BUSY output indicates when the FPGA can accept another byte. If BUSY is Low, the FPGA reads the data bus on the next rising CCLK edge where both $\overline{CS}$ and $\overline{WRITE}$ are asserted Low. If BUSY is High, the current byte is ignored and must be reloaded on the next rising CCLK edge when BUSY is Low. When $\overline{CS}$ is not asserted, BUSY is tri-stated.

BUSY is only necessary for CCLK frequencies above 50 MHz. For frequencies at or below 50 MHz, BUSY is ignored, see "Express-Style Loading" on page 59. For parallel chains, as shown in Figure 5, where the same bitstream is to be loaded into multiple devices simultaneously, BUSY should not be used. Thus, the maximum CCLK frequency for such an application must be less than 50 MHz.

CCLK

The CCLK pin is a clock input to the SelectMAP interface that synchronizes all loading and reading of the data bus for configuration and readback. Additionally, the CCLK drives internal configuration circuitry. The CCLK may be driven either by a free running oscillator or an externally-generated signal.

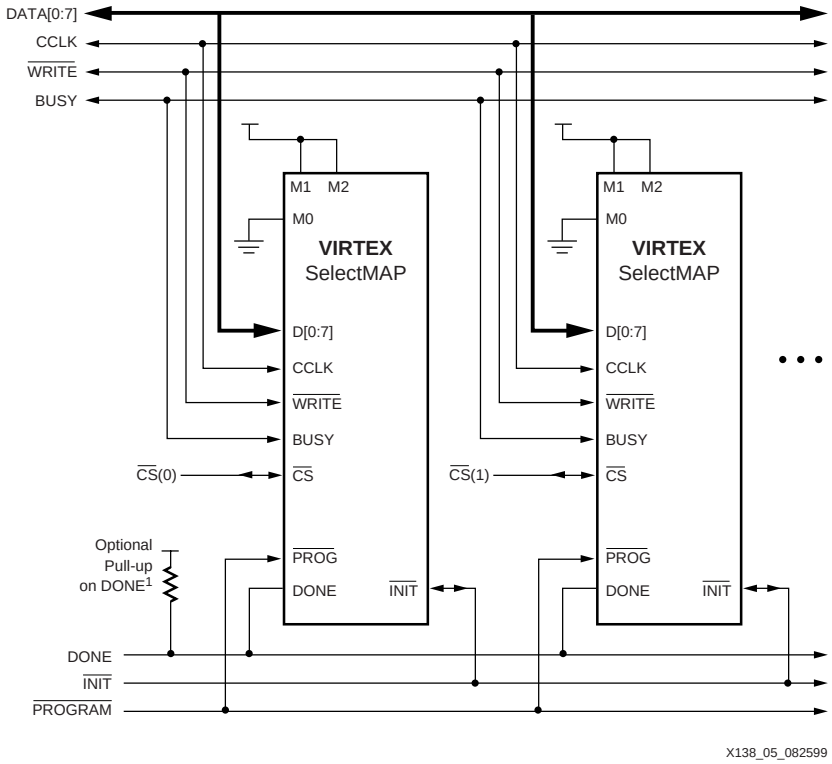


Figure 5: **SelectMAP Mode Circuit Diagram**

Notes:

1. If none of the Virtex devices have been selected to DriveDONE, add an external pull-up of 330Ω should be added to the common DONE line. This pull-up is not needed if DriveDONE is selected. DriveDONE should only be selected for the last device in the configuration chain.

Free-Running CCLK

A free-running oscillator may be used to drive Virtex CCLK pins. For applications that can provide a continuous stream of configuration data, refer to the timing diagram discussed in "Express-Style Loading" on page 59. For applications that cannot provide a continuous data stream, missing the clock edges, refer to the timing diagram discussed in "Non-Contiguous Data Strobe" on page 60. An alternative to a free-running CCLK is discussed in "Controlled CCLK" on page 61.

Express-Style Loading

In express-style loading, a data byte is loaded on every rising CCLK edge as shown in Figure 6. If the CCLK frequency is less than 50 MHz, this can be done without handshaking. For frequencies above 50 MHz, the BUSY signal must be monitored. If BUSY is High, the current byte must be reloaded when BUSY is Low.

The first byte may be loaded on the first rising CCLK edge that $\overline{INIT}$ is High, and when both $\overline{CS}$ and $\overline{WRITE}$ are asserted Low. $\overline{CS}$ and $\overline{WRITE}$ may be asserted anytime before or after $\overline{INIT}$ has gone High. However, the SelectMAP interface is not active until after $\overline{INIT}$ has gone High. The order of $\overline{CS}$ and $\overline{WRITE}$ does not matter, but $\overline{WRITE}$ must be asserted throughout configuration. If $\overline{WRITE}$ is de-asserted before all data has been loaded, the FPGA aborts the operation. To complete configuration, the FPGA must be reset by $\overline{PROGRAM}$ and reconfigured with the entire stream. For applications that need to de-assert $\overline{WRITE}$ between bytes, see "Controlled CCLK" on page 61.

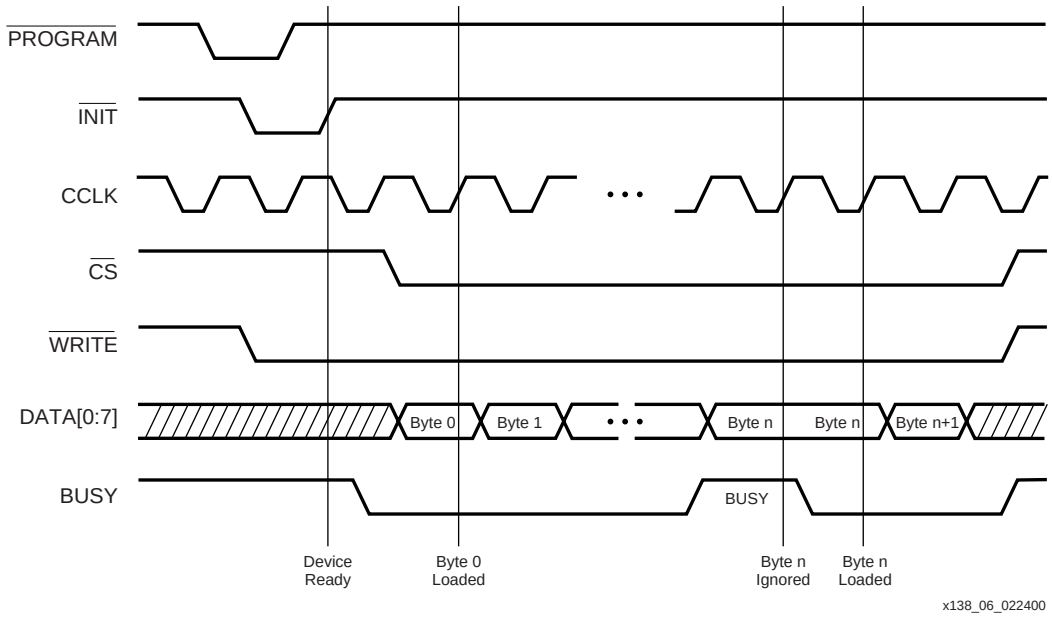


Figure 6: **"Express Style" Continuous Data Loading in SelectMAP**

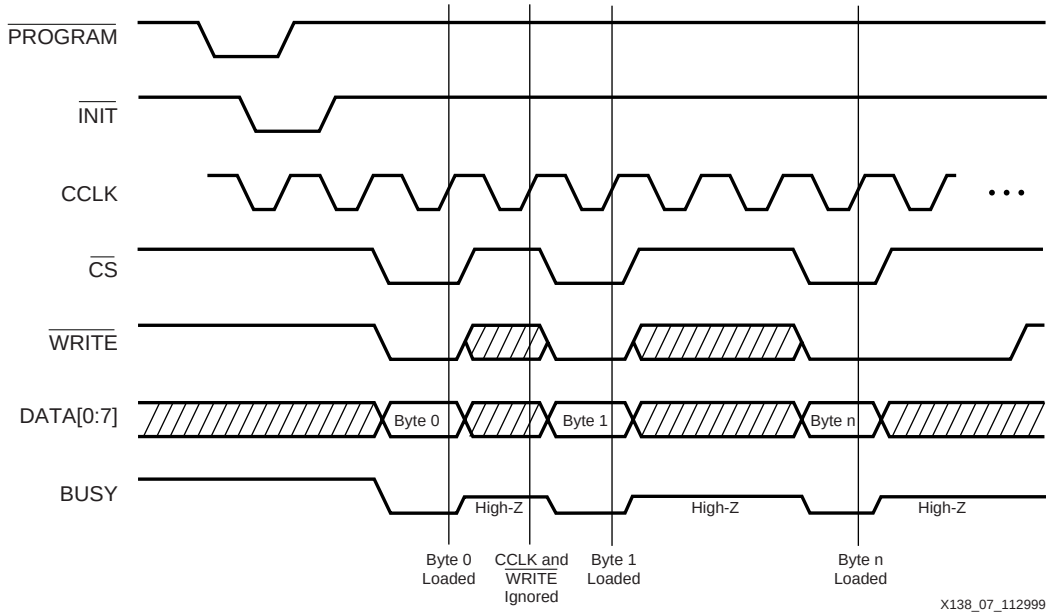


Figure 7: **Separating Data Loads by Multiple CCLK Cycles Using $\overline{CS}$**

Non-Contiguous Data Strobe

In applications where multiple clock cycles may be required to access the configuration data before each byte can be loaded into the SelectMAP interface, data may not be ready for each consecutive CCLK edge. In such a case, the $\overline{CS}$ signal may be de-asserted until the next data byte is valid on the DATA[0:7] pins. This is demonstrated in Figure 7. While $\overline{CS}$ is High, the SelectMAP interface does not expect any data and ignores all CCLK transitions. However, $\overline{WRITE}$ must continue to be asserted while $\overline{CS}$ is asserted. If $\overline{WRITE}$ is High during a positive CCLK transition while $\overline{CS}$ is asserted, the FPGA aborts the operation. For applications that need to de-assert the $\overline{WRITE}$ signal without de-asserting $\overline{CS}$, see "Controlled CCLK" on page 61.

Controlled CCLK

Some applications require that $\overline{\text{WRITE}}$ be de-asserted between the loading of configuration data bytes asynchronously from the $\overline{\text{CS}}$. Typically, this would be due to the $\overline{\text{WRITE}}$ signal being a common connection to other devices on the board, such as memory storage elements. In such a case, driving CCLK as a controlled signal instead of a free-running oscillator makes this type of operation possible. In Figure 8, the CCLK, $\overline{\text{CS}}$, and $\overline{\text{WRITE}}$ are asserted Low while a data byte becomes active. Once the CCLK has gone High, the data is loaded. $\overline{\text{WRITE}}$ may be de-asserted and re-asserted as many times as necessary, just as long as it is Low before the next rising CCLK edge.

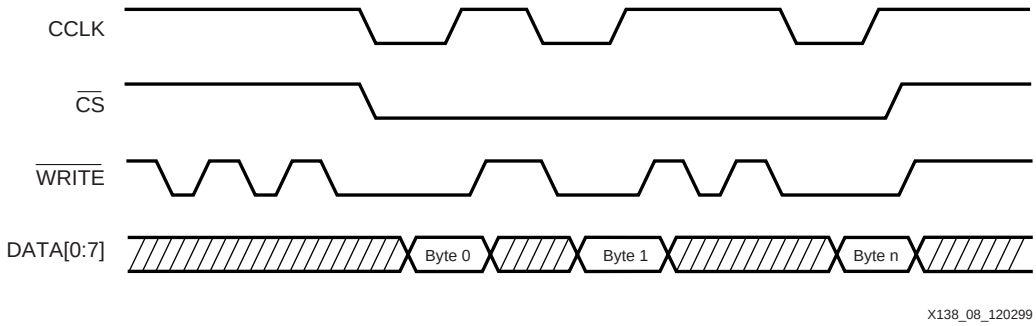


Figure 8: **Controlling CCLK for $\overline{\text{WRITE}}$ De-assertion**

Bitstream Format

The Virtex bitstream has a very different format from that of all other Xilinx FPGAs. The typical FPGA user does not need a bit-level understanding of the configuration stream. However, for the purpose of debugging, designing embedded readback operations, or otherwise complex styles of configuring multiple FPGAs, a review of the bitstream format is recommended. Therefore, this section describes the Virtex bitstream, the internal configuration logic, and the internal processing of configuration data.

Data Frames

The internal configuration memory is partitioned into segments called "Frames." The portions of the bitstream that actually get written to the configuration memory are "Data Frames." The number and size of frames varies with device size as shown in Table 4. The total number of configuration bits for a particular device is calculated by multiplying the number of frames by the number of bits per frame, and then adding the total number of bits needed to perform the *Configuration Register Writes* shown in Table 7.

Table 4: **Virtex Configuration Data Frames**

Device	Frames	Bits per Frame	Configuration Bits
XCV50	1453	384	559,232
XCV50E	1637	384	629,888
XCV100	1741	448	781,248
XCV100E	1925	448	863,680
XCV150	2029	512	1,040,128
XCV200	2317	576	1,335,872
XCV200E	2501	576	1,441,856
XCV300	2605	672	1,751,840
XCV300E	2789	672	1,875,488

Table 4: **Virtex Configuration Data Frames *(Continued)***

Device	Frames	Bits per Frame	Configuration Bits
XCV400	3181	800	2,546,080
XCV400E	3365	800	2,693,280
XCV405E	4285	800	3,429,280
XCV600	3757	960	3,608,000
XCV600E	4125	960	3,961,280
XCV800	4333	1088	4,715,584
XCV812E	5989	1088	6,517,312
XCV1000	4909	1248	6,127,712
XCV1000E	5277	1248	6,586,976
XCV1600E	6037	1376	8,308,192
XCV2000E	6613	1536	10,158,848
XCV2600E	7477	1728	12,921,536
XCV3200E	8341	1952	16,282,912

Configuration Registers

Table 5: **Internal Configuration Registers**

Symbol	Register Name	Address
CMD	Command	0100b
FLR	Frame Length	1011b
COR	Configuration Option	1001b
MASK	Control Mask	0110b
CTL	Control	0101b
FAR	Frame Address	0001b
FDRI	Frame Data Input	0010b
CRC	Cyclic Redundancy Check	0000b
FDRO	Frame Data Output	0011b
LOUT	Daisy-chain Data Output (DOUT)	1000b

The Virtex configuration logic was designed so that an external source may have complete control over all configuration functions by accessing and loading addressed internal configuration registers over a common configuration bus. The internal configuration registers that are used for configuration and readback are listed in Table 5. All configuration data, except the synchronization word and dummy words, is written to internal configuration registers.

Command Register (CMD)

The CMD is used to execute the commands shown in Table 6. These commands are executed by loading the binary code into the CMD register.

Table 6: **CMD Register Commands**

Symbol	Command	Binary Code
RCRC	Reset CRC Register	0111b
SWITCH	Change CCLK Frequency	1001b
WCFG	Write Configuration Data	0001b
RCFG	Read Configuration Data	0100b
LFRM	Last Frame Write	0011b
START	Begin Start-Up Sequence	0101b

Frame Length Register (FLR)

The FLR is used to indicate the frame size to the internal configuration logic. This allows the internal configuration logic to be identical for all Virtex devices. The value loaded into this register is the number of actual configuration bits that get loaded into the configuration memory frames. The actual frame sizes in the bitstream, shown in Table 4, are slightly longer than the FLR value to account for internal pipelining and rounding up to the nearest 32-bit word.

Configuration Option Register (COR)

The COR is loaded with the user selected options from bitstream generation. See "BitGen Switches and Options" on page 49.

Control Register (CTL)

The CTL controls internal functions such as *Security* and *Port Persistence*.

Mask Register (MASK)

The MASK is a safety mechanism that controls which bits of the CTL register can be reloaded. Prior to loading new data into the CTL register, each bit must be independently enabled by its corresponding bit in the MASK register. Any CTL bit not selected by the MASK register is ignored when reloading the CTL register.

Frame Address Register (FAR)

The FAR sets the starting frame address for the next configuration data input write cycle.

Frame Data Register Input (FDRI)

The FDRI is a pipeline input stage for configuration data frames to be stored in the configuration memory. Starting with the frame address specified in the FAR, the FDRI writes its contents to the configuration memory frames. The FDRI automatically increments the frame address after writing each frame for the number of frames specified in the FDRI write command. This is detailed in the next section.

CRC Register (CRC)

The CRC is loaded with a CRC value that is embedded in the bitstream and compared against an internally calculated CRC value. Resetting the CRC register and circuitry is controlled by the CMD register.

Frame Data Register Output (FDRO)

The FDRO is an outgoing pipeline stage for reading frame data from the configuration memory during readback. This works the same as the FDRI but with the data flowing in the other direction.

Legacy Data Output Register (LOUT)

The pipeline data to be sent out the DOUT pin for serially daisy-chained configuration data output.

Configuration Data Processing Flow

The complete (standard) reconfiguration of a Virtex device internally follows the flow chart shown in Figure 9. All the associated commands to perform configuration are listed in Table 7.

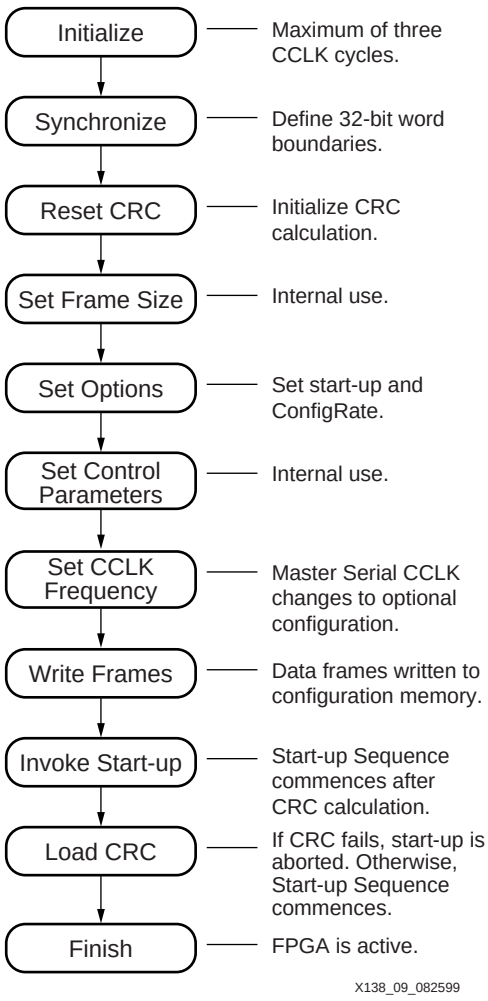


Figure 9: **Internal Configuration Processing Flow**

Table 7: **Configuration Register Writes**

Type	32-bit Words
Command Set 1	
Dummy words	(See Note 1)
Synchronization word	1
Write CMD (RCRC)	2
Write FLR	2
Write COR	2
Write CMD (SWITCH)	2
Command Set 2	
Write FAR	2
Write CMD (WCFG)	2
Write FDRI	2
Write FAR	2
Write FDRI	1
Write FAR	2
Write FDRI	1
Write CRC	2
Write CMD (LFRM)	2
Write FDRI	1
Command Set 3	
Write CMD (START)	2
Write MASK	2
Write CTL	2
Write CRC	2
Dummy words	4
TOTAL	40

Notes:

1. Different versions of BitGen may insert fewer dummy words at the beginning of the stream.

The first command set prepares the internal configuration logic for the loading of the data frames. The internal configuration logic is first initialized with several CCLK cycles represented by dummy words, and then synchronized to recognize the 32-bit word boundaries by the synchronization word. The CRC register and circuitry must then be reset by writing the RCRC command to the CMD register. The frame length size for the device being configured is then loaded into the FLR register. The configuration options are loaded into the COR. The CCLK frequency selected is specified in the COR; however, to switch to that frequency the SWITCH command must be loaded into the CMD register. Now the data frames can be loaded.

The second command set loads the configuration data frames. First, a WCFG (Write Configuration) command is loaded into the CMD register activating the circuitry that writes the data loaded into the FDRI into the configuration memory cells. To load a set of data frames, the starting address for the first frame is first loaded to the FAR, followed by a write command, and then by the data frames to the FDRI. The FDRI write command also specifies the amount of data that is to follow in terms of the number of 32-bit words that comprise the data frames being

written. Typically, three large sets of frames are loaded by this process. When all but the last frame has been loaded, an initial CRC checksum is loaded into the CRC register. The Last Frame command (LFRM) is loaded into the CMD register followed by a final FDRI write command and the last data frame into the FDRI register.

The third command set initializes the Start-up Sequence and finishes CRC checking. After all the data frames have been loaded, the START command is loaded into the CMD register, followed by any internal control data to the CTL and by the final CRC value into the CRC register. The four dummy words at the end are flushed through the system to provide the finishing CCLK cycles to activate the FPGA.

The Standard Bitstream

Virtex devices have the ability to be only partially re-configured or read back; however, this topic is beyond the scope of this note. For more information on partial configuration, refer to application note XAPP151 "Virtex Configuration Architecture User Guide". The standard bitstream, currently generated by BitGen, follows the format shown in Table 8, Table 9, and Table 10. **This format assumes D0 is considered the MSB**. It is divided into three tables to follow the three command sets described in the previous subsection.

Table 8 shows the first set of commands in the bitstream that prepare the configuration logic for rewriting the memory frames. All commands are described as 32-bit words, since configuration data is internally processed from a common 32-bit bus.

From Table 8, the first two dummy words pad the front of the bitstream to provide the clock cycles necessary for initialization of the configuration logic. No actual processing takes place until the synchronization word is loaded. Since the Virtex configuration logic processes data as 32-bit words, but may be configured from a serial or 8-bit source, the synchronization word is used to define the 32-bit word boundaries. That is, the first bit after the synchronization word is the first bit of the next 32-bit word, and so on.

Table 8: **Bitstream Header and Configuration Options**

Data Type	Data Field
Dummy word	FFFF FFFFh
Dummy word	FFFF FFFFh
Synchronization word	AA99 5566h
Packet Header: Write to CMD register	3000 8001h
Packet Data: RCRC	0000 0007h
Packet Header: Write to FLR register	3001 6001h
Packet Data: Frame Length	0000 00--h
Packet Header: Write to COR	3001 2001h
Packet Data: Configuration options	---- ----h
Packet Header: Write to MASK	3000 C001h
Packet Data: CTL mask	0000 0000h
Packet Header: Write to CMD register	3000 8001h
Packet Data: SWITCH	0000 0009h
Packet Header: Write to CMD register	3000 8001h
Packet Data: WCFG	0000 0001h

After synchronization, all data (register writes and frame data) are encapsulated in *packets.* There are two kinds of packets: Type 1 and Type 2. Type 1 packets are used for register writes. A combination of Type 1 and Type 2 packets are used for frame data writes. A packet contains

two different sections: Header and Data. A Type 1 Packet Header, shown in Figure 10, is always a single 32-bit word that describes the packet type, whether it is a read/write function or a specific configuration register address (see Table 5) as the destination, and how many 32-bit words are in the following Packet Data portion. A Type 1 Packet Data portion may contain anywhere from 0 to 2,047 32-bit data words.

The first packet in Table 8 is a Type 1 packet header that specifies writing one data word to the CMD register. The following packet data is a data word specifying a reset of the CRC register (compare the data field of Table 8 to the binary codes of Table 6).

The second packet in Table 8 loads the frame size into the FLR. The value is the frame size from Table 4, divided by 32, minus 1, and converted to Hex (e.g., the FLR for a V300 is 14h).

The third packet loads the configuration options into the COR register. The binary description of this register is not documented. Following this is a similar write of the SWITCH command to the CMD register which selects the CCLK frequency specified in the COR. Finally, the WCFG command is loaded into the CMD register so the loading of frame data may commence.

Table 9 shows the packets that load all the data frames starting with a Type 1 packet to load the starting frame address, which is always 0h.

Packet Header	Type	Operation (Write/Read)	Register Address (Destination)	Byte Address	Word Count (32-bit Words)
Bits[31:0]	31:29	28:27	26:13	12:11	10:0
Type 1	001	10/01	XXXXXXXXXXXXX	XX	XXXXXXXXXX

Figure 10: **Type 1 Packet Header**

Packet Header	Type	Operation (Write/Read)	Word Count (32-bit Words)
Bits[31:0]	31:29	28:27	26:0
Type 2	010	10/01	XXXXXXXXXXXXXXXXXXXXXXXXXX

Figure 11: **Type 2 Packet Header**

Table 9: **Bitstream Data Frames and CRC**

Data Type	Data Field
Packet Header: Write to FAR register	3000 2001h
Packet Data: Starting frame address	0000 0000h
Packet Header: Write to FDRI	3000 4000h
Packet Header Type 2: Data words	5--- ----h
Packet Data: Configuration data frames in 32-bit words. Total number of words specified in Type 2 Packet Header	---- ----h ....
Packet Header: Write to FAR register	3000 2001h
Packet Data: Next frame address	---- ----h
Packet Header: Write to FDRI	3000 4---h
Packet Data: Configuration data frames in 32-bit words. Total number of words specified in Packet Header	---- ----h ....
Packet Header: Write to FAR register	3000 2001h
Packet Data: Next frame address	---- ----h
Packet Header: Write to FDRI	3000 4---h
Packet Data: Configuration data frames in 32-bit words. Total number of words specified in packet header	---- ----h ....

Table 9: **Bitstream Data Frames and CRC *(Continued)***

Data Type	Data Field
Packet Header: Write to CRC	3000 0001h
Packet Data: CRC value	---- ----h
Packet Header: Write to CMD register	3000 8001h
Packet Data: LFRM	0000 0003h
Packet Header: Write to FDRI	3000 4---h
Packet Data: Configuration Data Frames in 32-bit words. Total number of words specified in packet header	---- ----h ....

The loading of data frames requires a combination of Type 1 and Type 2 packets. Type 2 packets must always be preceded by a Type 1 packet that contains no packet data. A Type 2 packet also contains both a header and a data portion, but the Type 2 packet data can be up to 1,048,575 data words in size.

The Type 2 packet header, shown in Figure 11, differs slightly from a Type 1 packet header in that there is no Register Address or Byte Address fields.

To write a set of data frames to the configuration memory, after the starting frame address has been loaded into the FAR, a Type 1 packet header issues a write command to the FDRI, followed by a Type 2 packet header specifying the number of data words to be loaded, and then followed by the actual frame data as Type 2 packet data. Writing data frames may require a Type 1/Type 2 packet combination, or a Type 1 only. This depends on the amount of data being written.

This series of FAR and FDRI writes is executed three times to load all but the last data frame. Before the last data frame is loaded, a CRC check is made. To load the last frame, a LFRM command is written to the CMD register followed by a Type 1/Type 2 packet combination to the FDRI, just as before, except that there is no FAR specified. The FAR is not needed when writing the last data frame.

Table 10 shows the packets needed to issue the start-up operations and load the final CRC check. The FPGA does not go active until after the final CRC is loaded. The number of clock cycles required to complete the start-up depends on the BitGen options. Completion of the configuration process requires eight to 16 clock cycles after the final CRC is loaded. Typically, DONE is released within the first seven CCLK cycles after the final CRC value is loaded but, the rest of the dummy data at the end of the stream should continue to be loaded. The FPGA needs the additional clock cycles to finish internal processing, but this is not a concern when a free-running oscillator is used for CCLK. In serial mode this requires only 16 bits (two bytes), but in SelectMAP mode, this requires 16 bytes of dummy words at the end of the bitstream. Since the intended configuration mode to be used is unknown by Bitgen, four 32-bit dummy words (16 bytes) are always placed at the end of the bitstream.

Table 10: **Bitstream Final CRC and Start-up**

Data Type	Data Field
Packet Header: Write to CMD register	3000 8001h
Packet Data: START	0000 0005h
Packet Header: Write to CTL	3000 A001h
Packet Data: Control commands	0000 0000h
Packet Header: Write to CRC	3000 0001h
Packet Data: CRC value	---- ----h
Dummy word	0000 0000h
Dummy word	0000 0000h
Dummy word	0000 0000h
Dummy word	0000 0000h

Cyclic Redundancy Checking Algorithm

Virtex configuration utilizes a standard 16-bit CRC checksum algorithm to verify bitstream integrity during configuration. The 16-bit CRC polynomial is shown below.

$$CRC\text{-}16 = X^{16} + X^{15} + X^{2} + 1$$

The algorithm is implemented by shifting the data stream into a 16-bit shift register, shown in Figure 12. Register Bit(0) receives an XOR of the incoming data and the output of Bit(15). Bit(2) receives an XOR of the input to Bit(0) and the output of Bit(1). Bit(15) receives an XOR of the input to Bit(0) and the output of Bit(14).

A CRC Reset resets all the CRC registers to zero. As data is shifted into the CRC circuitry, a CRC calculation accumulates in the registers. When the CRC value is loaded into the CRC calculation register, the ending CRC checksum is loaded into the CRC Register. The value loaded into the CRC Register should be zero; otherwise, the configuration failed CRC check.

Not all of the configuration stream is loaded into the CRC circuitry. Only data that is written to one of the registers shown in Table 11 is included. For each 32-bit word that is written to one of the registers (Table 11), the address code for the register and the 32-bit data word is shifted LSB first into the CRC calculation circuitry, see Figure 12. When multiple 32-bit words are written to the same register, the same address is loaded after each word. All other data in the configuration stream is ignored and does not affect the CRC checksum.

Table 11: **CRC Registers**

Symbol	Register Name	Address
CMD	Command	0100b
FLR	Frame Length	1011b
COR	Configuration Option	1001b
MASK	Control Mask	0110b
CTL	Control	0101b
FAR	Frame Address	0001b
FDRI	Frame Data Input	0010b
CRC	Cyclic Redundancy Check	0000b

This description is a model that may be used to generate an identical CRC value. The actual circuitry in the device is a slightly more complex Parallel CRC circuit that produces the same result.

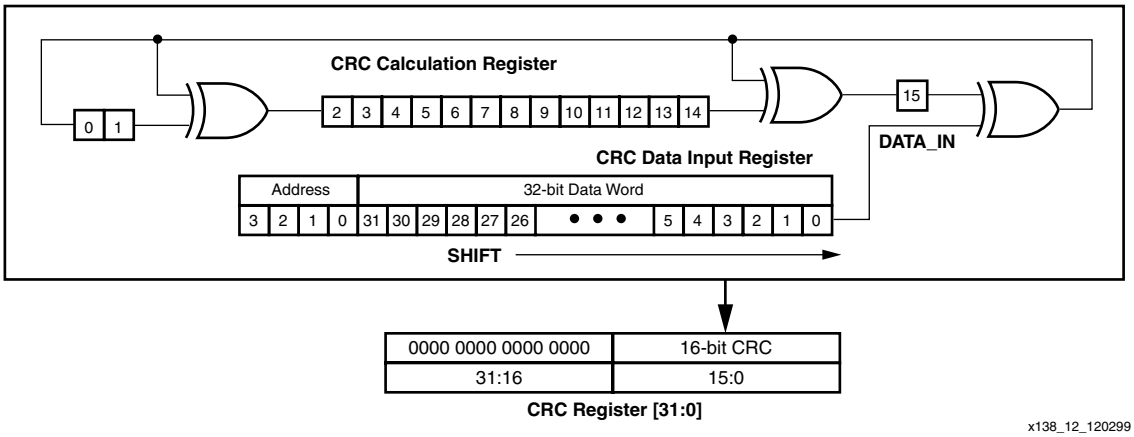


Figure 12: **Serial 16-bit CRC Circuitry**

Readback

Readback is the process of reading all the data in the internal configuration memory. This can be used to verify that the current configuration data is correct and to read the current state of all internal CLB and IOB registers as well as the current LUT RAM and block RAM values.

Readback is only available through the SelectMAP and Boundary Scan interfaces. This application note only demonstrates the use of the SelectMAP interface for performing readback. For information on using the Boundary Scan interface for readback refer to application note XAPP139 “Configuration and Readback of Virtex FPGAs Using (JTAG) Boundary Scan”.

Readback Verification and Capture

Readback verification is used to verify the validity of the stored configuration data. This is most commonly used in space-based applications where exposure to radiation may alter the data stored in the configuration memory cells.

Readback capture is used to list the states of all the internal flip-flops. This can be used for hardware debugging and functional verification. When Capture is initiated, the internal register states are loaded into unused spaces in the configuration memory which may be extracted after a readback of the configuration memory.

While both *Verify* and *Capture* can be performed in one readback, each require slightly different preparation and post processing.

Preparing for Readback in Design Entry

If only a readback verification is to be performed, there are no additional steps at the time of design entry. However, if readback capture is to be used, the Virtex library primitive CAPTURE_VIRTEX must be instantiated in the user design as shown in Figure 13.

The CAPTURE_VIRTEX component is used in the FPGA design to control when the logic states of all the registers are captured into configuration memory. The CLK pin may be driven by any clock source that would synchronize Capture to the changing logic states of the registers. The CAP pin is an enable control. When CAP is asserted, the register states are captured in memory on the CLK rising edge.

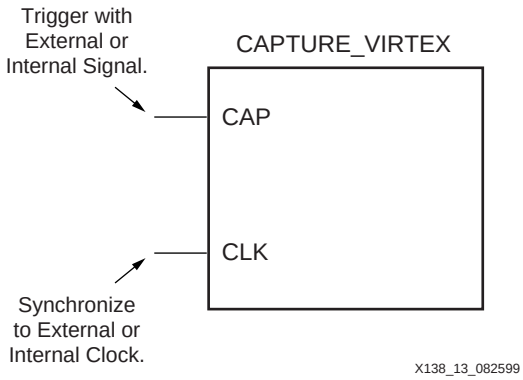


Figure 13: **Readback Capture Library Primitive**

Enabling Readback in the Software

Since readback is performed through the SelectMAP interface after configuration, the configuration ports must continue to be active by setting the persistence switch in BitGen. Additionally, a readback bit file, which contains the commands to execute a readback and a bitmap for data verification, may be optionally generated by setting the readback option in BitGen. An example of the BitGen command line is shown below:

```
bitgen -w -l -m -g readback -g persist:X8 ...
```

The **-w** overwrites existing output. The **-l** generates a *Logic Allocation* file, which is discussed in "Capturing Register States" on page 79. The **-m** generates a *Mask* file, which is discussed in "Verifying Configuration Data" on page 75. The **-g readback** generates the *readback bit* file, which is discussed in "Readback Operations" on page 72, and the **-g persist:X8** keeps the SelectMAP interface active after configuration. A listing of all the associated BitGen files used for readback is shown in Table 12.

For more information about BitGen options see "BitGen Switches and Options" on page 49.

Table 12: **BitGen files used in Readback**

File Name	File Type	File Extension	File Description
Readback B	Binary	.rbb	Binary command set and verification bitmap.
Readback A	ASCII	.rba	ASCII command set and verification bitmap.
Mask	Binary	.msk	Binary command set and verification data mask.
Logic Allocation	ASCII	.ll	ASCII bit number and location of captured signal names.

Readback Operations

Readback is performed by reading a data packet from the FDRO register. The flow for this process is shown in Figure 14.

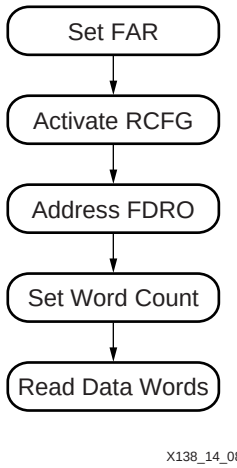


Figure 14: **CLB Readback Operation Flow**

The entire configuration memory map cannot be read in one readback sequence. Three sequences are required: one for the CLB frames and two for the block RAM frames. However, all of the configuration data frames that need to be read for verification, as well as all of the register states stored by Capture, are contained within the CLB frames. The other frame sections contain the configuration data for the columns of block RAMs. The block RAM configuration data need not be used for verification purposes, but may be used to extract the current internal states of the block RAMs just as Capture is used to extract the current internal states of registers. Therefore, a full readback and capture would require three separate readback sequences, but a simple verification requires onlyone (the CLB frames). This section describes the process for readback of the CLB Frames. For readback of the block RAM frames, first review this section and then refer to "Readback of Block RAM Frames" on page 81.

Table 13 shows the command set to initiate a readback of the CLB Frames. This command set is provided in the `<design>.rbb` file shown in Figure 19, `<design>.rba` and the `<design>.msk` file shown in Figure 17 on page 76.

To perform the first readback sequence after configuration, it is not necessary to re-synchronize the SelectMAP interface. However, if re-synchronization is required, an ABORT process should be executed followed by loading the synchronization word. See Table 13. If a re-synchronization is not necessary, the synchronization word may be omitted from the readback command set. If the synchronization word is reloaded, it is merely interpreted as a “No Operation” command and is ignored. The total readback command set, not including the synchronization word, is 24 bytes.

Table 13: **Readback Command Set for CLB Frames**

Data Type	Data Field
Synchronization word	AA99 5566h
Packet Header: Write to FAR register	3000 2001h
Packet Data: Starting frame address	0000 0000h
Packet Header: Write to CMD register	3000 8001h
Packet Data: RCFG	0000 0004h
Packet Header: Read from FDRO	2800 6000h
Packet Header Type 2: Data words	48-- ----h

Since all data loaded through the SelectMAP interface is processed as 32-bit words, re-synchronization is needed when either an unknown number (or a number that is not a multiple of four bytes) of data write cycles have taken place since the last command was loaded.

Once the configuration logic is synchronized, set the starting frame address in FAR as shown in Table 13. For a complete readback of the CLB frames, this is always 32 x 0h. However, this value is different for the block RAM frames. See "Readback of Block RAM Frames" on page 81.

Next, load the RCFG command into the CMD register to set the FPGA for readback. Address the FDRO register with a Type *1 read packet data header* that specifies "0" following data words. Follow that with a *Type 2 read data packet header* which specifies the number of 32-bit words to be readback. The number of data words to be readback depends on which Virtex device is being readback, shown in Table 14. Type 1 or Type 2 headers may be used depending on the amount of data that is to be readback. See "Bitstream Format" on page 61.

Table 14: **CLB Frame Word Counts per Device**

Device	TYPE 2 Packet Header for CLB Frames	CLB Frames Word Count
XCV50	4800 3E04h	15876
XCV50E	4800 408Ch	16524
XCV100	4800 581Ah	22554
XCV100E	4800 5B0Eh	23310
XCV150	4800 76B0h	30384
XCV200	4800 99C6h	39366
XCV200E	4800 9D92h	40338
XCV300	4800 CB07h	51975
XCV300E	4800 CF75h	53109
XCV400	4801 29F3h	76275
XCV400E	4801 2F39h	77625
XCV405E	4801 4997h	84375
XCV600	4801 A90Ah	108810
XCV600E	4801 B5B2h	112050
XCV800	4802 2E36h	142902
XCV812E	4802 6EC2h	159426
XCV1000	4802 D80Dh	186381
XCV1000E	4802 E881h	190593
XCV1600E	4803 9EAFh	237231
XCV2000E	4804 7670h	292464
XCV2600E	4805 BB7Eh	375678
XCV3200E	4807 4799h	477081

Now the readback data is ready to be clocked out. The readback sequence is shown in waveform format in Figure 15. First, assert the $\overline{CS}$ and $\overline{WRITE}$ signals and load the readback command set data described above, or from either the `<design>.rbb`, `.rba` or `.msk` file. See "Verifying Configuration Data" on page 75. for a detailed description of these files. Then, de-assert $\overline{WRITE}$ and $\overline{CS}$, and de-activate any external drivers on the D0 through D7 pins. To begin reading back the data, assert $\overline{CS}$ leaving $\overline{WRITE}$ High. The readback data bytes are driven out on each positive edge CCLK transition. Continue to clock for the entire readback

(Word Count x 4) bytes, and then de-assert $\overline{CS}$. The process may be repeated for additional readbacks.

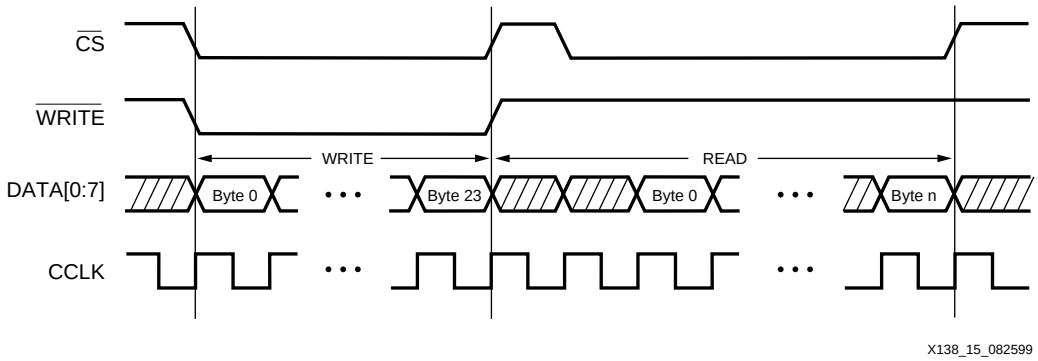


Figure 15: **Readback Clocking Sequence**

Readback Data Format

The readback data stream contains the information contained within the configuration memory map (data frames) plus additional pad data produced by the pipelining process of reading the data. The readback stream does not contain any of the commands, options, or packet information found in the configuration stream, nor does it contain any CRC values, since this information is stored in internal configuration registers, not the configuration memory. Additionally, no CRC calculation is performed during readback.

The readback stream consists of data frames each proceeded by one 32-bit word of pad data, shown in Figure 16. The first frame readback is pad data as well, and should be discarded along with the 32-bit word of pad data that proceeds it and every other frame. The size of each frame per device is shown in Table 15. The readback frame sizes are one 32-bit word smaller than the frame sizes listed for the configuration bitstream. This is because the configuration frame sizes account for the extra 32-bit pad word needed to push the configuration data through the FDRI pipeline.

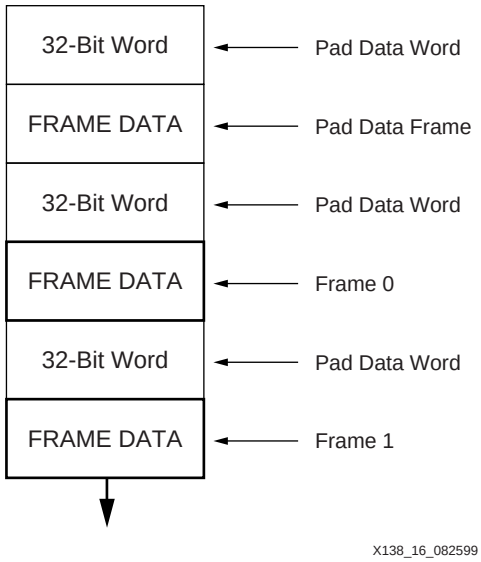


Figure 16: **Readback Data Stream**

Table 15: **Readback System Bytes for CLB Frames**

Device	CLB Frames	Bytes per Frame	Frame Bytes	Pad Bytes	Readback Bytes
XCV50	1322	44	58168	5336	63504
XCV50E	1376	44	60544	5556	66100
XCV100	1610	52	83720	6496	90216
XCV100E	1664	52	86528	6716	93244
XCV150	1898	60	113880	7656	121536
XCV200	2186	68	148648	8816	157464
XCV200E	2240	68	152320	9036	161356
XCV300	2474	80	197920	9980	207900
XCV300E	2528	80	202240	10200	212440
XCV400	3050	96	292800	12300	305100
XCV400E	3104	96	297984	12520	310504
XCV405E	3374	96	323904	13600	337504
XCV600	3626	116	420616	14624	435240
XCV600E	3734	116	433144	15060	448204
XCV800	4202	132	554664	16944	571608
XCV812E	4688	132	618816	18892	637708
XCV1000	4778	152	726256	19268	745524
XCV1000E	4886	152	742672	19704	762376
XCV1600E	5516	168	926688	22240	948928
XCV2000E	6092	188	1145296	24564	1169860
XCV2600E	6956	212	1474672	28044	1502716
XCV3200E	7820	240	1876800	31528	1908328

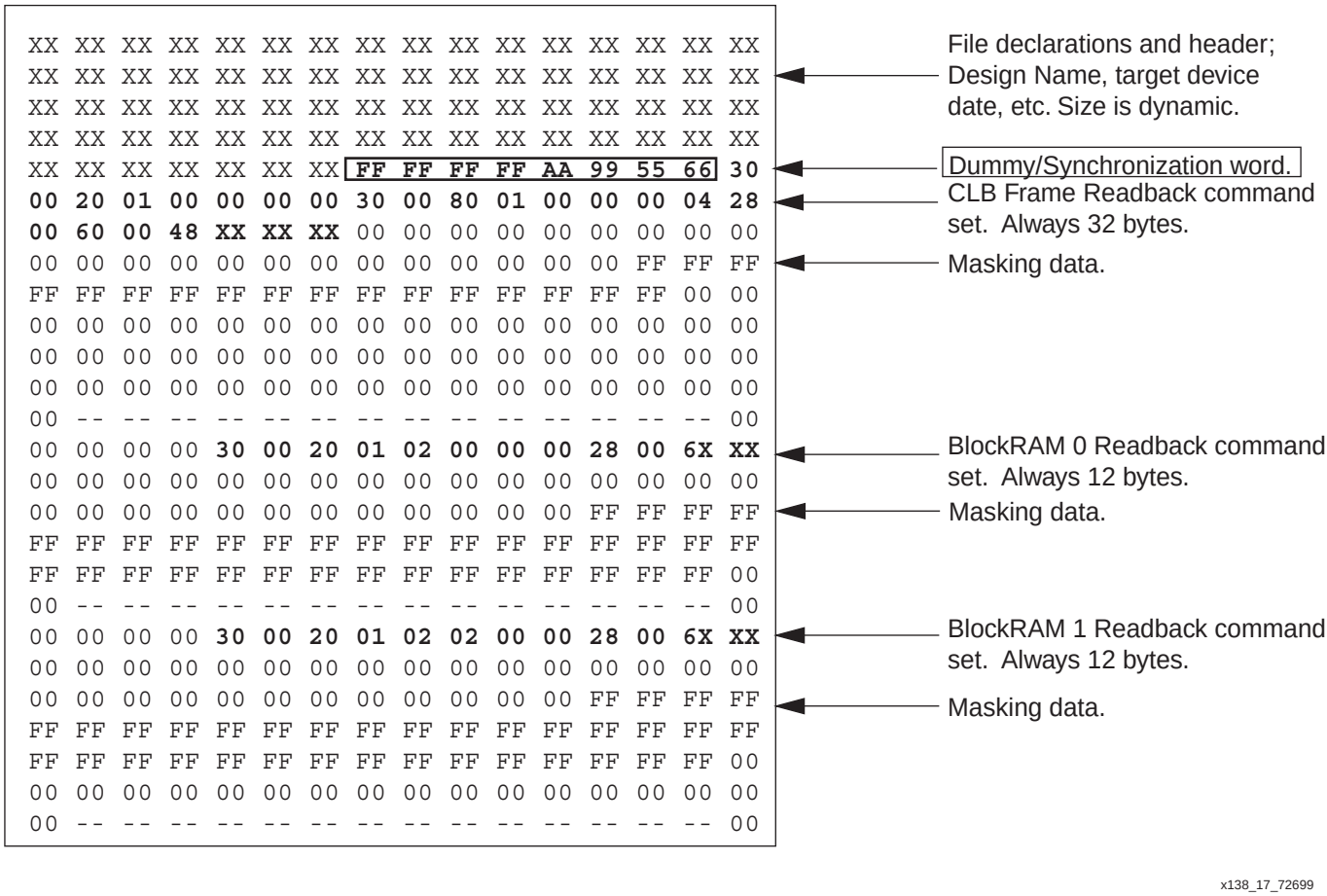
Verifying Configuration Data

Readback verification is a process of making a bit per bit comparison of the readback data frames to the bitmap in the `<design>.rbb` readback file. However, not all of the readback data should be used for verification. There are three types of data bits that cannot be verified against the bitmap: pad data, RAM bits, and Capture bits. The pad data is that described in the previous section, see Figure 17 and Table 15. RAM bits are configuration memory cells that hold the contents of LUT RAMs and block RAMs. These values are dynamically changing per the user design. The Capture bits are the memory locations reserved for capturing internal register states.

While the pad data words are separate data frames and must be ignored by any system performing readback, the RAM and Capture bits are sprinkled throughout the data frames and must be masked out. The `<design>.msk` mask file is used to mask out the RAM and Capture bits. An example of a mask file is shown in Figure 17.

The declarations portion is throw-away data. The first command set is for the CLB frames and includes the synchronization word which may be omitted if an Abort has not been executed. The second and third command sets are required for block RAM0 and block RAM1.

<design>.msk



x138_17_72699

Figure 17: **Readback Mask File for the Virtex Family**

The masking data is used to determine which of the data frame bits are configuration bits and should be verified against the bitmap in the `<design>.rbb` readback file, and which bits are either RAM or Capture bits and thus should be skipped. The MSK file will mask out the 32 bits following each frame, but does not mask out the first 32-bit portion of the readback stream, nor the first frame pad data or following 32-bit pipeline data portion. See Figure 18. The equation for this file follows.

$$RBB[i] = MSK[i] * DATA[i].$$

Each bit position of the masking data corresponds to the bit position of the readback data. Therefore, the first masking data bit specifies if the first bit of the first valid frame should be verified against the bitmap `<design>.rbb` file. If the mask bit is a "0b," the frame bit should be verified. If the mask bit is a "1b," the frame bit should not be verified. Since the mask file has the

32-bit pad data portions trailing the frames, at the end of each mask is a superfluous 32-bit portion which may be ignored.

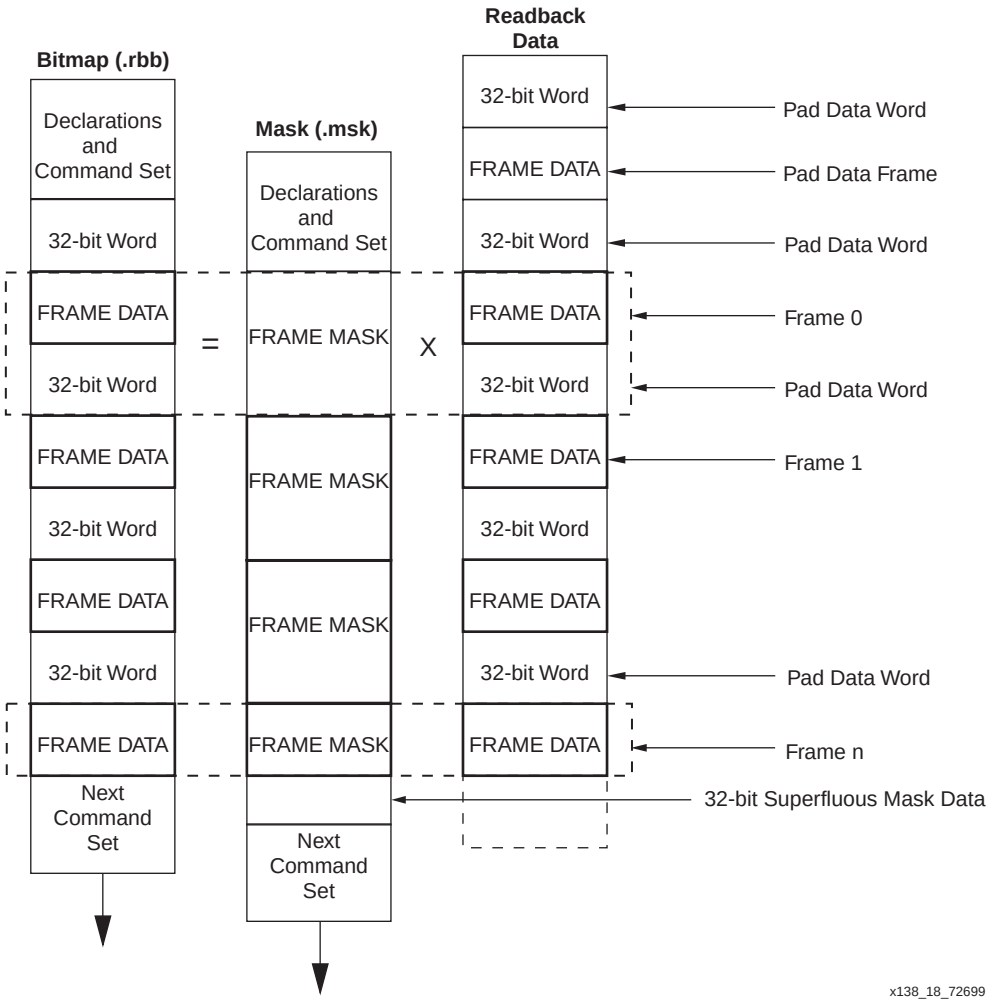


Figure 18: **Readback Data Stream Alignment**

The readback bit file `<design>.rbb` provides the configuration stream bitmap (data frames) for verifying the readback data stream. This must be used instead of the bitstream `<design>.bit` file, because, the frame data is encapsulated inside packets along with command data that is not written into configuration memory. The readback bit file is shown in Figure 19.

<design>.rbb

```
XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
XX XX XX XX XX XX XX FF FF FF FF AA 99 55 66 30
00 20 01 00 00 00 00 30 00 80 01 00 00 00 04 28
00 60 00 48 XX XX XX XX XX XX XX XX XX XX XX XX
XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
XX -- -- -- -- -- -- -- -- -- -- -- -- -- -- XX
XX XX XX XX 30 00 20 01 02 00 00 00 28 00 6X XX
XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
XX -- -- -- -- -- -- -- -- -- -- -- -- -- -- XX
XX XX XX XX 30 00 20 01 02 02 00 00 28 00 6X XX
XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
XX -- -- -- -- -- -- -- -- -- -- -- -- -- -- XX
```

File declarations and header; Design Name, target device date, etc. Size is dynamic.

Dummy/Synchronization word.

Readback command set. Always 32 bytes

Bitmap data.

BlockRAM 0 Readback command set. Always 12 bytes.

Bitmap data.

BlockRAM 1 Readback command set. Always 12 bytes.

Bitmap data.

x138_19_72699

Figure 19: **Readback Bit File for the Virtex Family**

Unlike the mask file, the bitmap does take into account that the pad data in between the data frames in the readback data stream proceed, rather than follow, each frame. The pad data portions in the readback data stream should not be verified against the bitmap. However, for every bit of pad data that is discarded from the readback data stream, a corresponding bit must be discarded from the bitmap data. A flow chart to demonstrate how a readback verification algorithm should work is provided in Figure 20.

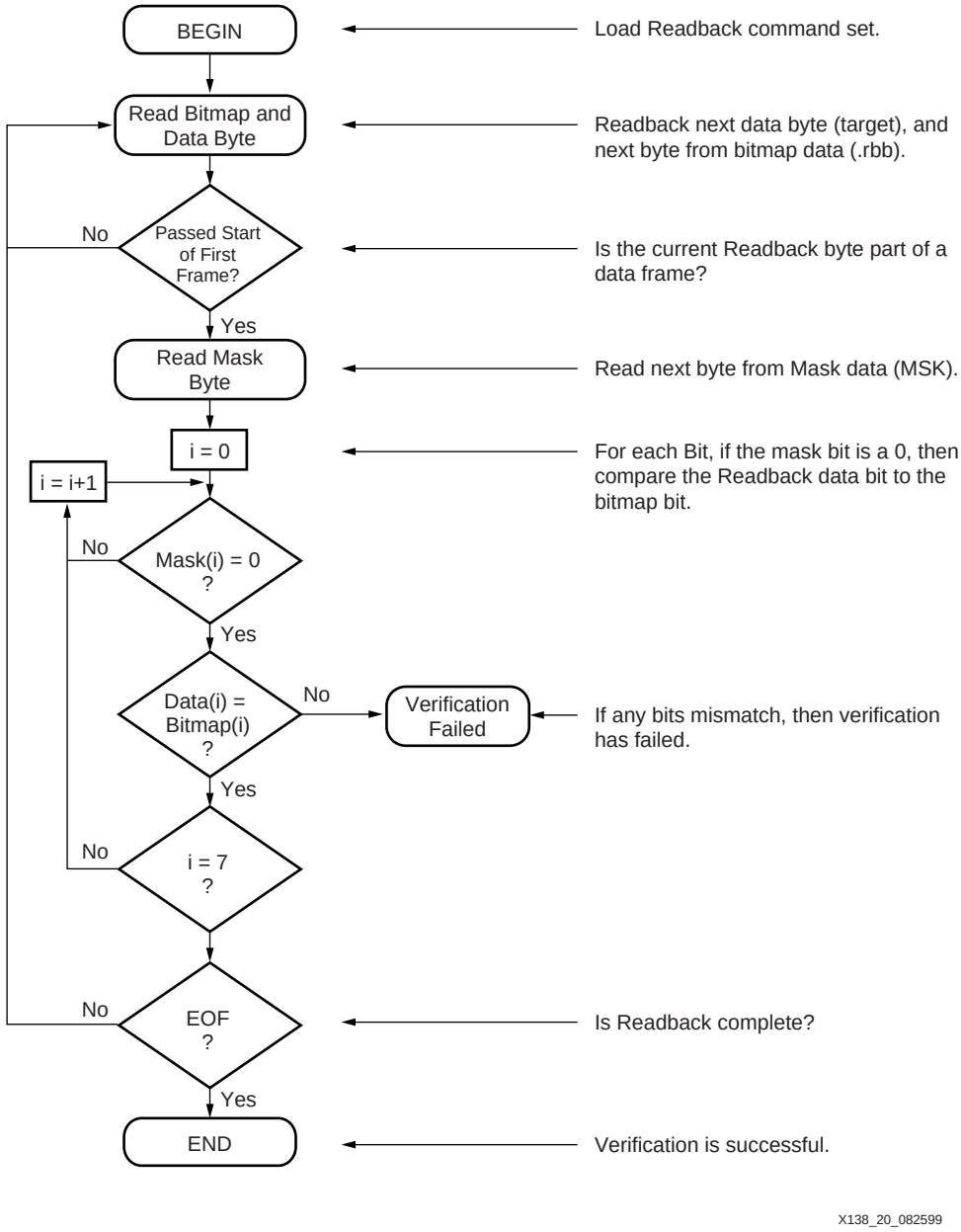


Figure 20: **Readback Verification Flow Diagram**

Capturing Register States

If Capture has been used to include the states of all internal registers in the readback data stream, the logic allocation `<design>.ll` file can be used to locate those signal state bits within the data frames. The logic allocation file includes all CLB and IOB outputs as well as all block RAM values, whether they are used in the design or not.

An example of portions of a Logic Allocation file is shown in the following text. Each Bit line includes a `<Bit offset> <Frame> <Frame offset> <CLB_location.Slice> <Type>` and a user net name if this node is used in the design.

```
;Revision 3
; Created by bitgen 2.1i at Fri. Mar 19 10:47:49 1999
; Bit lines have the following form:
; <offset> <frame number> <frame offset> <information>
;
```

```
Info Capture=Used
Info STARTSEL0=1
Info Persist=1
Bit      3274      11      35 Block=CLB_R16C13.S1 Latch=XQ
Bit      3292      11      53 Block=CLB_R15C13.S1 Latch=XQ
Bit      3310      11      71 Block=CLB_R14C13.S1 Latch=XQ
Bit      3328      11      89 Block=CLB_R13C13.S1 Latch=XQ
Bit      3346      11     107 Block=CLB_R12C13.S1 Latch=XQ
Bit      3364      11     125 Block=CLB_R11C13.S1 Latch=XQ

Bit    409801    1265     266 Block=P9 Latch=PAD
Bit    409808    1265     273 Block=P7 Latch=PAD
Bit    409818    1265     283 Block=P6 Latch=PAD

Bit    360970    1115      35 Block=CLB_R16C1.S1 Latch=XQ Net=N$8

Bit    419598    1296      19 Block=RAMB4_R3C1 Ram=B:BIT47
Bit    419599    1296      20 Block=RAMB4_R3C1 Ram=B:BIT15
Bit    419600    1296      21 Block=RAMB4_R3C1 Ram=B:BIT14
```

The bit offsets describe the position of a junk bit in the configuration stream `<design>.bit`, and is not useful for this purpose. To calculate which bit in the readback stream correlates to a desired node or signal from the LL file, the frame-number, frame-offset, and frame-length must be used in the equation below.

Readback Bit Number = (FrameNumber x FrameLength) + Bitmap Length - FrameOffset + 32

The Frame Number and Frame Offset are given in the .11 file. The Frame Length is shown on Table 4 on page 61.

The readback bit number, calculated above, is relevant to the entire readback stream. That is, all readback data, including the pad frame and pad data words, should be counted to find the state bit represented by the readback bit number. Table 16 shows the different Bitmap Lengths for each Virtex device.

Table 16: **Bitmap Length by Virtex Device**

Device	Bitmap Length
XCV50	324
XCV50E	324
XCV100	396
XCV100E	396
XCV150	468
XCV200	540
XCV200E	540
XCV300	612
XCV300E	612
XCV400	756
XCV400E	756
XCV405E	756
XCV600	900
XCV600E	900
XCV800	1044
XCV812E	1044

Table 16: **Bitmap Length by Virtex Device *(Continued)***

Device	Bitmap Length
XCV1000	1188
XCV1000E	1188
XCV1600E	1332
XCV2000E	1476
XCV2600E	1692
XCV3200E	1908

The frame order for the block RAMs assumes that all the bits from a complete readback of all the CLB frames have been counted, and that the count continues on with the readback of the block RAM frames starting from the lowest block number. Therefore, when readback of block RAMs is used, the data frame bit count must be offset by the number of bits in all the CLB frames. This offset may be obtained from the Frame Bytes number in Table 15 and multiplying by eight.

Readback of Block RAM Frames

A readback of the block RAM frames may follow the same procedure as that for the CLB frames. However, when a readback of the block RAM is initiated, control of the block RAM is taken from the user logic so the block RAM elements may be accessed by the configuration circuitry. In order to make this hand off smooth and glitch free, it is recommended that a shutdown be performed prior to readback, and then a start-up again after readback. After a shutdown sequence has been performed, all user logic and I/O is disabled until a start-up sequence is performed. This is the same start-up sequence used in configuration. See "Start-up Sequence" on page 51. The start-up sequencer is used for both start-up and shut-down.

In applications where it is preferable not to shut-down the device, any user logic designed to drive the block RAM should also be designed to halt any write operations just prior to and during the block RAM readback session.

The flow for a block RAM readback is shown in Figure 21 with the shut-down and start-up sequences shown in the grey areas of Figure 21. RAM readback follows the same process as for CLB frames, but with a different FAR value. See "Readback Operations" on page 72. However, the synchronization step may be omitted if a previous readback sequence has already synchronized the SelectMAP interface.

The shut-down sequence is enabled by setting bit 15 of the COR. The preferred method of setting this value is to read the current value of COR, toggle bit 15 to a logic “1,” and then load the new 32-bit value back into the COR.

The full command set is shown in Table 18. After loading the COR, the START command, followed by the RCRC command must be written to the CMD register. For the Shut-down Sequence to commence, the device needs to be clocked eight times. This also flushes the data pipeline. Once the Shut-down Sequence is complete, it is safe to imitate the readback sequence of the block RAM.

To read back both columns of block RAMs, the readback sequence must be repeated for each column. The sequence is the same except for different FAR values as shown in Table 17.

Table 17: **Virtex Family Devices Starting Frame Address**

Frame Type	FAR
BlockRAM_0	0200 0000h
BlockRAM_1	0202 0000h

In Virtex-E and Virtex-EM devices the block RAM address alternates around the center to the right and left side starting with address "1" instead of the "0" in the Virtex family devices. The addressing is interweaved by starting with the block RAM to the right of the center at "1". The block to the left of the center is for address "2", and the block to the right of block "1" is "3". For a more detailed discussion, please refer to **XAPP151**.

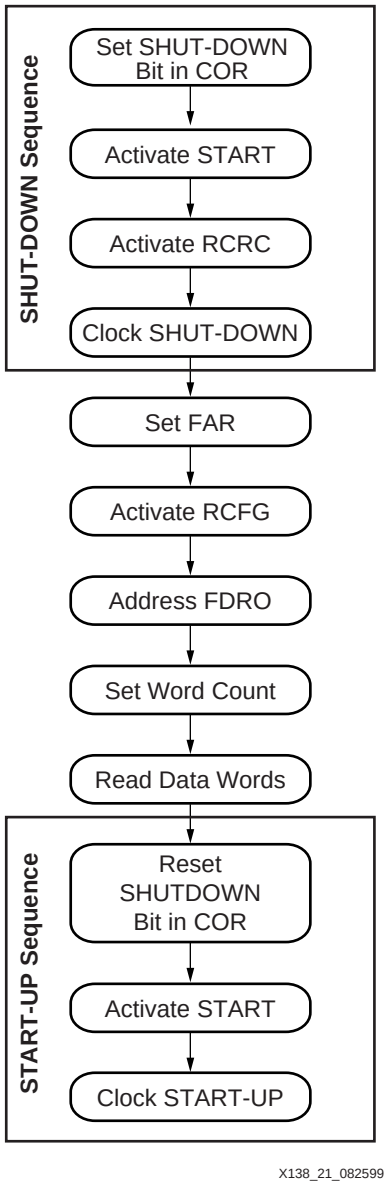


Figure 21: **Block RAM Readback Operation Flow**

Table 18: **Readback Command Set for Block RAM Frames**

Data Type	Data Field
Shut-down Sequence	
Packet Header: Read from COR	2801 2001h
Packet Data: Configuration options	---- ----h
Packet Header: Write to COR	3001 2001h
Packet Data: Set bit (15) to 1	---- ----h
Packet Header: Write to CMD register	3000 8001h
Packet Data: START	0000 0005h
Packet Header: Write to CMD register	3000 8001h
Packet Data: RCRC	0000 0007h
Dummy word	FFFF FFFFh
Dummy word	FFFF FFFFh
Block RAM Readback Sequence	
Packet Header: Write to FAR register	3000 2001h
Packet Data: Starting frame address	0200 0000h
Packet Header: Write to CMD register	3000 8001h
Packet Data: RCFG	0000 0004h
Packet Header: Read from FDRO	2800 6000h
Packet Header Type 2: Data words	48-- ----h
Start-up Sequence	
Packet Header: Write to COR	3001 2001h
Packet Data: Set bit (15) to 1.	---- ----h
Packet Header: Write to CMD register	3000 8001h
Packet Data: START	0000 0005h
Packet Header: Write to CMD register	3000 8001h
Packet Data: RCRC	0000 0007h
Dummy word	FFFF FFFFh
Dummy word	FFFF FFFFh

The two sets of block RAM frames in every device size consist of 65 frames in each column; however, the frame sizes vary per device. The word count for block RAM readback and the associated code for each device are shown in Table 19.

Table 19: **Word Counts per Frame Section**

Device	TYPE 2 Packet Header for Block RAM Frames	Block RAM Frames Word Count (each)
XCV50	4800 030Ch	780
XCV50E	4800 030Ch	780
XCV100	4800 038Eh	910
XCV100E	4800 038Eh	910
XCV150	4800 0410h	1040
XCV200	4800 0492h	1170
XCV200E	4800 0492h	1170
XCV300	4800 0555h	1365
XCV300E	4800 0555h	1365
XCV400	4800 0659h	1625
XCV400E	4800 0659h	1625
XCV405E	4800 0659h	1625
XCV600	4800 079Eh	1950
XCV600E	4800 079Eh	1950
XCV800	4800 08A2h	2210
XCV812E	4800 08A2h	2210
XCV1000	4800 09E7h	2535
XCV1000E	4800 09E7h	2535
XCV1600E	4800 0AEBh	2795
XCV2000E	4800 0C30h	3120
XCV2600E	4800 0DB6h	3510
XCV3200E	4800 0F7Dh	3965

After the completion of the readback session, a Start-up Sequence must be performed to reactivate the user logic and I/O. To enable the start-up, the shut-down bit (15) of the COR must be reset to a logic "0". Then, just as with the Shut-down Sequence, the START and RCRC commands must be loaded into the CMD register and the Sequence must be clocked eight times, at which time the device may resume normal operation.

Virtex-E Device Addendum

The configuration modes and operation of the 1.8V Virtex-E and Virtex-EM (Extended Memory) devices are similar with the 2.5V Virtex devices. The designer differences between the Virtex family and Virtex-E or Virtex-EM devices are discussed in this addendum.

Power Supplies

Virtex-E V_{CCINT}, the supply voltage for the internal logic and memory, is 1.8V instead of 2.5V for Virtex devices.

I/O Standards Supported

Virtex-E devices can be used with 20 high-performance interface standards, including LVDS and LVPECL differential signalling standards. A new LVCMOS I/O standard based on 1.8V V_{CCO} is also supported. I/O pins are 3.0V tolerant with appropriated external resistors. PCI 5.0V is not supported.

I/O Banking

In Virtex-E devices, the banking rules are different because the input buffers (with LVTTL, LVCMOS, and PCI standards) are powered by V_{CCO} instead of V_{CCINT}. For these standards, only input and output buffers that have the same V_{CCO} can be combined together in the same bank.

Configuration Bitstream Lengths

The total number of bits required to configure each Virtex-E device is different from Virtex devices. Table 20 shows the bitstream lengths.

Table 20: **Virtex-E Bitstream Lengths**

Device	# of Configuration Bits
XCV50E	630,048
XCV100E	863,840
XCV200E	1,442,016
XCV300E	1,875,648
XCV400E	2,693,440
XCV405E	3,430,400
XCV600E	3,961,632
XCV812E	6,519,648
XCV1000E	6,587,520
XCV1600E	8,308,992
XCV2000E	10,159,648
XCV2600E	TBD
XCV3200E	TBD

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
3/21/99	1.0	Initial release
7/29/99	1.1	Overall update to application note
9/23/99	1.2	Virtex-E update
2/24/00	2.0	Revised to new template, new drawings
6/15/00	2.1	Virtex-EM update to tables 4, 7, 8, 10, 14,15,18, and 19. Revised Figures 1 and 3.

XAPP181 (v1.0) March 15, 2000

SEU Mitigation Design Techniques for the XQR4000XL

Author: Phil Brinkley, Avnet and Carl Carmichael

Summary

This Application Note discusses system and FPGA design techniques for applications that operate in space or in other environments exposed to heavy ion or charged particle radiation. Single Event Upset (SEU) detection, correction, and mitigation for the XQR4000XL are demonstrated.

Overview

FPGA design for use in a radiation environment presents new challenges to the traditional digital designer. Often people associate radiation tolerance with the so-called "hardness" of the part. "Hardness" is simply a measure of the total dose of radiation to which an IC can be subjected before critical parameter(s) cross a predefined threshold. An IC is therefore said to be "rad tolerant" to a given total dosage, at which point some critical parameter goes out of specification.

Supply Current (I_{CC}) and Radiation Dosage

For many technologies, the supply current of a device (I_{CC}) is a critical parameter for determining useful life for a device when subjected to ionizing radiation. In some technologies, the gate control voltage at the onset of conduction (the threshold voltage) decreases (or increases) when subjected to radiation. If this threshold voltage gets too low, the integrated circuit can experience an increase on I_{CC} caused by leakage across an "off" transistor. Another cause of an increase in I_{CC} with ionizing radiation is a decrease in the field threshold (the field oxide parasitic transistor in parallel with every active transistor). If the field threshold decreases, the integrated circuit can also experience an increase in I_{CC}. While both of these phenomena limit the useful radiation exposure a device can withstand, they present different aspects to the circuit designer.

A decrease in the threshold voltage will also manifest itself in an increase in the frequency capability of the integrated circuit and an increase in I_{CC}, while a decrease in the field voltage will result only in an increase of I_{CC}. It is this latter effect that has dominates the useful ionizing radiation performance of the XQR4000XL. A plot of I_{CC} versus total dose for the XQR4000XL is shown in Figure 1.

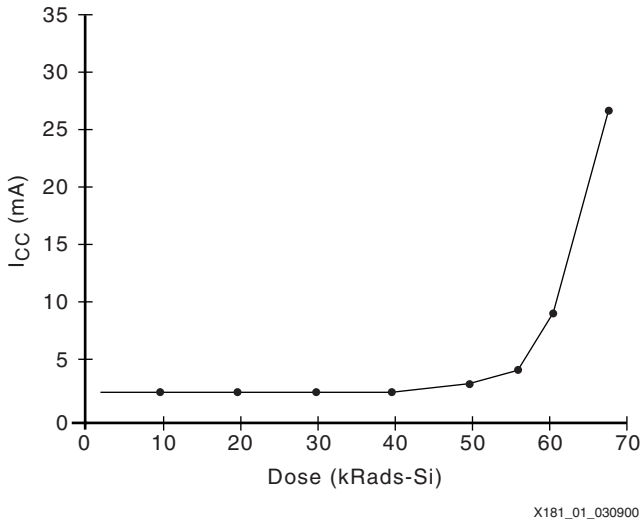


Figure 1: **I_{CC} (mA) vs. Total Dose (KRads)**

Xilinx defines the dose limit of their XCR4000XL FPGAs as the point where I_{CC} has increased to twice the commercial I_{CC} specification, with all AC parameters remaining within specification. The commercial I_{CC} specification is a very conservative value, so twice this number still falls within absolute operating limits. The 0.35µ XC4000XL radiation-tolerant FPGAs are rated as 60 KRad parts.

If the application requires a higher total dosage rating than that specified, shielding may be employed to keep the effective dosage of the FPGA below the maximum specification.

Single-Event Upset (SEU) Logic Errors

In addition to the Total Dose, Single Event Effects (SEE) must be considered. As an IC is bombarded with radiation particles, a temporary logic state change can occur within the IC. This phenomenon is known as a Single Event Upset (SEU). This effect can manifest as a *transient upset* which can last a few nanoseconds, or as a *static upset* which changes the stored charge of a static cell. For simple gates, a transient glitch in the logic is usually not an issue. When an SEU occurs within the latch that makes up a flip-flop or memory cell, however — a *static upset* — the effects on functionality are often problematical. Since a flip-flop is a memory device, the flip-flop can change state and remain in that state until the next occurring clock or reset. In this condition the flip-flop is said to have been "upset" (i.e., its state has changed independently of circuit operation). Likewise, the configuration latches, which define the user's design functionality, can be also susceptible to static upsets.

Before methods to mitigate the risks and effects of an SEU are discussed, it is important to note that the functional effect(s) of an SEU are application specific. For example, if an FPGA is being used as a digital filter and an upset causes the filter to miscalculate, the result is "bad" data for a few clock cycles. This is typically a non-mission-critical function, and as long as the error can be detected and corrected, then it may be fully acceptable. However, a mission-critical function obviously cannot tolerate a functional upset. This application note will demonstrate ways to remove risk from functional upsets. Determining the risks and effects of an SEU in your system should be the first step in deciding upon an SEU mitigation approach.

A conventional design mitigation technique for standard logic is the "majority vote" circuit. The functionality of a single flip-flop is implemented by three flip-flops in parallel. These flip-flops

feed a gating circuit the output of which reflects the state of the majority of the flip-flops. A typical majority vote circuit is shown in Figure 2.

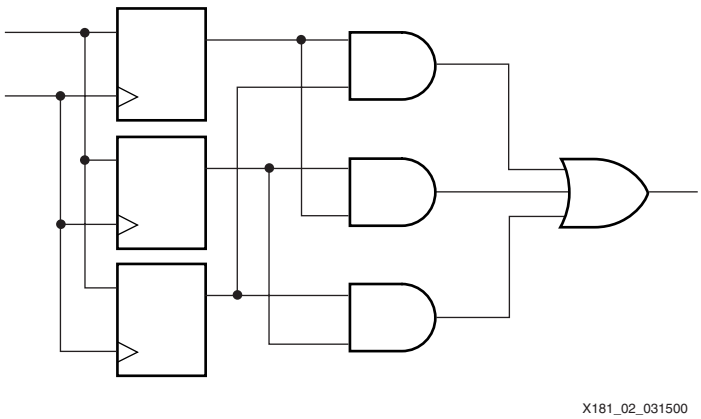


Figure 2: **Majority Vote Circuit**

Inherent in this technique is the assumption that only one SEU occurs within a given time period (i.e., the time it takes for the next clock edge to occur and load the flip-flops with new data). Obviously, if two of the flip-flops suffer contemporaneous upsets, then the majority vote circuit will give the state of the two incorrectly set flip-flops. The chance of this occurring, though, is usually considered statistically negligible, calculated by squaring the "normal" SEU rate (e.g., $[10^{-5}$ bit-upsets/day$]^2 = 10^{-10}$ uncorrected bit-upsets/day).

It is important to acknowledge that FPGA designs for space always come down to a determined acceptable amount of risk. Decreasing risk means increasing design complexity. The cost of the standard majority mitigation technique is obvious: the use of three times as many flip-flops. But with the abundance of resources available in Xilinx's line of rad-tolerant FPGAs, this cost would be tolerable in most cases.

However, there are many more latches in a Xilinx FPGA than those actually design-specified by the user as flip-flops; the majority of latches are in fact used for configuration memory. Because the configuration memory cells are just as susceptible to SEUs as are the design-specified flip-flops, the standard majority mitigation technique alone is not adequate to overcome the effects of SEUs in FPGAs.

Reconfigurability

One of the very notable features of Xilinx FPGAs is that they are reconfigurable, as opposed to *one-time programmable*. If a design change is necessary, then a new configuration can be loaded and the functionality of the FPGA altered without having to remove and discard the IC, as is the case with anti-fuse FPGAs. This also allows upgrades to be made in the field, or even in space. Unfortunately, this increased flexibility results in a more involved design solution for SEU effects. An understanding of how a Xilinx FPGAs configuration works is necessary before we can discuss the next level of SEU design mitigation techniques.

FPGA "First Floor and Basement" Architecture

Before power-up, a Xilinx FPGA is completely unconfigured. In other words, thousands of flip-flops and logic gates are residing in the IC, connected neither to one another nor to the I/O pins. As the power supply voltage rises and crosses a certain threshold, the FPGA begins to load its "brains" (configuration) and all I/O pins are set in a tri-state condition. The internal configuration clock becomes active and begins to clock data from the configuration data storage into the configuration latches. Buried in this configuration data stream are the items that make up a configured FPGA: logic function, I/O pin definition, clock distribution, flip-flops, routing, and so on. Once the configuration data is loaded and the CRC checksum is verified, the FPGA becomes active and the I/O pins begin to function as specified by the design.

Using a "house" analogy, if all the functions that the FPGA is to perform (logic, flip-flops, pins, etc.) are considered to be on the "first floor", then all the configuration latches are in the "basement". See Figure 3.

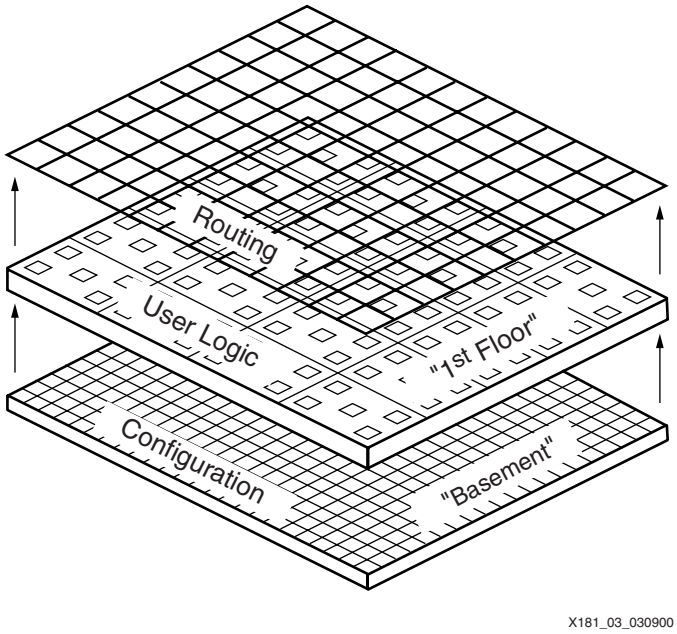


Figure 3: **FPGA Configuration Hierarchy**

As it turns out, the basement is necessarily much larger than the first floor. It takes approximately 30 configuration latches to configure each user-CLB, with each configuration latch controlling some specific property of the CLB or I/O block. The logic implemented in the look-up tables (LUTs) is one of the more important properties held in these latches. If a latch that configures an LUT experiences an upset, then the logic intended in the design may be altered. For example, it could be possible for a design-specified AND gate to become a NAND gate instead.

It should now become apparent that the majority vote circuit shown in Figure 2 is not reliable as an SEU mitigation technique, because the majority vote portion of the circuit can change its function in the event of an SEU occurring on a latch that controls the circuit. Therefore, some new methods of SEU mitigation are required.

Design Mitigation Techniques

FPGA designs are completed with varying degrees of risk based on the mitigation techniques employed. Since the amount of "acceptable risk" varies with the application, the design mitigation strategy employed will also vary. In some cases, it may be acceptable to do very little to accommodate SEUs; in other cases, the techniques may need to be rather sophisticated. The remainder of this Application Note will focus on various techniques for SEU mitigation. These techniques are listed in ascending complexity: auto-reconfiguration; using logic redundancy and an XOR gate for SEU detection; using the Xilinx "Readback" capability for SEU detection; using wired-AND outputs in conjunction with readback; and finally, building an SEU-safe system by combining these techniques.

Auto-Reconfiguration

The simplest approach to SEU mitigation is to reconfigure the FPGA upon detecting a system failure or at specified time intervals. For example, suppose an FPGA used to control a spacecraft heater experiences an SEU, causing the FPGA to improperly turn on the heater. If it can be determined through other spacecraft systems that the heater has been turned on, a command could be sent to restore the heater to its proper state and/or reconfigure the FPGA.

While this strategy may create an annoyance for the system, it might be seen as an acceptable approach in non-mission-critical applications where economy of design is paramount. If an application is of a more critical nature, however, then it may be imperative that the occurrence of an SEU be detected and specifically addressed.

XOR Gate for SEU Detection

One method for accomplishing this, shown in Figure 4, consists of adding a duplicate logic circuit to critical FPGA functions. One output drives whatever function the logic was designed to perform, while the output of the redundant circuit is used in conjunction with the primary output to drive the inputs of an XOR gate. If an SEU occurs which affects either circuit, the outputs of the logic will conflict and the XOR gate will output a "1" indicating that an SEU has occurred.

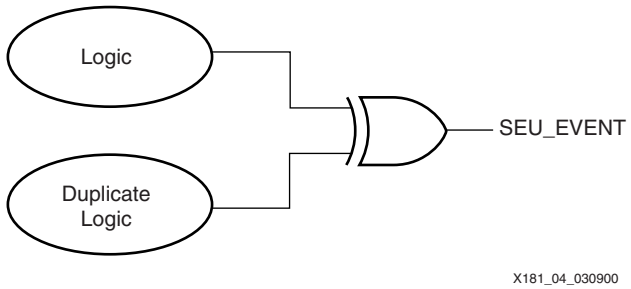


Figure 4: **SEU Detection by Redundancy and XOR Gating**

If there are several places where this method needs to be employed, the XOR outputs can all be ORed together to provide a single SEU status bit. This SEU status bit can also be used to drive the GTS (Global Tri-State) pin of the STARTUP component, causing all outputs to a high-impedance state in the event of an SEU occurrence.

Xilinx "Readback" Capability

Every Xilinx FPGA family incorporates a feature called Readback. Originally designed to facilitate testing during production of the ICs, it provides a non-intrusive method of reading the current state of every flip-flop and configuration memory cell within the FPGA. To make use of this feature, the "Readback" component needs to be instantiated in the design.

This function runs in the background, and in no way affects the performance of the FPGA. The design can run at full speed while simultaneously performing a readback. (See Xilinx Application Note XAPP015 "Using the XC4000 Readback Capability").

A CRC checksum based upon all the bits that have just been read back is generated and inserted at the end of the readback serial stream. This CRC checksum can be compared to the expected checksum for the current configuration; if it does not compare, then an SEU may have occurred.

During Readback, every bit that currently resides in each flip-flop along with every configuration bit is serially shifted out of the readback block. The output of the readback block can drive either an external pin or an internal signal. Readback of the XQR4000XL must be clocked out at a frequency between 1 MHz and 2 MHz. (Virtex™ is two orders of magnitude faster). The amount of time required to read back the FPGA varies on the size of the FPGA. For example, the XC4062XL contains 1,433,812 configuration bits. At a 1.5 MHz rate, it would take 960 ms to read back this FPGA.

There are three different ways to incorporate readback in a design. These are:

- Use a microcontroller or microprocessor to verify the checksum
- Use separate FPGAs to monitor one another
- Self-readback

Each method will be discussed in detail below.

NOTE: If SelectRAM is to be used in the design, then a simple CRC check of the readback data will not work. This is because SelectRAM actually employs the configuration bits as storage elements. Therefore, if a RAM value has been changed, the configuration readback checksum will differ from the default value checksum. When incorporating SelectRAM in the design, therefore, readback should be used to perform a *full bit-for-bit verification* of the readback data (see Application Note XAPP015).

Microcontroller for Readback

The block diagram shown in Figure 5 illustrates a readback CRC compare function easily implemented using a microcontroller. The microcontroller simply extracts the checksum from the readback serial stream and then compares it to the expected value. The output of the circuit, SEU_EVENT, can be used to interrupt to the system's processor signaling the occurrence of an SEU. At the next "convenient" time, the FPGA should be commanded to reconfigure.

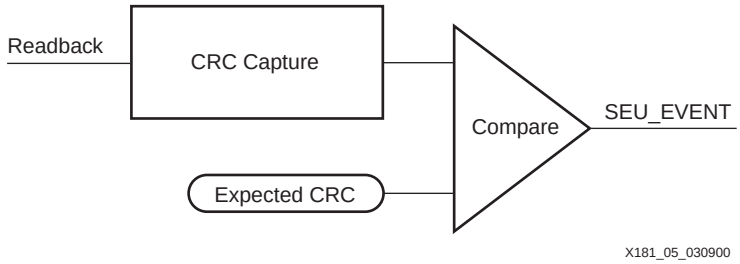


Figure 5: **Readback CRCComparator**

The CRC data is located in the last 11 bits of the readback stream. XAPP015 explains in greater detail the anatomy of the readback data; however, Table 1 summarizes the CRC locations for the XQR4000XL parts. The beginning of the readback stream is identified by a preamble consisting of five dummy "1s" followed by a "0". The amount of data between the preamble and the 11-bit CRC is device-dependent, as shown in Table 1.

Table 1: **Readback Datastream Size**

Device	Preamble	Data Stream	CRC (12 bits)
XQR4013XL	111110	<399,630 bits>	0<11 bits>
XQR4036XL	111110	<841,350 bits>	0<11 bits>
XQR4062XL	111110	<1,445,502 bits>	0<11 bits>

Using Separate FPGAs to Monitor One Another

If a design requires more than one FPGA, or multiple FPGAs are used as redundancy, then each FPGA can be used to monitor the readback serial stream of a neighboring FPGA. The CRC comparator shown in Figure 5 can easily be implemented in an FPGA. If an SEU is detected, one of two possibilities has occurred: Either the *FPGA* being monitored experienced an SEU, or the detection circuit in the monitoring FPGA itself experienced an SEU. The SEU_EVENT signal is used to alert the system that both FPGAs need to be reconfigured at the next opportunity.

Self-readback

Instead of having two or more FPGAs monitor one another's readback CRC, it is possible to use a single FPGA to monitor itself. Design redundancy is required, however, because an SEU can occur in the readback monitor circuit itself, thereby rendering its result invalid. A simple redundancy method involves creating two readback compare circuits in parallel and wire-ANDing the outputs. Simultaneous occurrence of CRC errors in both comparators would indicate an SEU in the configuration logic under test, rather than in one of the readback compare circuits. A block diagram of this technique is shown in Figure 6.

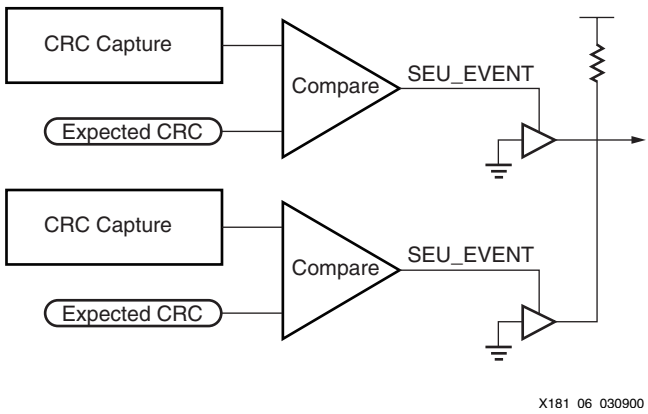


Figure 6: **Redundant CRC Comparator**

Wire-ANDed Outputs

Up to this point, we have focused on methods of detecting when a logic error caused by an SEU has already occurred. Some signals, however, are sufficiently mission-critical that an erroneous logic state on an output cannot be tolerated for any period of time. The technique of wire-ANDing redundant logic outputs can be employed to mitigate the effects of SEUs at this level of criticalness.

For example, suppose that the FPGA is being used to drive a pyrotechnic device that jettisons part of a spacecraft. In this example, it would be unacceptable for the signal output to remain erroneous for the time required to complete a readback, detect that an SEU has occurred, and remediate the condition. Wire ANDing using redundant design logic only drives a mission-critical output to the active state when the two legs of redundant logic agree.

It is important to understand that this mitigation method does not ensure that a desired signal will be correctly asserted in spite of an SEU which occurs during the assertion function. It does, however, ensure that a signal will not be erroneously asserted due to an SEU.

The technique is shown in Figure 7.

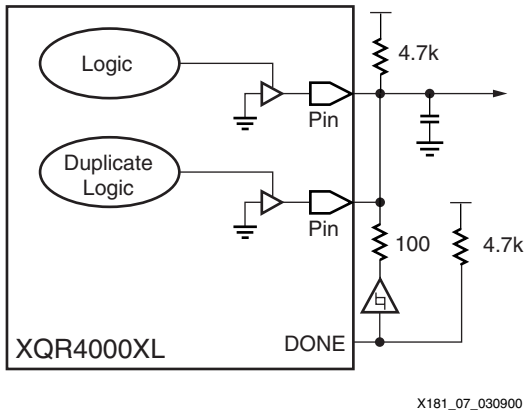


Figure 7: **Wire-ANDing Critical Outputs**

To drive an output High, both the primary and duplicate logic chains must direct their respective output buffers to a high-impedance condition. In this state, both logic outputs are high-impedance (looking back into the output pins), and the external pull-up resistor will pull the output signal High. If the logic chains do not agree, however, one or the other of the output buffers will be enabled, driving the wire-ANDed buffer output signal Low.

This technique is reliable for especially critical control signals, where one output state (logic High) is, by design, more meaningful than the other (logic Low). However, this approach is inappropriate for general data processing applications, where the output logic states are of equal importance and correct data propagation must be ensured.

Using the DONE signal to Control I/O Pins During Configuration

A precaution must be taken to ensure that the output of an unconfigured part is not interpreted as a true logic High. Since the FPGAs I/Os are in a high-impedance state before and during configuration, some other signal must hold the outputs Low during this time. The FPGAs DONE signal can be conveniently used to do this, since it drives Low during configuration. Since DONE will need to transition to High after configuration, an open-drain buffer should be placed between it and the outputs to be protected. (If many outputs are to be controlled in this fashion, additional buffers or relays may be added for each output pair.)

WARNING: *It is imperative that the bit-stream generation (BitGen) software start-up options specify that the I/Os are released before the DONE. Note that this is NOT the default!*

Reliable System Design

To be considered reliable, a system must process and propagate data correctly even in the event of an upset to the configuration and/or user logic. To build a reliable FPGA system, therefore, we must combine the techniques of SEU detection, correction and mitigation.

Whichever method of SEU detection is chosen (full verification or CRC checking), adequate SEU correction requires reconfiguring the FPGA, as the configuration logic and memory cannot be ruled out as being a possible cause of the error detected. The XQR4000XL, therefore, does constrain the designer in one significant respect: a temporary disruption in

service must be tolerated when correcting detected upsets. Designers of systems that cannot tolerate such a disruption should consider using the Virtex FPGA, which can be partially reconfigured without interruption.

Therefore, while an upset is present and being addressed, the logical functionality of the user design must be validated in some way so that incorrect data is not propagated through the system. The classical method for accomplishing this is Triple-Module Redundancy (TMR): that is, three identical FPGAs processing the same data in tandem, with the outputs mediated by an external voting circuit (Figure 2 on page 89).

TMR carries the further advantage that the entire FPGA may be used for the basic design, with no internal SEU mitigation techniques applied. However, since three duplicate FPGAs are required, it also carries the disadvantage of consuming significantly more board space and power. Where full TMR is deemed unsuitable by design economics or other considerations, the number of redundant FPGAs can be reduced from three to two by combining variations of the previously discussed techniques, provided the basic design (including duplicated logic) can be implemented within one FPGA.

Dual-voting Device Redundancy

A dual-voting system incorporates in just two FPGAs a fully redundant, self-mitigating system with built-in SEU detection and correction. The system, shown in Figure 8, is comprised of two FPGAs and a storage PROM.

The basic logic design is duplicated in each FPGA. The two FPGAs configure sequentially and then resynchronize. Corresponding output pairs are XORed, and then all XOR outputs are ORed together to drive the (GTS) pin of the STARTUP component.

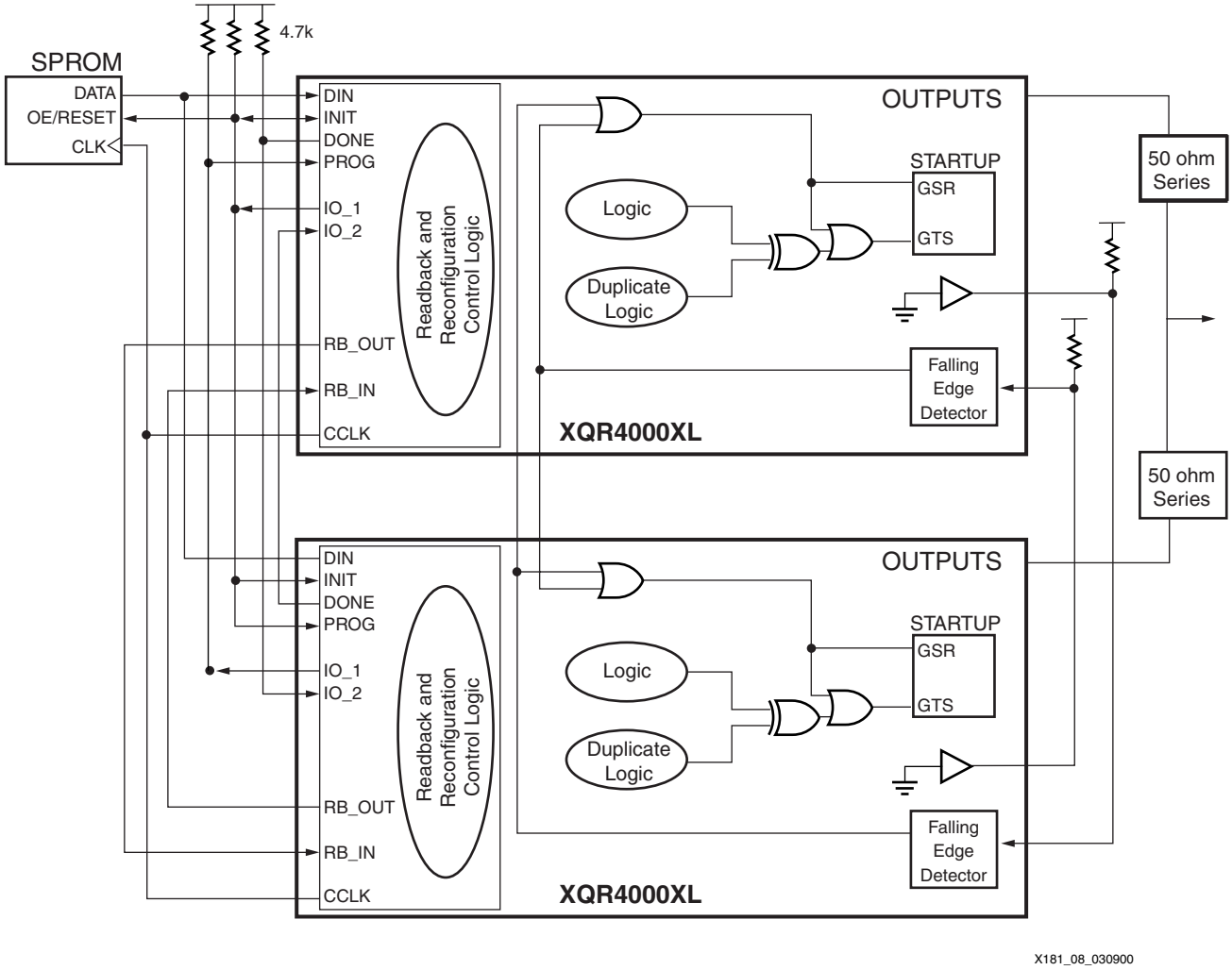


Figure 8: **Dual Redundant Self-mitigating FPGA Design**

If the occurrence of an SEU affects the function of the user logic, the compare circuitry will assert the GTS signal for that device. Asserting GTS causes all the I/O pins of the affected FPGA to a high-impedance state; however, the unaffected FPGA will continue to drive the correct data. If the SEU is merely transient (i.e., no configuration cells are upset), GTS will release when the redundant logic modules are resynchronized. (For complex designs an additional security measure may be added to time-out when one device has been off-line too long and issue a soft reset to both FPGAs to resynchronize the system).

To protect against the effects of an SEU occurring within the configuration memory cells, each FPGA should perform a constant readback on the other. When one FPGA detects that the other has been upset, it will force the upset FPGA to reconfigure. When the upset FPGA is reinitialized and resumes operation, it should notice that the other FPGA is already running, and should assert a soft reset (GSR) to both FPGAs to resynchronize the system. (The soft reset causes an unfortunate disruption of the system, but the interruption is less severe than it would be with less sophisticated SEU mitigation, as the system will still function while an upset FPGA is being reconfigured.)

The following sections describe the different aspects of this system in greater detail.

Power-on Configuration

Both FPGAs (top and bottom) shown in Figure 8 should be set for Master Serial Mode configuration (all mode pins tied Low M[2:0]<000>). The power-on configuration process executes according to the following steps:

1. Upon power-up, both FPGAs will drive their INIT pins Low until they are ready for configuration. Since they are in Master Mode, they will release their INIT pins and commence clocking the configuration data out of the serial PROM once their INIT pins have externally transitioned High. (This process can be delayed by holding INIT Low externally.)
2. The top FPGA will commence configuration first. The DONE pin of each FPGA is driven Low by each device until configuration is complete. Since the DONE pin of the top FPGA is connected to the INIT pin of the bottom FPGA, the bottom FPGA cannot commence configuration until the top FPGA has released its DONE pin upon completion of its own configuration.
3. When the top FPGA has completed configuration and has released its DONE pin, the bottom FPGA will attempt to commence configuration. However, in order for the bottom FPGA to successfully configure, both the PROM and the bottom FPGA must be reset by pulsing Low OE/$\overline{\text{RESET}}$ and PROG, respectively. This is accomplished with the IO_1 pin, which is controlled by user-defined logic and is described in "Auto-Reconfiguration" on page 90.

   NOTE: The IO_1 pin is a user-defined pin that may, if the user so chooses, co-exist on the same pin as INIT, a dual-function pin that becomes a user-programmable I/O (IOB) after configuration is complete. The IO_2 pin is also a user-defined I/O; it must be on a standard programmable I/O pin.
4. Upon configuration and activation, the top FPGA should sense that the DONE of the bottom device is Low on its IO_2 input, and subsequently pulse its IO_1 output Low for at least 300 ns. This will reset the serial PROM and force the bottom FPGA into reconfiguration
5. Upon completion of the bottom FPGAs configuration, the top FPGA's DONE should be observed High on the IO_2 input, and normal system operation will begin.

Top Level Design

As shown in Figure 8, the top level design consists of the user's basic design (logic); a duplicate of the basic design (duplicate logic); The STARTUP component (primitive); a constant Low output; a falling edge detector, and other random logic as shown; and a state machine to control the readback and auto-reconfiguration of the neighboring FPGA.

SEU Correction and Reconfiguration

The user must provide a small circuit within the top level design that will force the neighboring FPGA to reconfigure upon certain conditions. Those conditions should be:

1. The DONE of the neighboring FPGA is observed to be Low (IO_2).
2. A readback of the neighboring FPGA indicates that an upset in the configuration memory is present.
3. (Optional, not illustrated) The neighboring FPGA has held its outputs in a high-impedance state too long.

Condition 1 indicates a failed configuration or "deconfiguration", as well as controlling the Power-on Configuration sequence.

Condition 2 provides SEU correction when an SEU has been detected by readback.

Condition 3 is not illustrated in Figure 8. The basic concept is for each FPGA to be cognizant of the operational status of its neighbor FPGA. If the neighbor FPGA tri-states its pins because of a functional interrupt or effect other than an SEU to the configuration memory, *but does not seem to recover on its own,* then the system should be reset before such time has elapsed that would put the system in danger of both FPGAs being upset simultaneously. See "Optional Watch-Dog" on page 99.

If any of the above conditions occur, the FPGA should pulse the IO_1 output Low for 300 ns (min) to reconfigure the other FPGA.

The constant Low output, shown in Figure 8 as an output buffer (OBUF) tied Low, indicates whether the FPGA is online or off-line.

When an FPGA is configuring, all its outputs are in a high-impedance state. Therefore, the constant Low output will pull High indicating that the FPGA is off-line. When the FPGA is done configuring, the constant Low output will return Low.

The falling-edge detector in the active FPGA generates a pulse when the other FPGA comes back online. This pulse should be used to assert a global reset in the logic of both FPGAs. This will resynchronize all the logic of both FPGAs after one FPGA has been reconfigured, or when one FPGA has been momentarily off-line due to a transient interrupt. This is important, as it protects the hard-wired OUTPUTS from being in a state of contention.

The benefit of this practice is that the system will continue to function on one FPGA while the other is either upset or being reconfigured. However, the basic user's logic must be designed to tolerate unexpected global resets.

Readback and SEU Detection

As described in the section "Design Mitigation Techniques" on page 90, readback provides the method for detection of upsets in the configuration memory. The simplest approach is to capture the 11-bit CRC value at the end of the readback stream. See "Microcontroller for Readback" on page 92.

RB_IN and RB_OUT, shown in Figure 8, are arbitrary bus names for the readback interface and the direction of data flow between the devices.

The RB_OUT port provides external access to the READBACK primitive and consists of three separate pins (two inputs and one output). The two inputs are the readback trigger (RT) and the readback clock (CLK). These must be connected to the RT and CLK pins of the READBACK primitive (see Application Note XAPP015). The output signal is for the readback data which comes from the RD pin of the READBACK primitive.

The RB_IN port interfaces directly to the RB_OUT of the other FPGA, and thus has the same pins but in opposite direction (the clock and trigger are outputs and data is input).

The user must build the control logic for performing and capturing the readback. The process requires execution of the following steps:

1. To begin the readback, assert the RT High, and hold until readback is complete.
2. Clock continuously without interruption from the beginning to the end of readback. The clock signal MUST be between 1 MHz and 2 MHz.
3. Pipe the input readback data through a 6-bit decoder to watch for the "preamble" <111110> as shown in Table 1 on page 93.
4. When the preamble is observed, begin counting the number of clock cycles. When the count reaches the value shown in Table 1, the next bit should be a zero followed by the 11-bit CRC.
5. Compare this CRC to the expected CRC.

WARNING: The CRC of the very first readback after reconfiguration should be ignored. Only the CRC from the second (and subsequent) readback should be used.This is because the value of the expected CRC cannot be known prior to execution of a readback.

The readback control logic must be designed to do three consecutive readbacks in order to perform the first compare: the first to initialize; the second to capture the CRC; and the third to execute the compare. Each subsequent readback then results in an immediate compare. However, if the FPGA being read back is reconfigured, this process must start again from the beginning.

The CRC value captured from the second readback needs to be stored for comparison with succeeding readbacks. This can be done with registers, but should use triple module redundancy so that the wrong value is not used should one of the registers get upset.

In this case, it is acceptable to use LUTs for the voting circuit, because even if LUTs get upset, the system will eventually reconfigure and repair itself.

SEU Mitigation with STARTUP

The primary mitigation technique of this system is for the FPGA to turn off its outputs when a functional upset occurs. This is accomplished by duplicating the user's basic design and XORing output pairs. All XOR outputs should then be ORed together, along with the GSR signal, to drive the GTS. (The GSR is included in case the OR gate driving the GSR gets upset).

As mentioned earlier, the GTS signal, when asserted, will tri-state all FPGA outputs. This will keep incorrect data from propagating out into the system. The GSR and GTS of the STARTUP component are entirely asynchronous and hard-wired. Thus, do not depend on any storage elements or clock sources.

When neither device is upset, both sets of outputs will be driving. The 50 ohm series resistance (actual impedance should be specified by the designer) on each FPGA output provides impedance-matching to board traces to reduce reflections. In addition, the 100 ohm series resistance between output pairs absorbs transient contention caused by output transition skew.

Because the logic is already duplicated in each device, this mitigation approach provides an additional benefit by nicely supporting the wire-AND approach to critical control signals. See "Wire-ANDed Outputs" on page 93. Since the device itself is duplicated as well, a quadruple pin redundancy system actually results.

Combining these techniques creates a reconfigurable system that is reliable for even the most critical functions and applications.

Optional Watch-Dog

It is possible for an SEU to affect the functional operation of the design without upsetting any configuration memory latches (i.e., upsetting the stored value in a CLB flip-flop). Such an upset would not be detected by a readback, and thus would not induce a reconfiguration.

When a functional upset like this occurs, there will most likely be a discrepancy between the "Logic" and "Duplicate Logic" which will cause the FPGA outputs to a high-impedance state. Whether or not the FPGAs' design will eventually resynchronize without a reset depends entirely on the complexity of the design itself.

A simple pipelined arithmetic through-put function, such as a multiplier, will always resynchronize within the number of clock stages present between the upset flip-flop and the output. However, a highly complex state-machine may never recover. It is therefore left to the designer to determine if this is a possibility for the design in question.

If the possibility of a functionally upset design never recovering is of concern, then the designer should include a "watch-dog" timer to reset the system.

For this system the timer would be merely a counter that is clock-enabled by the constant Low output of the neighbor FPGA. When the neighbor FPGA tri-states its pins, the Low output will

pull high and thus cause the timer to start incrementing. When the timer has reached a "terminal count" value, it should pulse the GSR of both FPGAs.

It is left to the designer to determine the appropriate "terminal count" value for the application. For example, one application may require that the timer time-out before the next statistically expected upset. The time interval between upsets depends on the orbit and location. This may be a matter of seconds, minutes, hours, days, or years.

Summary

With the release of Xilinx radiation-tolerant FPGAs, engineers now have a more powerful and flexible option for programmable logic in space applications. While the techniques to mitigate the effects of SEUs are more complicated than those methods employed for older technology radiation-tolerant FPGAs, in many applications the benefits of Xilinx FPGAs are an overwhelming return for the additional design effort. These benefits include: higher density (up to 62K gates); significantly lower cost; in-circuit reprogrammability (ISP), allowing rapid changes with no rework or scrapping; and three densities utilizing the same footprint that adds to cost savings and makes room for design growth.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/15/00	1.0	Initial Xilinx release.

XAPP216 (v1.0) June 1, 2000

Correcting Single-Event Upsets Through Virtex Partial Configuration

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Co-authors: Michael Caffrey, Anthony Salazar; Los Alamos National Laboratories

Summary

This application note describes the use of partial reconfiguration in Virtex™ series FPGAs for the purpose of correcting Single Event Upsets to the configuration memory array induced by cosmic rays. It is essential for the reader to have a basic understanding of the Virtex SelectMAP™ interface as well as configuration and readback operations. An in-depth review of Xilinx Application Note XAPP138 is highly recommended.

Overview

- SEUs are unavoidable and must be corrected
- Using Partial Configuration for SEU Correction
- SEU Correction Methods
- SEU Detection
- SEU Scrubbing
- Design Examples
- Application of Static and Dynamic Cross-sections
- Reference Tables

Introduction

On-orbit, space based, and extra-terrestrial applications must consider the effects high energy charged particles (radiation) may have on electronic components. In Particular, Single Event Upsets (SEU) may alter the logic state of any static memory element (latch, flip-flop, or RAM cell). Since the user-programmed functionality of an FPGA depends on the data stored in millions of configuration latches within the device, an SEU in the configuration memory array may have adverse effects on the expected functionality.

A static upset in the configuration memory is not synonymous with a functional error. Upsets may have no effect on functionality. Design mitigation techniques, such as triple redundancy, can harden functionality against single events upsets. However, the upsets must be corrected so that errors do not accumulate.

The Virtex Series FPGA SelectMAP interface provides post-configuration read/write access to the configuration memory array. "Readback" is a post-configuration read operation of the configuration memory, and "Partial Reconfiguration" is a post-configuration write operation to the configuration memory. Readback and Partial Reconfiguration allow a system to detect and repair SEUs in the configuration memory without disrupting its operations or completely reconfiguring the FPGA.

Before continuing with this application note it is essential for the reader to have a full understanding of the basic configuration and readback operations, as well as the bit-stream format and command structure, of the Virtex Series configuration logic and SelectMAP interface. A careful review of Xilinx Application Note XAPP138 "Virtex FPGA Series Configuration and Readback" will provide this information. For further reading on the Virtex Series FPGAs' configuration architecture, see Xilinx Application Note XAPP151 "Virtex Configuration Architecture Advanced Users' Guide."

Partial Reconfiguration

Configuration Memory Architecture

The configuration memory array is divided into three separate segments: The "CLB Frames", "BRAM0 Frames" and "BRAM1 Frames." See Figure 1. The two BRAM segments contain only the RAM content cells for the Block RAM elements. The BRAM segments are addressed separately from the CLB Array. Therefore, accessing the Block RAM content data requires a separate read or write operation. Read/Write operations to the BRAM segments should be avoided during post-configuration operations, as this may disrupt user operation.

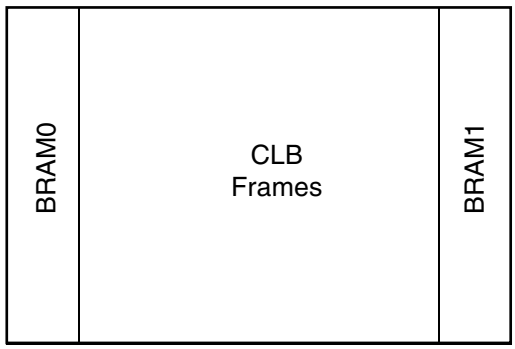


Figure 1: **Virtex Frame Segments**

The CLB Frames contain all configuration data for all programmable elements within the FPGA. This includes all Lookup Table (LUT) values, CLB, IOB, and BRAM control elements, and all interconnect control. Therefore, every programmable element within the FPGA can be addressed with a single read or write operation. All of these configuration latches can be accessed without any disruption to the functioning user design, as long as LUTs are not used as distributed RAM components.

While CLB flip-flops do have programmable features that are selected by configuration latches, the flip-flop registers themselves are separate from configuration latches and cannot be accessed through configuration. Therefore, readback and partial configuration will not effect the data stored in these registers.

However, when a LUT is used as either a distributed RAM element, or as a shift register function, the 16 configuration latches that normally only contain the static LUT values are now dynamic design elements in the user design. Therefore, the use of partial reconfiguration on a design that contains either LUT-RAM (i.e., RAM16X1S) or LUT-Shift-register (SRL16) components may have a disruptive effect on the user operation. For this reason the use of these components can not be supported for this type of operation.

However, Block RAMs (RAMB) may be used in such an application. Since all of the programmable control elements for the Block RAM are contained within the CLB Frames and the Block_RAM content is in separate frame segments, partial reconfiguration may be used without disrupting user operation of the Block RAM as design elements.

Data Frames

The configuration memory segments are further divided into columns of data frames. A data frame is the smallest portion of configuration data which may be read from, or written to, the configuration memory. The CLB array contains four categories of frame columns: one center column (eight frames), CLB columns (48 frames/column), two BRAM-Interconnect columns (27 frames/column), and two IOB columns (54 frames/column). The number of CLB columns and the size of the frames vary per device. However, the frame sizes are constant for a particular

device regardless of the column type in which it resides. The entire array may be addressed as one block, or alternatively any individual frame may be accessed as a unique block of data.

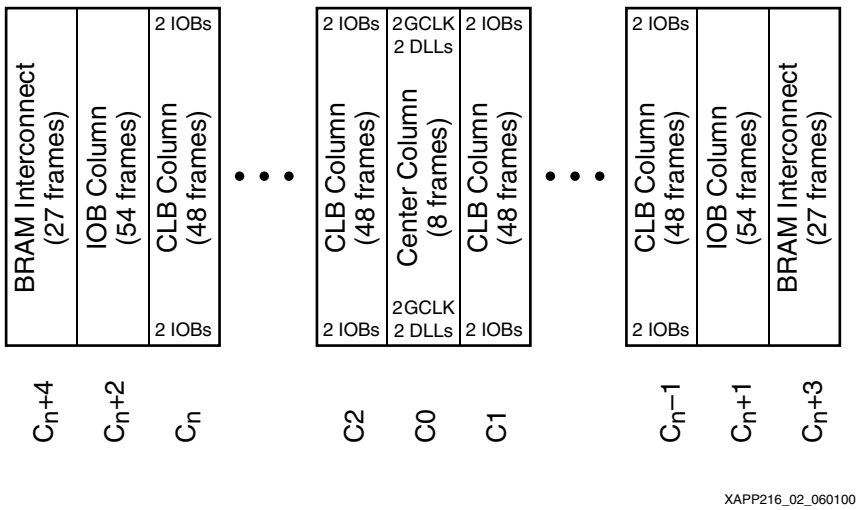


Figure 2: **CLB Frame Columns**

As shown in Figure 2, the frame columns are numbered in a "ping-pong" order which places all the even numbered columns to the left of the center column and all the odd numbered frames to the right. The frames within a column are numbered sequentially within that column away from the center. If all the frames were simply numbered sequentially in accordance with the

order of their appearance when performing a full readback of the CLB Frames, their order would be as shown in Figure 3.

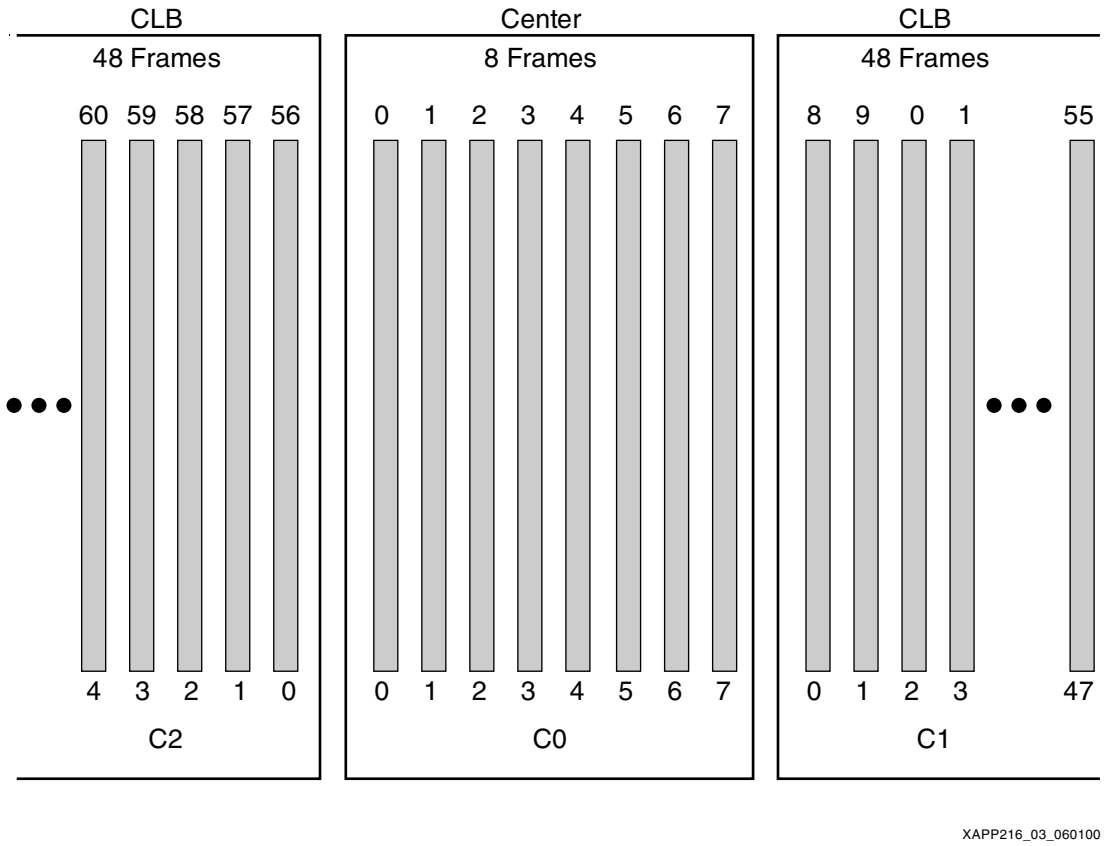


Figure 3: **Data Frame Numbering**

Partial Read/Write Operations

To write a series of data frames, the Frame Address Register (FAR) must first be set to the address of the first frame in the series. Then specify the number of data words to be written to the FDRI register followed by the data. A data-word is a 32-bit word. Therefore, the number of words to be written is the number of frames to be written times the number of words per frame (see Table 3 on page 112) plus one dummy word (typically all zeros) to follow each frame and plus one more frame of dummy words which also must be followed by a dummy word. If writing multiple frames, the first frame will be written to the address specified in the FAR and will automatically increment the address by one frame for each frame of data thereafter.

For each write operation the number of frame data words must also include a dummy word in order to complete the write operation. Data written to the FDRI register is assembled into 32-bit words and then loaded into a Frame register equal in size to one data frame. When the frame register is full the entire frame is loaded in parallel into the configuration memory latches. The last 32-bit word written is always stuck in the FDRI register. Therefore, a dummy word is needed to push the last word of the last frame of real data into the frame register in order for the entire last frame to be loaded into configuration memory.

A frame address is expressed as a major address and a minor address. The major address is the column number and the minor address is the frame number within that column. The value written to the FAR register contains a Block Type field, the major address, and the minor address. The Block Type should always be "00" to indicate the CLB Frames Segment. The Major Address is positioned in bits 17 through 24. The Minor Address is positioned in bits 9 through 16. All other bits should be "0". Therefore, to read or write the first frame of the first column, the value written to the FAR would be all zeros (00000000h).

SEU Correction Methods

SEU Detection and Single Frame Correction

One method of SEU correction is to use Readback to detect when an upset to the configuration memory has occurred. When an upset is detected only the data frame that contains the effected bit need be corrected. Using this method of writing only a single data frame, and only after an upset has occurred means that the configuration logic will be in "write mode" for the shortest amount of time. Most of the time the configuration logic will be in "read mode". This decreases the probability of an upset to the configuration logic itself from having any adverse effects to the configuration memory array. However, this method also requires some system overhead and support for the readback and detection of SEUs in the configuration memory.

Using readback for SEU detection requires a hardware implementation of algorithms for reading and evaluating each data frame. Additionally, memory space is needed to store constants and variables.

SEU Scrubbing

A simpler method to SEU correction is to omit readback and detection of SEUs and simply reload the entire CLB Frame segment at a chosen interval. This is called "scrubbing." Scrubbing requires substantially less overhead in the system, but does mean that the configuration logic is likely to be in "write mode" for a greater percentage of time. However, the cycle time for a complete scrub can be made relatively short as the SelectMAP interface is capable of operating at a throughput of 400 Mbits/s. Additionally, the chosen interval for scrub cycles should be based on the expected static upset rate for a given application or mission, and may be fairly infrequent. A longer cycle interval (time between scrubs) and shorter cycle time (scrub time) decreases the total percentage of time that the configuration logic is in "write mode."

SEU Detection

Readback and Comparison

The more traditional method of verification of the data stored in configuration memory is to readback the data and perform a bit for bit comparison. This requires the use of a mask file (.msk) and readback file (.rbb) each of which are equal in size to the original bit-stream used to configure the FPGA. This method is explained in detail in Application Note XAPP138.

This method would effectively triple the amount of system memory required for configuration and readback operations. Therefore, this method is not generally considered to be desirable for space applications.

CRC Frame Checks

Another method for readback verification and SEU detection was developed by the Los Alamos National Laboratories Space Data Systems Group. This method records a 16-bit CRC value for each data frame. During readback a new CRC value is generated for each data-frame that is read back and compared to the expected CRC result. Since a data-frame is the smallest amount of configuration memory which may be read from, or written to, the device, it is not important to know which data bit is upset but merely which data frame the upset exists in. Then only the data frame effected need be rewritten to the FPGA to correct the SEU.

This method greatly reduces the amount of system memory required to perform SEU Detection. The algorithm for calculating a CRC sum is presented in Application Note XAPP138.

SEU Correction

System Architecture

There are two different methods for implementing the CRC frame constants. For an application that will never require any update or changes to the FPGAs' design after deployment, the CRC constants for a specific FPGA design can be pregenerated in software and stored in system ROM. For applications that can accept updates for the FPGAs' bit-stream, the CRC constants

should be generated by the host system and stored in RAM. If the FPGAs' bitstream is ever updated then the CRC values can be refreshed.

Figure 4 shows a basic overview of one possible implementation of this system. The basic sub-blocks represent either logic or algorithms to interface with the Virtex SelectMAP Port, interface with the memory components, calculate and compare CRC values, and some sort of finite state machine to control the operations. The design details are left for the user to implement; however, an example design will be published by Los Alamos National Labs and posted as an addendum to this application note.

The mapping of the memory components should be done uniquely for each system. One possible method would be to store the CRC values in addresses such that the address number itself corresponds to the Frame number that the CRC value represents. This could reduce the number of processing steps, or decode logic, to access a specific CRC frame constant.

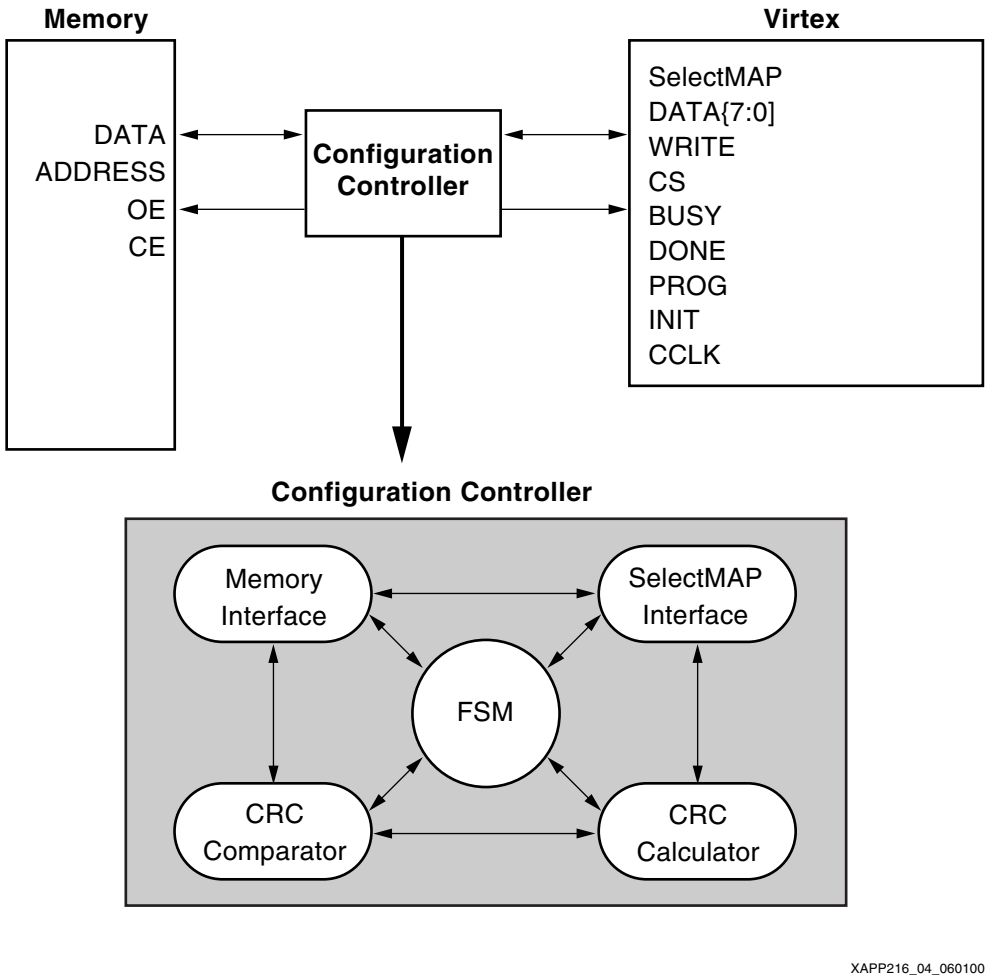


Figure 4: **Simple Configuration and SEU Correction Design**

Single Frame Correction

The process for configuration, readback and CRC calculation are omitted because these are explained in XAPP138. Whenever a data frame produces a CRC value that differs from its corresponding CRC frame constant stored in memory, the frame number should be stored for use after the readback cycle is complete. Although it is very unlikely to have more than one frame containing an SEU within one readback cycle, the CRC mismatch could potentially be produced by an SEU elsewhere in the system and not actually in the readback data. Therefore, the system should be designed to record multiple frame numbers for the correction cycle.

If the readback cycle did produce some CRC mismatches then the data for the stored frame numbers must be accessed from memory and reloaded into the FPGA. The procedure for a single frame write cycle follows:

1. **Abort**

   An Abort command is issued by holding the CS Low and the WR High for at least three clock cycles. This will reset the SelectMAP and configuration logic so that the interface may be re-synchronized. This alleviates tracking the number of clock cycles between readback and write cycles and clears any errors caused by an SEU in the configuration logic itself.

2. **Synchronize**

   Before a new process can commence the SelectMAP interface must be resynchronized by reloading the Synchronization Word.

3. **Issue WCFG Command to CMD Register**

   Enable write access to the configuration memory array by loading the WCFG command into the CMD register.

4. **Load FAR**

   Specify the frame address in the FAR with a major and minor address location. See "Frame Address Register" on page 108.

5. **Access FDRI Register**

   Use a Type 1 packet header to issue a write command to the FDRI register specifying the frame data length in 32-bit words plus one 32-bit dummy word.

6. **Load Frame Data**

   Load the data frame into the FPGA followed by one dummy frame. Each frame must be followed by a dummy word; However, the bitstream includes these dummy words at the end of each data frame.

7. **Reset CRC**

   Issue a RCRC command to the CMD register to clear the CRC register.

8. **Abort**

   Although a second Abort command may be superfluous, a resetting of the SelectMAP interface and subsequent resynchronization for any new process increases the likelihood that the process will be successful.

The data fields for the previous commands, except for the frame data, is shown in Table 1. The Abort command does not have any associated data.

Table 1: **Instruction Set for Single Frame Write Operation**

Command		Data (32 Bits)
Synchronize		AA 99 55 66
Write to CMD		30 00 80 01
WCFG		00 00 00 01
Write FAR		30 00 20 01
Frame Address		0? ?? ?? 00
Write FDRI	XQVR300	30 00 40 2A
	XQVR600	30 00 40 3C
	XQVR1000	30 00 40 4E
Frame Data		
Write CMD		30 00 80 01
RCRC		00 00 00 07

Frame Address Register

The simplest method for determining the frame address for the frame which needs to be reloaded is to count the frames during readback, starting with zero but not counting the dummy frame (see XAPP138), and then calculate the address based on that frame number.

The algorithm for calculating the frame address from the frame number needs to be conditional on which column type the frame comes from because different column types have a different number of frames and because of their organization (refer back to "Data Frames" on page 102).

Following is a description of the variables used in the subsequent equations and conditions.

N = Frame Number

Cols = The number of CLB columns in the device

Maj = Major Address portion of the FAR

Min = Minor Address portion of the FAR

DIV = Integer Division operation

MOD = Modulus remainder operation

The following algorithm is used to determine the Major and MInor Frame Address from a specific frame number and will be followed by an example exercise. It should be obvious that these conditions and equations would be greatly simplified if they were rewritten for a single device size, removing the number of columns as a variable. All variables are represented as decimal values and subsequently will need to be converted to hexidecimal before obtaining the actual FAR code.

```
Begin
   IF (0 ≤ N ≤ 7) Then {Frame is in Center Column}
      Maj = 0;
      Min = N;
   ElsIF (8 ≤ N ≤ [Cols x 48 + 7]) Then {Frame is in CLB Columns}
      Maj = (N-8)DIV(48) + 1;
      Min = (N-8)MOD(48);
   ElsIF ([Cols x 48 + 8] ≤ N ≤ [Cols x 48 + 115]) Then {Frame is in
   IOB Columns}
      Maj = (N-Colsx48-8)DIV(54) + Cols + 1;
      Min = (N-Colsx48-8)MOD(54);
   ElsIF ([Colsx48+116] ≤ N ≤ [Colsx48+169]) Then {Frame is in BRAM
   Interconnect}
      Maj = (N-Colsx48-116)DIV(27) + Cols + 3;
      Min = (N-Colsx48-116)MOD(27);
   End IF;
End;
```

Example

In this example the target device is an XQVR300. Therefore, the Cols=48. If the frame that needs to be corrected is the 2373rd valid data frame that was read back (not counting the dummy frame), then counting from zero, the frame number is N=2372.

```
   Colsx48 = 48x48 = 2304 and N-2304 = 2372 - 2304 = 68;
   N satisfies the third condition: 2312 ≤ N ≤ 2419; Therefore,
   Maj = (N-Colsx48-8)DIV(54) + Cols + 1 = (60)DIV(54) + 49 = 50;
```

And

Min = (N-Colsx48-8)MOD(54) = (60)MOD(54) = 6;

Converting these to 8-bit Binay values gives the following major and minor addresses:

Major: 00110010; Minor: 00000110;

Inserting the Major Address into bits 17 through 24, the Minor Address into bits 9 through 16, and placing zeros in all other positions gives an FAR value of:

FAR(31:0) =0000 0000 0110 0100 0000 1100 0000 0000b = 00 64 0C 00h;

SEU Scrubbing

Scrub Data and Flow

Scrubbing is a much simpler approach to SEU correction because it does not require any readback or data verification operations, nor does it require any data generation when reloading the data frames.

In short, the process is to reload the bit-stream starting at the beginning, but stopping at the end of the first write to the FDRI register. In a standard bit-stream the first write to the FDRI register includes all the configuration data for the CLB Frames segment of the memory map. The rest of the bit-stream contains the BRAM segments, a CRC check, and the start-up sequence, all of which are not applicable to partial reconfiguration. No adjustments to the data or headers are needed.

A scrub cycle should be preceded and followed by an Abort operation. However, the Abort operation preceding the scrub cycles may be omitted if one Abort cycle is inserted after the completion of the initial configuration of the FPGA. The bitstream already contains the synchronization word at the beginning. The only support circuitry necessary is a counter to generate memory addresses (if necessary), and decode logic to toggle the control signals of the memory and SelectMAP interface at specific count values. This is the mechanism that controls how much of the bitstream is loaded. An example of this is shown in Figure 5. This example does not account for the initial configuration of the FPGA. However, the necessary additions to perform an initial configuration before the first scrub is fairly straight forward and left to the reader. For additional reading, XAPP137 provides a design example of using an interface logic device to configure a Virtex FPGA from a parallel memory source. If the FPGA is to be configured from a Serial PROM, then adding a serial-parallel converter to the interface would allow the serial prom to act as the data source for both configuration and scrubbing. Since

Scrubbing reloads the majority of the bitstream from the beginning, randomly accessible memory is not required.

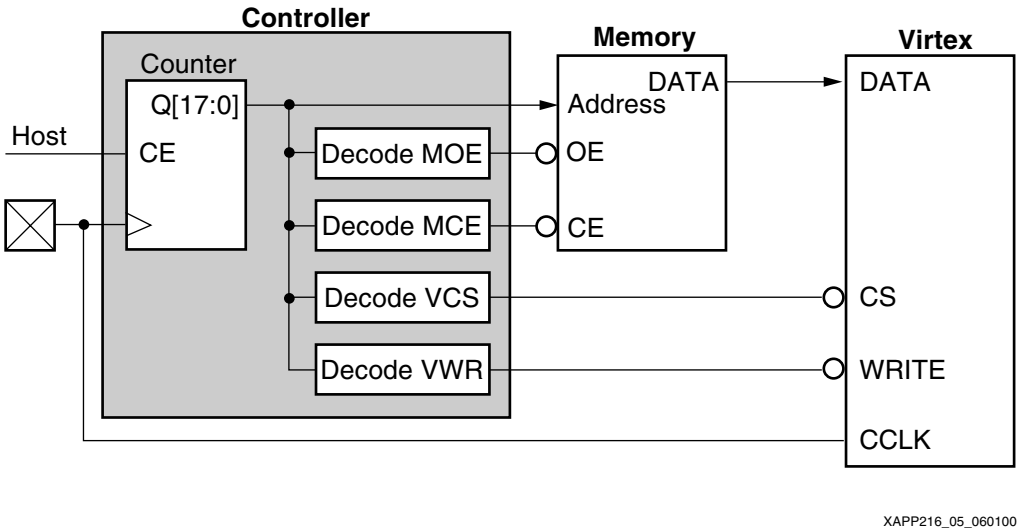


Figure 5: **Scrubbing Control Circuit**

The example shown in Figure 5 demonstrates the use of a parallel (8-bit wide) memory device. This allows the data signals to be connected directly from the memory to the Virtex SelectMAP data pins. If the memory's data ports are of any other configuration then the data should be reorganized into 8-bit words within the control chip.

For this example a simple counter is a sufficient state machine to control the scrubbing operations. The LSB outputs of the counter (number depends on the size of the memory) may be used as the address for the memory module. The example uses an 18-bit counter because this is the minimum value for a V300 bit-stream. A V600 or V1000 would require a larger counter. Additionally, the system clock may be too fast for the configuration interface (50 MHz max). In which case the address lines could be shifted to higher order bits of the count value leaving the lower order bits to serve as a clock divider.

There are four signals that need to be decoded from the Counter: MOE (Memory Output Enable), MCE (Memory Chip Enable), VCS (Virtex Chip Select), and VWR (Virtex Write). The complexity of these decoders and their associated values depends on how many Memory chips and FPGAs are being designed into the system. Since this is an entirely application specific variable we will simplify this example further by assuming a single memory chip and a single FPGA.

If the system had several memory chips, each memory would require its own MCE decoder. However, for one memory the MCE may be eliminated altogether and tied to the MOE decoder. The MOE must disable the memory's output during an Abort sequence. However, the VCS and VWR may not be combined, even for a single FPGA implementation, because the Abort sequence requires separate control of these signals.

Table 2 shows the state transitions for a complete scrubbing operation, including a trailing Abort sequence, and the associated clock cycles for each state. One clock cycle represents one byte

of data transferred. If the Counter is to be used as a Configuration Clock (CCLK) divider as well, then the number of clock transitions would need to be multiplied by the Divisor.

Table 2: **Scrubbing State Transitions**

States					Clock Cycles		
Type	**MOE**	**MCE**	**VCS**	**VWR**	**XQVR300**	**XQVR600**	**XQVR1000**
Load	L	L	L	L	207,972	435,312	745,596
Abort	H	H	L	H	4		
Disable	H	H	H	H	1		

Note: The clock cycles specified for the load operation are based on the bitstream format generated by the bitgen utility version 2.1i. If using any other version then these numbers should be manually verified in the bitstream.

The system also needs some sort of mechanism to control how often a scrub cycle takes place. In Figure 5 this is shown simply as a connection from the Host System to the CE input of the counter. Consideration is also needed for a reset control to the counter. If the desired time between scrub cycles is constant, then this could be automated by using another counter to control the CE of the scrub counter and another decoder to control a synchronous reset of the counters. Choosing how long to wait between scrub cycles (Scrub Rate) should be determined primarily from the expected upset rate for the specific application, orbit or mission.

Scrub Rates

A Scrub Rate describes how often a scrub cycle should occur. It may be denoted by either a unit of time between scrubs, or a percentage (scrub cycle time divided by the time between scrubs). The scrub rate should be determined by the expected upset rate of the device for the given application.

Upset rates are calculated from the Static Bit Cross Section (see Data Sheet) of the device and the charged particle flux the application or mission is expected to endure. For other technologies, the upset rate is an indication of how often the system will have to tolerate a functional bit error. But this is not precisely the case for an FPGA.

The static cross-section for a given device is derived by determining the cross-section per bit (obtained through experimentation and measurement) multiplied by the number of bits in the device. The static cross-section for a Virtex Series FPGA may be orders of magnitude higher than what the experienced space applications designer might be used to. This is because of the high density of configuration latches. But this upset rate does not carry the same meaning as it does for other technologies.

For example, lets compare a 6,000 flip-flop ASIC to a 6,000 flip-flop Virtex Series FPGA. If the ASIC and the FPGA have similar process geometries, then the static cross-section per bit will be similar for both devices. However, the device cross-section is the bit cross-section multiplied by the number of bits in the device. For a 6000 flip-flop ASIC the number of bits is 6000, but the a Virtex FPGA this number is 6000 plus 1.7 Million (approximately).

However, for an ASIC, a bit upset is considered to be a definite functional bit error. This would be an incorrect assumption for an FPGA. An upset in the configuration memory may or may not have any effect on the functional integrity of the user's design in the FPGA.

Design techniques may be applied to strengthen the functional integrity of the user design and protect it from the effect of any Single Event Upset. This process is called "SEU Mitigation." These design techniques are described in Xilinx Application Note XAPP186: "Space Application Design Techniques for the Virtex QPRO™ Radiation Hardened Series FPGA."

Where systems that include ASIC technology use a static upset rate to determine how often a functional bit failure may be expected, systems that use Virtex Series FPGAs should define a "Dynamic Upset Rate" for this purpose. The application of a dynamic upset rate is discussed in

the previously mentioned application note and is not covered in this paper. However, the necessary assumption is that the scrub rate should be set such that any SEU on the configuration memory will be fixed before the next will occur. Additionally, the life span of an SEU, time between the occurrence of the upset and it's subsequent correction, should be minimized. It is entirely up to the designer to choose the scrub rate. However, a good "rule of thumb" is to place the scrub rate at one order of magnitude from the upset rate. In other words, the system should scrub, on average, ten times between upsets.

For example, if we were to assume a bit upset rate of once per hour and a configuration clock frequency of 10 MHz, then the scrub rate should be once every six minutes. Thus, the scrub time, for a V1000 is 80 ms. Therefore, the scrub rate as a percentage would be 0.2%. Meanwhile, the FPGA will be capable of carrying out it's operations and functioning normally. It's ability to do so is a function of the design methodologies and mitigation strategies employed in the system.

Reference Tables

Table 3: **Device Statistics and Static Elements**

Devices	XQVR300	XQVR600	XQVR1000
CLB Array Size (RowxCol)	32 x 48	48 x 72	64 x 96
CLB Flip Flops	6,144	13,824	24,576
Select Block RAM (bits)	65,536	98,304	131,072
Frames	2474	3626	4778
Words (32-bit) per Frame (Including one dummy word)	21	30	39
Configuration Latches	1,583,360	3,364,928	5,810,048

Revision History

The following table shows the revision history for this document.

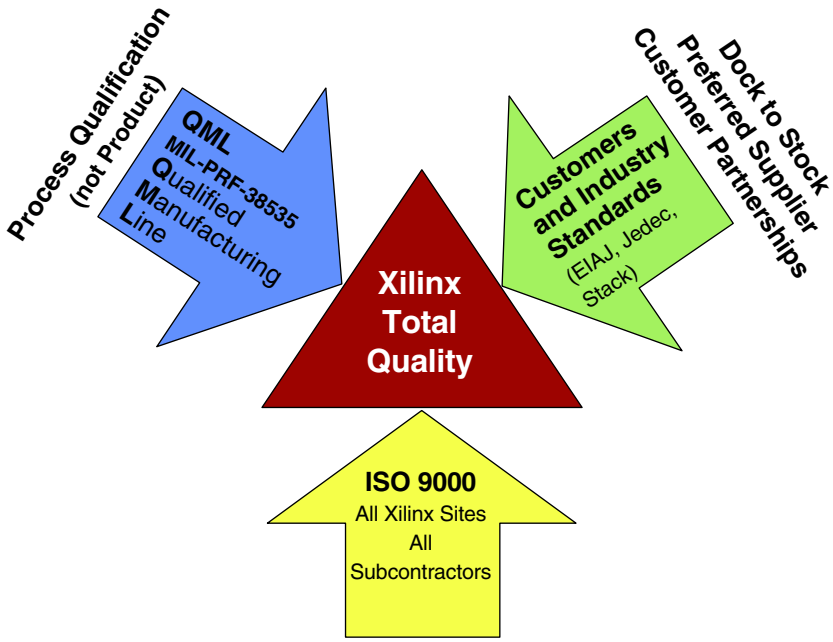
Date	Version	Revision
06/01/00	1.0	Initial Xilinx release.

QPRO Quality and Reliability and Manufacturing Flow Table of Contents

QPRO High-Reliability QML Products Quality and Reliability Program

Quality Systems Compliance:

The quality level of all Xilinx products are assured by strict compliance to several world wide standards. These standards include QML, ISO9000 (9001 and 9002), STACK, PURE, Siemen's 72500, and others (see Table 1 on page 2). All Xilinx products are manufactured in compliance with the rigorous quality requirements of these standards. This includes all of our commercial grades, our QML product lines and our MIL-M-38510 full "B-grade" Military and "T-grade" Radiation Tolerant product lines. However, not all product lines are screened to the screening requirements of MIL-M-38510. While all products are manufactured on QML certified lines and are capable of passing the screening levels of MIL-M-38510, only those products designated as compliant to these screening levels are so tested. A comparison of the various flows available from Xilinx is detailed in Table 2.



QML Background

In 1994, Dr. William Perry issued a mandate that became known as the "Perry Initiative". It directed all contractors involved in the design and/or upgrade of military equipment(s) to utilize performance standards to define (hopefully) Commercial Off the Shelf (COTs) parts for use in these military systems. After this directive, it became mandatory for a manufacturer to utilize performance standards to define parts to be used in military systems, and it took a waiver from the government for the manufacturer to specify and/or utilize MIL-Spec parts. This was done to (hopefully) remove unnecessary costs from defense procurements. Like all generalizations, this one had its exceptions.

Fortunately, the defense industry with the aid of DSCC (then known as the Defense Electronics Supply Center, DESC) was already moving in this direction. In early 1995, the government formally recognized the QML concept in its issuance of MIL-PRF-38535. This directive went beyond the MIL-SPEC status of parts and gave manufacturers a cost effective way to provide military customers with the quality and reliability levels they needed, while meeting the "performance-based" requirements of the Perry Initiative. This methodology was the

establishment of QML (Qualified Manufacturing Lines) originally audited and overseen by DSCC but eventually governed by the TRB (Technical Review Board) of the certifying manufacturer.

Table 1: **Quality Standards**

Standard	Description
QML	A standard for the Qualification of Manufacturing Lines, instituted by DSCC as part of MIL-PRF-38535. Full compliance certified at Xilinx by DSCC in November, 1997.
ISO9000	An international standard for implementation of Quality systems. ISO9001 is the standard which includes design, manufacturing and testing. Xilinx compliance was registered to ISO9001 by an independent auditor in November, 1997.
STACK	A consortium of international electronic manufacturers who share pre-competitive data and establish standards for qualification and reliability assessment. Xilinx was audited and found compliant to STACK 0001 in June, 1994.
PURE	An association of European equipment makers concerned with quality and reliability. PURE members are committed to the use of plastic components in rugged environments. Their actions are supported by the French and Swedish Ministries of Defense. Xilinx was audited and found compliant to PURE requirements in March, 1997.
72500	Siemen's 72500 is an international reliability and qualification specification that is imposed on all suppliers of high-reliability products by Siemens. Xilinx was found to be compliant to Siemens 72500 in 1994.

Screening-In Quality

The Qualified Parts List was the government's original attempt to establish a supply of integrated circuit products with assured quality and reliability levels. This concept establish a "cookbook" of screening tests (defined by then MIL-STD-883) to which each and every part had to be subjected. While the standardization of these flows led to a supply of products (from various manufacturers) capable of meeting the government's quality and reliability requirements, the tracking and screening (and the fallout of product through the screening process) led to high costs of manufacturing, and hence to high procurement costs. Indeed, the paperwork or documentation costs of product often exceeded the costs of manufacture of the devices themselves. But the primary limitation of this methodology was that it required the "screening-in" of reliability through a rigid set of tests that every manufacturer of every part had to implement for every lot. The method made no allowances for design similarity, design process control, SPC, wafer scale reliability monitoring, or other equivalent (or superior) methodologies to be substituted for the screening.

Best Commercial Practices

While the QPL system worked well for years, it suffered from stagnation. It did not allow the implementation of advances in technology or advances in methodology (like some of those cited above). Thus, while the commercial semiconductor industry made great strides in the quality and reliability (and yield) of its products (and hence the cost), the military establishment was chained to the "screening-in" methodology. That changed in 1995 when DSCC published the QML concepts. The major change between the two systems is that the QPL system was stagnant and strictly prescribed, while the QML system was flexible and allowed the incorporation of those "best commercial practices" that improve component quality and reliability while decreasing costs. Finally, it was possible to establish the "performance based" standards mandated by Dr. Perry and gain the flexibility and process improvements that came from the incorporation of "best commercial practices" while assuring the military needs for

quality and reliability. In 1998 the DOD allowed the approval of off-shore wafer fabs (off shore assembly had been available for several years) as sourceing for QPL and QML devices, extending the number and availability of more total system solutions to those customers who elect QML certified products.

Current Status

Xilinx was audited by DSCC in November 1997, was found to be in full compliance with the requirements of MIL-M-38535 and was granted full status as a QML supplier. In 1998 and 1999 DSCC was invited by Xilinx to participate in the Xilinx annual audits of our hermetic assembly supplier and two of our wafer fabrication suppliers, and in all three instances DSSC and Xilinx confirmed full compliance of these suppliers to the requirements of the QML program. Future supplier management and the audit conformance demonstration of additional suppliers was left to the control of the Xilinx Technical Review Board. In February, 2000 DSCC again visited Xilinx and reviewed our conduct of the QML program and the performance of our Technical Review Board. At that time Xilinx proposed “class T” flow was reviewed and Xilinx was approved to manufacture and certify “class T” products for the radiation hardened communities (both commercial and military).

What QML Means Today

From a customer’s stand point, QML means that the supplier has the ability to rapidly convert to newer, superior technologies. Reduced screening tests mean reduced lead times and lower manufacturing costs. Designing-in and manufacturing-in reliability means that product is not handled unnecessarily during the screening steps. Rather, process design, control and SPC are strictly monitored by the manufacturer’s Technical Review Board. This, combined with robust reliability monitoring programs and sound technical assessments, ensures that product manufactured under the QML flows meet or exceed the reliability and quality of product manufactured utilizing screening. Indeed today, per directives from DSCC and from Dr. Perry, QML products represent the preferred procurement methodology for high reliability integrated circuits for use in military systems.

It should be noted that the incorporation of QML manufacturing flows does not throw out the baby with the bath water. Xilinx QML products still retain the special services military customers require. These includes configuration control, device traceability, standard supplier certification and obsolescence control. Indeed, QML products represent the most cost effective methodology to meet the quality and reliability requirements of military equipment manufacturers.

ISO9000

All aspects of the Quality Assurance Program at Xilinx have been designed to eliminate the root cause of defects by prevention, rather than to try to remove defects through inspection. This is the heart of the ISO9000 philosophy, and is in concert with the QML programs referenced above. A quality management system is in place at Xilinx which is in full compliance with the requirements of ISO9001. Xilinx has been audited and found in full compliance to ISO9001:1994 by an independent auditor and was registered in November 1997. Xilinx registration covers “the design, manufacturing and testing of programmable logic devices”. Xilinx was the first “fabless” semiconductor company to be registered as a “manufacturer of semiconductor products”, due to the engineering support, the process control and partner relationships we exhibited with our wafer fabrication suppliers.

Those aspects of ISO conformance which are in place at Xilinx include the following 16 points:

1. **Management Review:** a comprehensive system of management attention to and direction of all aspects of company performance with directly affects customers. This policy is implemented and understood at all levels of the organization.
2. **Quality Systems:** are in place to ensure that all Xilinx products conform to customer specifications. These systems facilitate, measure and foster the continuous improvement process.

3. **Contract Review:** is conducted to ensure that each contract adequately defines and documents customer requirements, and that compliance is assured or differences negotiated and agreed.
4. **Document Control:** procedures are established and maintained to control all documents and data that relate to the performance of Xilinx business and processing requirements. All access to these documents is electronically assured to be the latest revision and properly controlled.
5. **Purchasing**: procedures are in place to ensure that all purchased products and materials conform to specified requirements. Special attention is paid to the performance of our subcontractors, all of whom are ISO9000 registered.
6. **Product Identification and Traceability:** is maintained throughout the manufacturing process, and is uniquely identified through product markings.
7. **Process Control:** is assured by identifying and planning those processes which directly affect the quality of our products, whether performed by Xilinx or by our subcontractors. All Xilinx subcontractors are ISO9000 registered.
8. **Inspection and Test**: is performed to ensure that incoming product is verified (both by Xilinx and our Subcontractors) to be compliant with requirements.
9. **Inspection, Measuring and Test Equipment**: is calibrated in conformance with ANSI/NCSL Z540-I-1994 (and former MIL-REF-45662) and maintained to ensure consistent verification of specification compliance.
10. **Inspection and Test Status**: products are uniquely identified throughout the manufacturing process, both at Xilinx and at our qualified subcontractors. Control of Non-Conforming Product is assured through disposition procedures which are defined to prevent the shipment of non-conforming product.
11. **Corrective Action**: processes are documented and implemented to prevent the recurrence of product non-conformance. Root cause elimination through corrective action is the main focus of ISO9000.
12. **Handling, Storage, Packaging and Delivery:** procedures are defined and implemented to prevent damage or deterioration of product once manufacturing is complete.
13. **Quality Records**: procedures are established and maintained for the collection, indexing, filing, and storage of quality records.
14. **Internal Quality Audits**: are carried out to verify that quality activities comply with the documented requirements and further, to determine their effectiveness. These audits are regularly supplemented by our independent auditors, by our customers, and by DSCC.
15. **Training:** procedures have been established and are implemented to identify the training needs of all personnel whose performance affects the quality and reliability of our products. Personnel performing such activities are qualified based on appropriate training, education and/or experience.
16. **Statistical Techniques:** are in place at Xilinx and at our subcontractors for verifying the acceptability of process capabilities and product characteristics.

Manufacturing Flows

All Xilinx Military classes have the following items under formal control:

- Wafer Scale Reliability Data
- Full Temperature Characterization
- Maverick Lot Elimination
- TRB Review (Monthly)
- Periodic Reliability Monitor
- "QCI Coverage (groups B,C,D)"

Table 2: **Manufacturing Flow Tests**

Test	Methodology	Class T	Class Q	Class N	M-grade
Specification Control	Documentation	SMD	SMD	SMD	Data Sheet
Mask Control	per Internal Controlled Documents	Yes	Yes	Yes	No
QML Qualified Wafer Fab	per MIL Prf 38535	Yes	Yes	Yes	Yes
Wafer Lot Acceptance	per Internal Parametric Specifications	Yes	Yes	Yes	Yes
Lot Radiation Hardness Assurance	per Method 1019 / per wafer fab lot	Yes	No	No	No
QML Qualified Assembly	per MIL Prf 38535	Yes	Yes	Yes	Varies
Destructive Bond Pull	per Method 2011, sample, SPC	Yes	Yes	Yes	Yes
Internal Visual	per Method 2010B / 100%	Yes	Yes	Sample only	Sample only
Temperature Cycling	per Method 1010 / 100%	Yes	Yes	No	No
Constant Acceleration	per Method 2001 / 100%	Yes	Yes	N/A	No
Fine/Gross Leak	per Method 1014 / 100%	Yes	Yes	N/A	Yes (ceramic only)
Radiographic Inspection	per Method 2012, sample, SPC	Yes	Yes	Yes	Yes
Interim (Pre Burn-In) Electrical Parameters	Per SMD or Data Sheet	Yes	Yes	N/A	N/A
Burn-In	per Method 1015, Condition B / 100%	Yes	Yes	No	No
Post Burn-In Electrical	per SMD or Data Sheet	Yes	Yes	N/A	N/A
Percent Defective Allowable (PDA) Calculation	per SMD or Data Sheet	Yes	Yes	N/A	N/A
Final Electrical Test	per SMD or Data Sheet / 3 temps	Yes	Yes	Class temp only	Class temp only
Group A sample, 0/116 every lot	per SMD or Data Sheet / 3 temps	Yes	Yes	Class temp only	Class temp only
External Visual	per Method 2009 /100%	Yes	Yes	Plastic equivalent	Commercial

Please note that, as a QML supplier, Xilinx reserves the right to substitute alternate control methodologies (which assure equivalent quality and reliability) for some of the screening elements of the class B flow on a part by part basis. Any such decisions are approved by the Xilinx Technical Review Board and communicated to DSCC (along with technical justification) on a quarterly basis.

For more information, refer to Xilinx Quality and Reliability web site:

http://www.xilinx.com/products/qa_data/index.htm

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/15/00	1.0	Initial Xilinx release.

QPRO Packaging and Thermal Characteristics
Table of Contents

Packages and Thermal Characteristics: High-Reliability Products

Package Information

Inches vs. Millimeters

The JEDEC standards for PLCC, CQFP, and PGA packages define package dimensions in inches. The lead spacing is specified as 25, 50, or 100 mils (0.025", 0.050" or 0.100").

The JEDEC standards for PQFP and HQFP packages define package dimensions in millimeters. These packages have a lead spacing of 0.5 mm, 0.65 mm, or 0.8 mm.

Because of the potential for measurement discrepancies, this Data Book provides measurements in the controlling standard only, either inches or millimeters. (See Table 1 for package dimensions.)

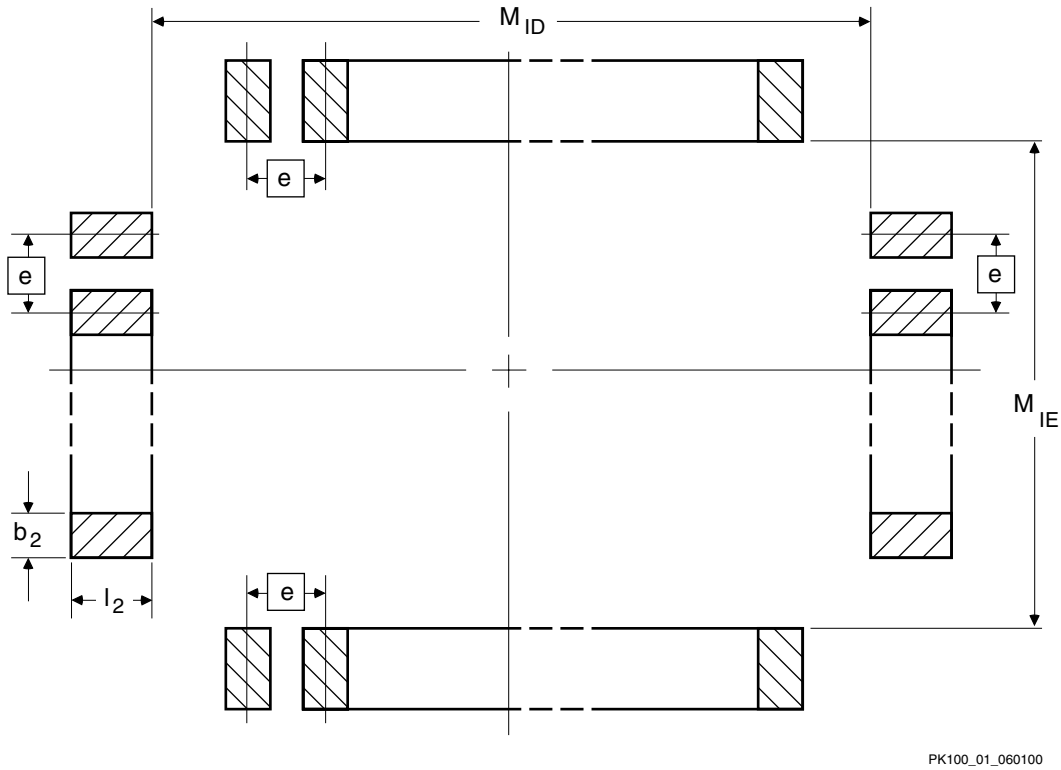


Figure 1: **EIA Standard Board Layout of Soldered Pads for QFP Devices**

Table 1: **Dimensions for Xilinx Quad Flat Packs(1)**

Dimension	PQ100	HQ160, PQ160	HQ208, PQ208	HQ240, PQ240	HQ304
M_{ID}	20.40	28.40	28.20	32.20	40.20
M_{IE}	14.40	28.40	28.20	32.20	40.20
e	0.65	0.65	0.50	0.50	0.50
b_2	0.3-0.5	0.3-0.5	0.3-0.4	0.3-0.4	0.3-0.4
l_2	1.80(2)	1.80	1.60	1.60	1.60

Notes:
1. Dimensions in millimeters
2. For 3.2 mm, footprint per MS022, JEDEC Publication 95.

Suggested Board Layout of Soldered Pads for BGA, CGA and FG Packages

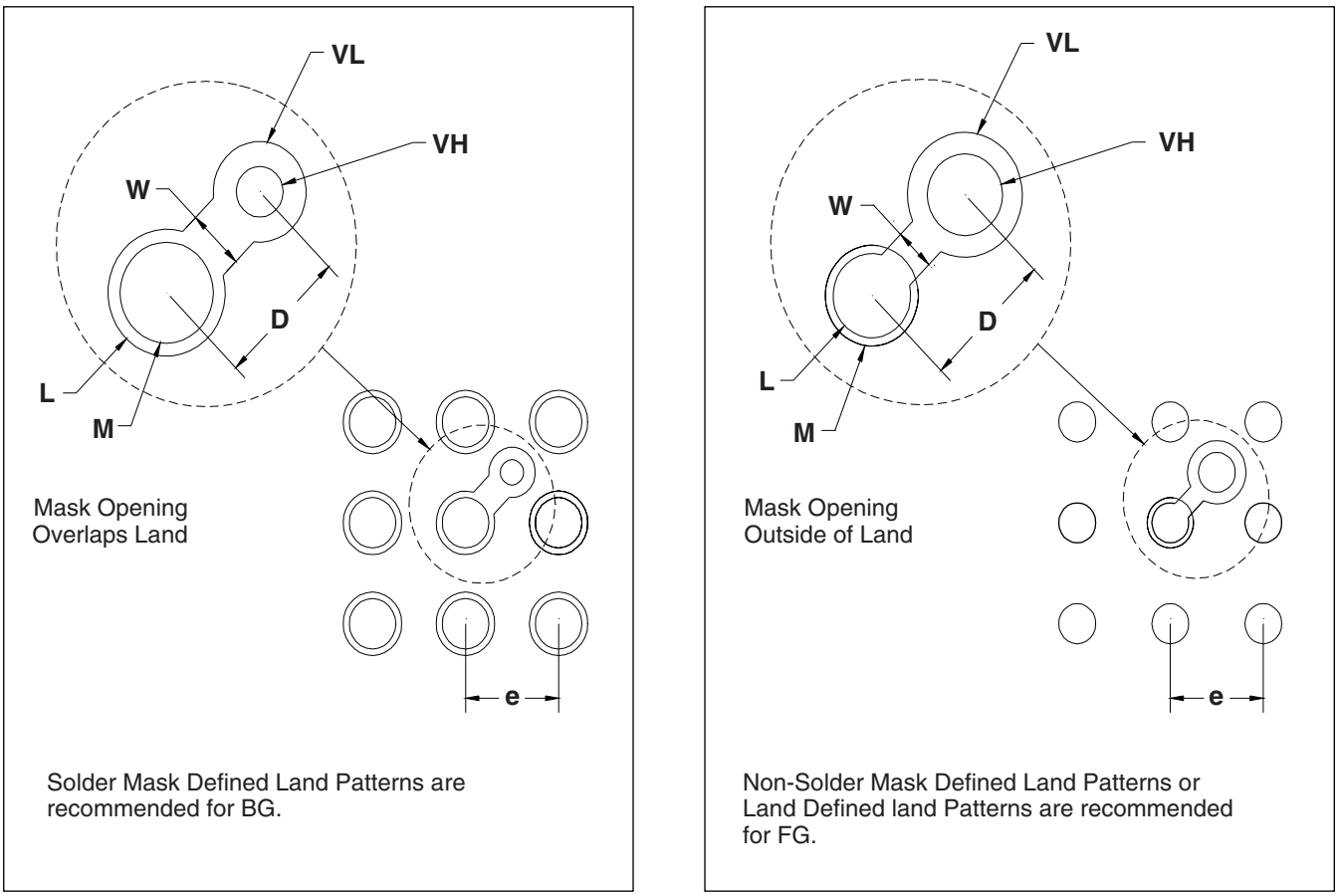


Figure 2: **Suggested Board Layout of Soldered Pads for BGA and FG Packages**

Table 2: **Soldering Dimensions for BG and CG Packages**

	BG225	BG256	BG352	BG432	BG560	CG560
Solder Land (**L**) diameter	0.89	0.79	0.79	0.79	0.79	0.79
Opening in Solder Mask (**M**) diameter	0.65	0.58	0.58	0.58	0.58	0.58
Solder (Ball) Land Pitch (**e**)	1.5	1.27	1.27	1.27	1.27	1.27
Line Width between Via and Land (**W**)	0.3	0.3	0.3	0.3	0.3	0.3
Distance between Via and Land (**D)**	1.06	0.9	0.9	0.9	0.9	0.9
Via Land (**VL**) diameter	0.65	0.65	0.65	0.65	0.65	0.65
Through Hole (**VH)** diameter	0.3	0.3	0.3	0.3	0.3	0.3
Pad Array	Full	-	-	-	-	-
Matrix or External Row	15 x 15	20 x 20	26 x 26	31 x 31	33 x 33	33 x 33
Periphery rows	-	4	4	4	5	5

Table 3: **Soldering Dimensions for FG Packages**

	FG256	FG456	FG556	FG676	FG680	FG860	FG900	FG1156
Solder Land (**L**) diameter	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4
Opening in Solder Mask (**M**) diameter	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Solder (Ball) Land Pitch (**e**)	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Line Width between Via and Land (**W**)	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13
Distance between Via and Land (**D**)	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7
Via Land (**VL**) diameter	0.61	0.61	0.61	0.61	0.61	0.56	0.61	0.61
Through Hole (**VH**) diameter	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3
Pad Array	Full	Full	-	Full	-	-	Full	Full
Matrix or External Row	16 x 16	22 x 22	30 x 30	26 x 26	39 x 39	42 x 42	30 x 30	34 x 34
Periphery rows	-	-	7	-	5	6	-	-

Cavity Up or Cavity Down

Most Xilinx devices attach the die against the inside bottom of the package (the side that does not carry the Xilinx logo). This is called cavity-up, and has been the standard IC assembly method for over 25 years. This method does not provide the best thermal characteristics. Pin Grid Arrays (greater than 130 pins) and Ceramic Quad Flat Packs are assembled "Cavity Down", with the die attached to the inside top of the package, for optimal heat transfer to the ambient air.

For most packages this information does not affect how the package is used because the user has no choice in how the package is mounted on a board. For Ceramic Quad Flat Pack (CQFP) packages however, the leads can be formed to either side. Therefore, for best heat transfer to the surrounding air, CQFP packages should be mounted with the logo up, facing away from the PC board.

Clockwise or Counterclockwise

The orientation of the die in the package and the orientation of the package on the PC board affect the PC board layout. PLCC and PQFP packages specify pins in a counterclockwise direction, when viewed from the top of the package (the surface with the Xilinx logo). PLCCs have pin 1 in the center of the beveled edge while all other packages have pin 1 in one corner, with one exception: The 100-pin and 165-pin CQFPs (CB100 and CB164) for the XC3000 devices have pin 1 in the center of one edge.

CQFP packages specify pins in a clockwise direction, when viewed from the top of the package. The user can make the pins run counterclockwise by forming the leads such that the logo mounts against the PC board. However, heat flow to the surrounding air is impaired if the logo is mounted down.

Thermal Management

Modern high-speed logic devices consume an appreciable amount of electrical energy. This energy invariably turns into heat. Higher device integration drives technologies to produce smaller device geometry and interconnections. With smaller chip sizes and higher circuit densities, heat generation on a fast switching CMOS circuit can be very significant. The heat removal needs for these modern devices must be addressed.

Managing heat generation in a modern CMOS logic device is an industry-wide pursuit. However, unlike the power needs of a typical Application Specific Integrated Circuit (ASIC) gate array, the power requirements for FPGAs are not determined as the device leaves the factory. Designs vary in power needs.

There is no way of anticipating the power needs of an FPGA device short of depending on compiled data from previous designs. For each device type, primary packages are chosen to handle "typical" designs and gate utilization requirements. For the most part the choice of a package as the primary heat removal casing works well.

Occasionally designers exercise an FPGA device, particularly the high gate count variety, beyond "typical" designs. The use of the primary package without enhancement may not adequately address the device's heat removal needs. Heat removal management through external means or an alternative enhanced package should be considered.

Removing heat ensures the functional and maximum design temperature limits are maintained. The device may go outside the temperature limits if heat build up becomes excessive. As a consequence, the device may fail to meet electrical performance specifications. It is also necessary to satisfy reliability objectives by operating at a lower temperature. Failure mechanisms and the failure rate of devices depend on device operating temperature. Control of the package and the device temperature ensures product reliability.

Package Thermal Characterization Methods and Conditions

Method and Calibration

Xilinx uses the indirect electrical method for package thermal resistance characterization. The forward-voltage drop of an isolated diode residing on a special test die is calibrated at constant forcing current of 0.520 mA with respect to temperature over a correlation temperature range of 22°C to 125°C (degree Celsius). The calibrated device is then mounted in an appropriate environment (still air, forced convection, circulating FC-40, etc.) Depending on the package, between 0.5 to 4 watts of power (P_d) is applied. Power (P_d) is applied to the device through diffused resistors on the same thermal die. The resulting rise in junction temperature is monitored with the forward-voltage drop of the precalibrated diode. Typically, three identical samples are tested at each data point. The reproducibility error in the setup is within 6%.

Definition of Terms

T_J Junction Temperature — the maximum temperature on the die, expressed in °C

T_A Ambient Temperature — expressed in °C.

T_C The temperature of the package body taken at a defined location on the body. This is taken at the primary heat flow path on the package and represents the hottest part on the package — expressed in °C.

T_I The isothermal fluid temperature when junction to case temperature is taken — expressed in °C.

P_d The total device power dissipation — expressed in watts.

Junction-to-Reference General Setup

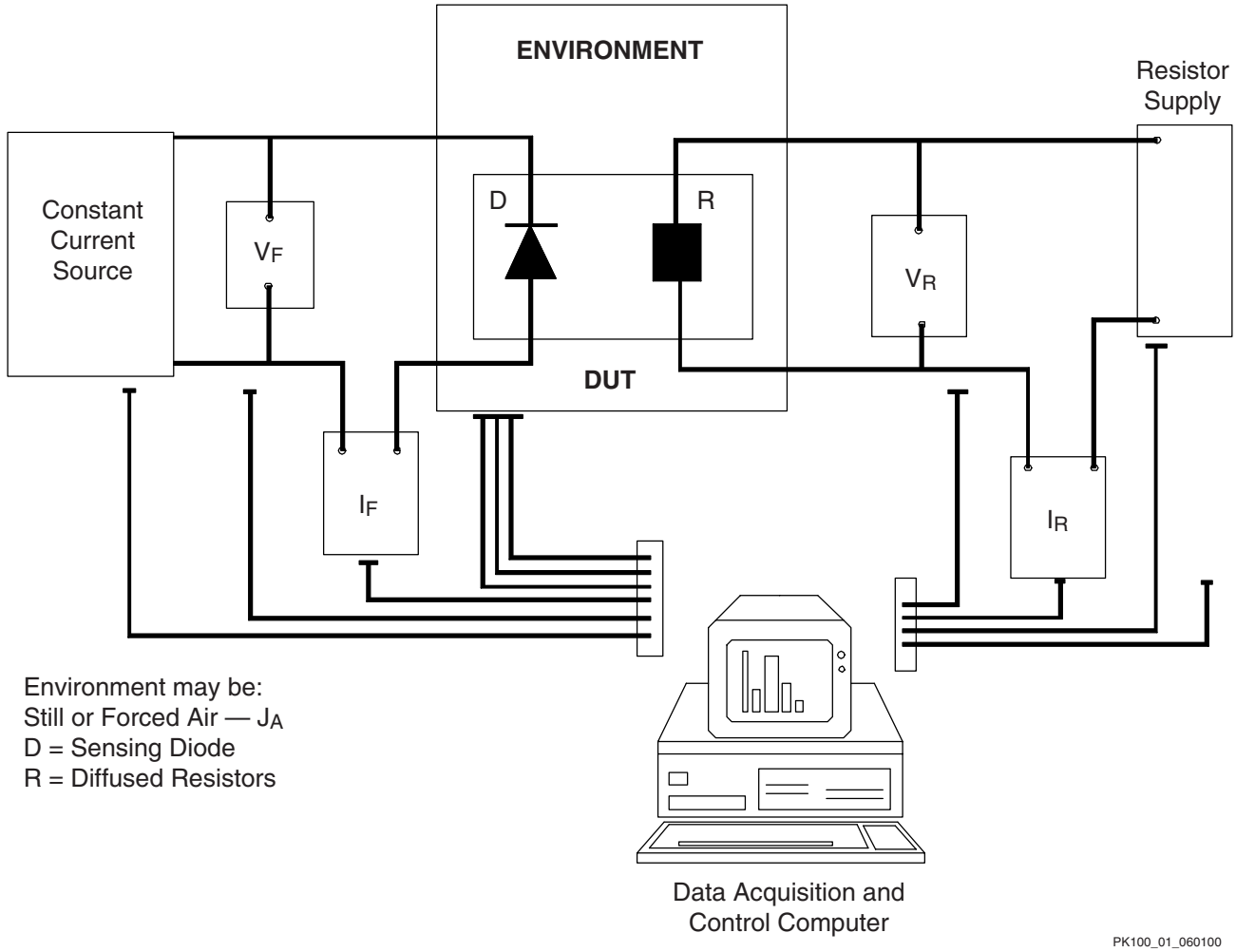


Figure 3: **Thermal Measurement Set-Up (Schematic for Junction to Reference)**

Junction-to-Case Measurement — Θ_{JC}

Θ_{JC} is measured in a 3M Flourinert (FC-40) isothermal circulating fluid stabilized at 25°C. The Device Under Test (DUT) is completely immersed in the fluid and initial stable conditions are recorded. P_d is then applied. Case temperature (T_C) is measured at the primary heat-flow path of the particular package. Junction temperature (T_J) is calculated from the diode forward-voltage drop from the initial stable condition before power was applied.

$$\Theta_{JC} = (T_J - T_C)/P_d$$

The junction-to-isothermal-fluid measurement (Θ_{JI}) is also calculated from the same data.

$$\Theta_{JL} = (T_J - T_l)/P_d$$

The latter data is considered as the ideal Θ_{JA} data for the package that can be obtained with the most efficient heat removal scheme. Other schemes such as airflow, heatsinks, use of copper clad board, or some combination of all these will tend towards this ideal figure. Since this is not a widely used parameter in the industry, and it is not very realistic for normal application of Xilinx packages, the Θ_{JI} data is not published. The thermal lab keeps such data for package comparisons.

Junction-to-Ambient Measurement — Θ_{JA}

Θ_{JA} is measured on FR4 based PC boards measuring 4.5” x 6.0” x .0625” (114.3mm x 152.4mm x 1.6mm) with edge connectors. There are two main board types.

Type I, 2L/0P board, is single layer with two signal planes (one on each surface) and no internal Power/GND planes. The trace density on this board is less than 10% per side. Type II, the 4L/2P board, has two internal copper planes (one power, one ground) and two signal trace layers on both surfaces.

Data may be taken with the package mounted in a socket or with the package mounted directly on the board. Socket measurements typically use the 2L/0P boards. SMT devices may use either board. Published data always reflects the board and mount conditions used.

Data is taken at the prevailing temperature and pressure conditions (22°C to 25°C ambient). The board with the DUT is mounted in a cylindrical enclosure. The power application and signal monitoring are the same as Θ_{JC} measurements. The enclosure (ambient) thermocouple is substituted for the fluid thermocouple and two extra thermocouples brought in to monitor room and board temperatures. The junction to ambient thermal resistance is calculated as follows:

$$\Theta_{JA} = (T_J - T_A)/P_d$$

The setup described herein lends itself to the application of various airflow velocities from 0-800 Linear feet per minute (LFM), i.e., 0-4.06 m/s. Since the board selection (copper trace density, absence or presence of ground planes, etc.) affects the results of the thermal resistance, the data from these tests shall always be qualified with the board mounting information.

Data Acquisition and Package Thermal Database

Xilinx gathers data for a package type in die sizes, power levels and cooling modes (air flow and sometimes heatsink effects) with a Data Acquisition and Control system (DAS). The DAS controls the power supplies and other ancillary equipment for hands-free data taking. Different setups within the DAS software are used to run calibration, Θ_{JA}, Θ_{JC}, fan tests, as well as the power effect characteristics of a package.

A package is characterized with respect to the major variables that influence the thermal resistance. The results are stored in a database. Thermal resistance data is interpolated as typical values for the individual Xilinx devices that are assembled in the characterized package. Table 4 shows the typical values for different packages. Specific device data may not be the same as the typical data. However, the data will fall within the given minimum and maximum ranges. The more widely used packages will have a wider range. Customers may contact the Xilinx application group for specific device data.

Table 4: **Summary of Thermal Resistance for Packages(1,2,3)**

Package Code	Θ_{JA} Still Air (Max)	Θ_{JA} Still Air (Typ)	Θ_{JA} Still Air (Min)	Θ_{JA} 250 LFM (Typ)	Θ_{JA} 500 LFM (Typ)	Θ_{JA} 750 LFM (Typ)	Θ_{JC} (Typ)	Comments
	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	
BG225	37	30	24	19	17	16	3.3	Various
BG256	32	29	24	19	17	16	3.2	4L/2P-SMT(4)
BG352	14	12	10	8	7	6	0.8	4L/2P-SMT(4)
BG432	13	11	9	8	6	6	0.8	4L/2P-SMT(4)
CG560	10	9	8	7	6	5	0.8	Estimated
CB100	44	41	38	25	19	17	5.1	Socketed
CB164	29	26	25	17	12	11	3.6	Socketed
CB196	25	24	24	15	11	10	1.8	Socketed
CB228	19	18	17	11	8	7	1.3	Socketed

Table 4: **Summary of Thermal Resistance for Packages(1,2,3) *(Continued)***

Package Code	Θ_{JA} Still Air (Max)	Θ_{JA} Still Air (Typ)	Θ_{JA} Still Air (Min)	Θ_{JA} 250 LFM (Typ)	Θ_{JA} 500 LFM (Typ)	Θ_{JA} 750 LFM (Typ)	Θ_{JC} (Typ)	Comments
	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	
DD8	114	109	97	90	73	60	8.2	Socketed
HQ160	14	14	14	10	8	7	1.0	4L/2P-SMT(4)
FG256	27	25	23	21	20	19	3.9	4L/2P-SMT(4)
FG456	19	18	17	14	13	13	1.5	4L/2P-SMT(4)
FG556	14	14	14	10	9	9	0.8	4L/2P-SMT(4)
FG676	17	17	17	13	12	12	0.9	4L/2P-SMT(4)
FG680	11	11	10	8	6	6	0.9	4L/2P-SMT(4)
FG860	10	10	10	7	6	5	0.8	4L/2P-SMT(4)
FG900	14	14	14	10	9	9	0.8	Estimated
FG1156	14	13	13	10	9	9	0.8	Estimated
HQ208	15	14	14	10	8	7	1.7	4L/2P-SMT(4)
HQ240	13	12	12	9	7	6	1.5	4L/2P-SMT(4)
HQ304	11	11	10	7	5	5	0.9	4L/2P-SMT(4)
PC20	86	84	76	63	56	53	25.8	2L/0P-SMT(5)
PC44	51	46	42	35	31	29	13.7	2L/0P-SMT(5)
PC68	46	42	38	31	28	26	9.3	2L/0P-SMT(5)
PC84	41	33	28	25	21	17	5.3	2L/0P-SMT(5)
PD8	82	79	73	60	54	50	22.2	Socketed
PG84	37	34	31	24	18	16	5.8	Socketed
PG120	32	27	25	19	15	13	3.6	Socketed
PG132	32	28	24	20	17	15	2.8	Socketed
PG156	25	23	21	15	11	10	2.6	Socketed
PG175	25	23	20	14	11	10	2.6	Socketed
PG191	24	21	18	15	12	11	1.5	Socketed
PG223	24	20	18	15	12	11	1.5	Socketed
PG299	18	17	16	10	9	8	1.9	Socketed
PG411	16	15	14	9	8	7	1.2	Socketed
PG475	14	13	12	9	8	7	1.2	Socketed
PG559	-	12.00	-	-	-	-	-	Estimated
PQ100	35	33	32	29	28	27	5.5	4L/2P-SMT(4)
PQ160	37	32	22	24	21	20	4.6	2L/0P-SMT(5)
PQ208	35	32	26	23	21	19	4.3	2L/0P-SMT(5)
PQ240	28	23	19	17	15	14	2.8	2L/0P-SMT(5)
SO8	147	147	147	112	105	98	48.3	IEEE-(Ref)

Notes:

1. Maximum, typical and minimum numbers are based on numbers for all the devices in the specific package at the time of compilation. The numbers do not necessarily reflect the absolute limits of that packages. Specific device data should lie within the limits. Packages used for a broader spectrum of devices have a wider range in the table. Specific device data in a package may be obtained from the factory.
2. Package configurations and drawings can be found on the Xilinx web site: **www.xilinx.com/partinfo/databook.htm**
3. Air flow is given Linear Feet per Minute (LFM). 500 LFM = 2.5 Meters per second.
4. 4L/2P-SMT: the data is from a 4-layer SMT board incorporating 2 internal planes. Socketed data is taken in socket.
5. 2L/0P-SMT: the data is from a surface mount Type I board—no internal planes on the board.

Application of Thermal Resistance Data

Thermal resistance data gauges the IC package thermal performance. Θ_{JC} measures the internal package resistance to heat conduction from the die surface, through the die mount material to the package exterior. Θ_{JC} strongly depends on the package's heat conductivity, architecture and geometrical considerations.

Θ_{JA} measures the total package thermal resistance including Θ_{JC}. Θ_{JA} depends on the package material properties and such external conditions as convective efficiency and board mount conditions. For example, a package mounted on a socket may have a Θ_{JA} value 20% higher than the same package mounted on a 4-layer board with power and ground planes.

By specifying a few constraints, devices are ensured to operate within the intended temperature range. This also ensures device reliability and functionality. The system ambient temperature needs to be specified. A maximum T_J also needs to be established for the system. The following inequality will hold.

$$T_J(max) > \Theta_{JA} * P_d + T_A$$

The following two examples illustrates the use of this inequality.

Example 1:

The manufacturer's goal is T_J (max) < 100°C

A module is designed for a T_A = 45°C max.

A XC3042 in a PLCC 84 has a Θ_{JA} = 32°C/watt.

Given a XC3042 with a logic design with a rated power P_d of 0.75watt.

With this information, the maximum die temperature can be calculated as:

$$T_J = 45 + (32 \times 0.75) \geq 69°C.$$

The system manufacturer's goal of T_J < 100°C is met.

Example 2:

A module has a T_A = 55°C max.

The Xilinx XC4013E is in a PQ240 package (HQ240 is also considered).

A XC4013E, in an example logic design, has a rated power of 2.50 watts. The module manufacturers goal is T_J (max.) < 100°C.

Table 5 shows the package and thermal enhancement combinations required to meet the goal of T_J < 100°C.

Table 5: **Thermal Resistance for XC4013E in PQ240 and HQ240 Packages**

Device Name	Package	Θ_{JA} Still Air	Θ_{JA} (250 LFM)	Θ_{JA} (500 LFM)	Θ_{JA} (750 LFM)	Θ_{JC}	Comments
XC4013E	PQ240	23.7	17.5	15.4	14.3	2.7	Cu, SMT 2L/0P
XC4013E	HQ240	12.5	8.6	6.9	6.2	1.5	4-layer board data

Notes:

1. Possible Solutions to meet the module requirements of 100°C :
2. Using the standard PQ240; $T_J = 55 + (23.7 \times 2.50) \geq 114.25°C$.
3. Using standard PQ240 with 250LFM forced air; $T_J = 55 + (17.5 \times 2.50) \geq 98.75°C$
4. Using standard HQ240, $T_J = 55 + (12.5 \times 2.50) \geq 86.25°C$
5. Using HQ240 with 250 LFM forced air; $T_J = 55 + (8.6 \times 2.50) \geq 76.5°C$

For all solutions, the junction temperature is calculated as: T_J = Power x Θ_{JA} + T_A. All solutions meet the module requirement of less than 100°C, with the exception of the PQ240 package in still air. In general, depending on ambient and board temperatures conditions, and most importantly the total power dissipation, thermal enhancements -- such as forced air cooling, heat sinking, etc. may be necessary to meet the T_J(max) conditions set.

Thermal Data Comparison Charts

The following charts (Figures 4, 5, 6, 7, and 8) are for reference only.

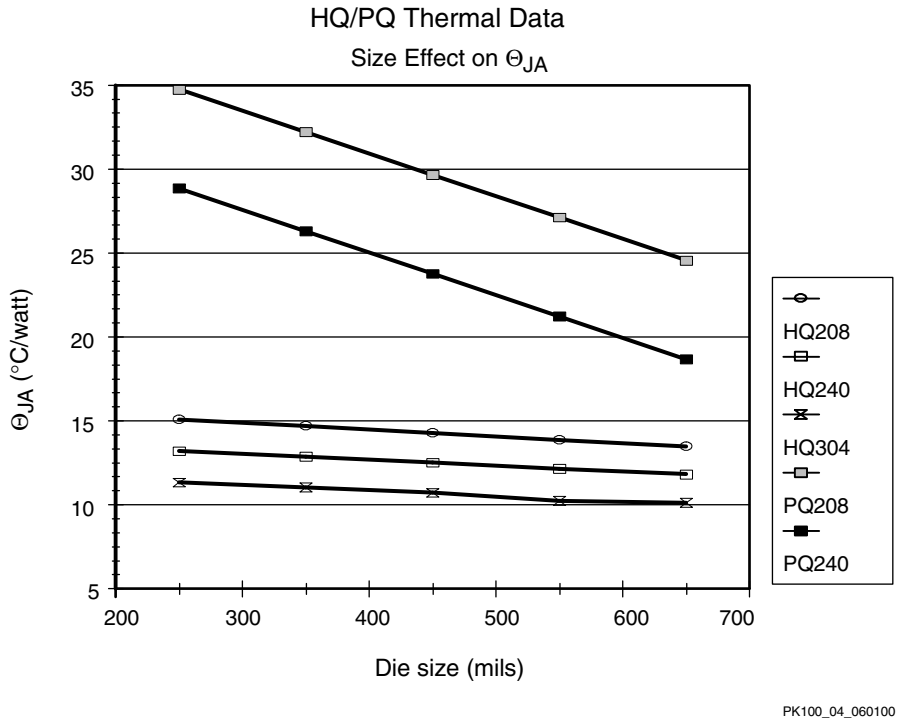


Figure 4: **HQ/PQ Thermal Data** (Size Effect on Θ_{JA})

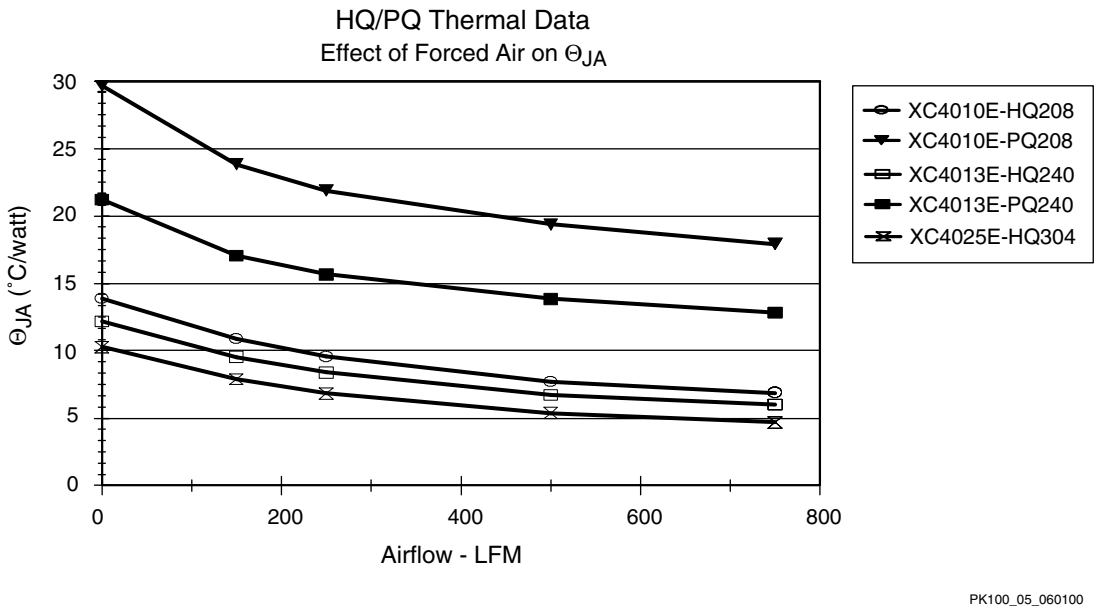


Figure 5: **HQ/PQ Thermal Data** (Effect of Forced Air on Θ_{JA})

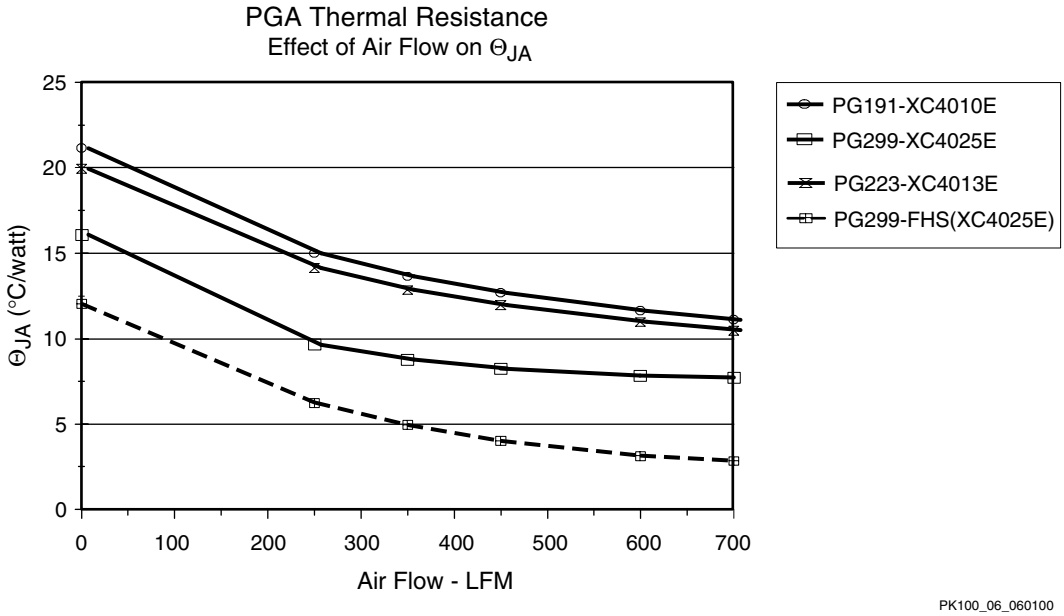


Figure 6: **PGA Thermal Data** (Effect of Air Flow on Θ_{JA})

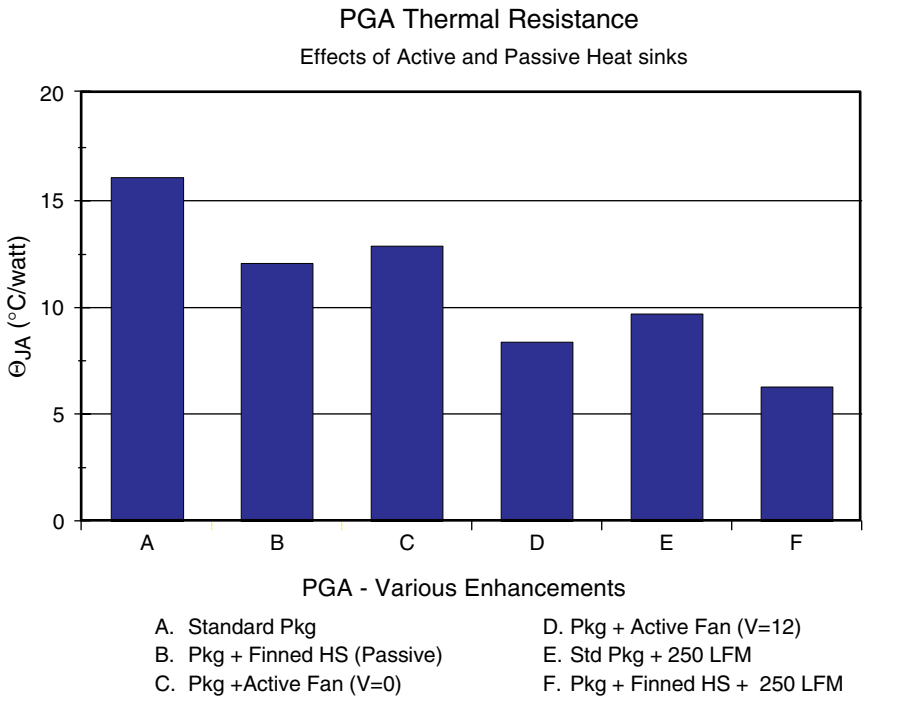


Figure 7: **PGA Thermal Data** (Effects of Active and Passive Heat Sinks)

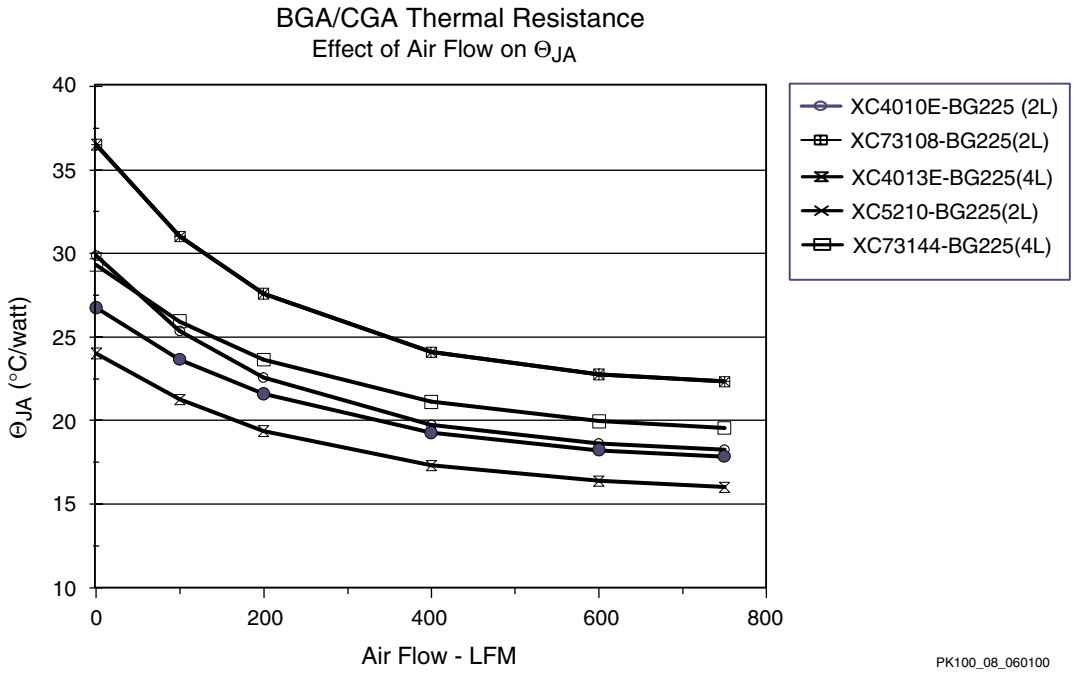


Figure 8: **BGA/CGA Thermal Data** (Effect of Air Flow on Θ_{JA})

Some Power Management Options

FPGA devices are usually not the dominating power consumers in a system, and do not have a big impact on power supply designs. There are obvious exceptions. When the actual or estimated power dissipation appears to be more than the specification of the chosen package, some options can be considered. Details on the engineering designs and analysis of some of these suggested considerations may be obtained from the references listed at the end of the section. The options include:

- Explore thermally enhanced package options available for the same device. As illustrated above, the HQ240 package has a thermal impedance of about 50% of the equivalent PQ240. Besides, the 240 lead, the 208 lead and the 304 lead Quad packages have equivalent heatsink enhanced versions. Typically 25% to 40% improvement in thermal performance can be expected from these heatsink enhanced packages. Most of the high gate count devices above the XC4013 level come either exclusively in heat enhanced packages or have these packages as options. If the use of a standard PQ appears to be a handicap in this respect, a move to the equivalent HQ package if available may resolve the issue. The heat enhanced packages are pin to pin compatible and they use the same board layout.
- The use of forced air is an effective way to improve thermal performance. As seen on the graphs and the calculations above, forced air (200-300 LFM) can reduce junction to ambient thermal resistance by 30%.
- If space will allow, the use of finned external heatsinks can be effective. If implemented with forced air as well, the benefit can be a 40% to 50% reduction. The HQ304, all cavity down PGAs, and the BG352 with exposed heatsink lend themselves to the application of external heatsinks for further heat removal efficiency.
- Outside the package itself, the board on which the package sits can have a significant impact. Board designs may be implemented to take advantage of this. Heat flows to the outside of a board mounted package and is sunk into the board to radiate. The effect of the board will be dependent on the size and how it conducts heat. Board size, the level of copper traces on it, the number of buried copper planes all lower the junction-to-ambient thermal resistance for a package. Some of the heatsink packages with the exposed heatsink on the board side can be glued to the board with thermal compound to enhance heat removal.

References

Forced Air Cooling Application Engineering

COMAIR ROTRON
2675 Custom House Court
San Ysidro, CA 92173
1-619-661-6688

Heatsink Application Engineering

The following facilities provide heatsink solutions for industry standard packages.

AAVID Thermal Technologies
1 Kool Path
Box 400
Laconia, NH 03247-0400
1-603-528-3400

Thermalloy, Inc.
2021 W. Valley View Lane
Box 810839
Dallas, TX 75381-0839
1-214-243-4321

Wakefield Engineering, Inc.
60 Audubon Road
Wakefield MA 01880-1255
1-617-245-5900

Xilinx does not endorse these vendors nor their products. They are listed here for reference only. Any materials or services received from the vendors should be evaluated for compatibility with Xilinx components.

Package Electrical Characterization

In high-speed systems, the effects of electrical package parasitics become very critical when optimizing for system performance. Such problems as ground bounce and crosstalk can occur due to the inductance, capacitance, and resistance of package interconnects. In digital systems, such phenomena can cause logic error, delay, and reduced system speed. A solid understanding and proper usage of package characterization data during system design simulation can help prevent such problems.

Theoretical Background

There are three major electrical parameters which are used to describe the package performance: resistance, capacitance, and inductance. Also known as interconnect parasitics, they can cause many serious problems in digital systems. For example, a large resistance can cause RC & RL off-chip delays, power dissipation, and edge-rate degradation. Large capacitance can cause RC delays, crosstalk, edge-rate degradation, and signal distortion. The lead inductance, perhaps the most damaging parasitic in digital circuitry, can cause such problems as ground bounce (also known as simultaneous switching noise or delta-I noise), RL delays, crosstalk, edge rate degradation, and signal distortion.

Ground bounce is the voltage difference between any two grounds (typically between an IC and circuit board ground) induced by simultaneously switching current through bondwire, lead, or other interconnect inductance.

When IC outputs change state, large current spikes result from charging or discharging the load capacitance. The larger the load capacitance and faster the rise/fall times, the larger the current spikes are: $I = C * dv/dt$. Current spikes through the IC pin and bondwire induces a voltage drop across the leads and bondwires: $V = L * di/dt$. The result is a momentary voltage difference between the internal IC ground and system ground, which show up as voltage spikes and unswitched outputs.

Factors that affect ground bounce:

- rise and fall times
- load capacitance
- package inductance
- number of output drivers sharing the same ground path
- device type

Analytical Formulas for Lead Inductance

1. Rectangular Leadframe/Trace (straight)

$$L_{self} = 5l\left[\ln\left(\frac{2l}{w+t}\right)+\frac{1}{2}\right] \text{ nH}$$

(no ground)

$$L_{self} = 5l\left[\ln\left(\frac{8h}{w+t}\right)+\left(\frac{w+t}{4h}\right)\right] \text{ nH}$$

(above ground)

where:

l = lead/trace length

w = lead/trace width

t = lead/trace thickness

h = ground height

unit = inches

2. Bondwire (gold wire)

$$L_{wire} = 5l\left[\ln\left(\frac{2l}{r}\right)-\frac{3}{4}\right] \text{ nH}$$

where:

L = wire length

r = wire radius

unit = inches

General Measurement Procedure

Xilinx uses the Time-Domain Reflectometry (TDR) method for parasitic inductance and capacitance measurements. The main components of a TDR setup includes: a digitizing sampling oscilloscope, a fast rise time step generator (<17 ps), a device-under-test (DUT) interface, and an impedance-profile analysis software to extract parasitic models from the TDR reflection waveforms. In this method, a voltage step is propagated down the package under test, and the incident and reflected voltage waves are monitored by the oscilloscope at a particular point on the line. The resulting characteristic impedance of the package interconnect shows the nature (resistive, inductive, and capacitive) of each discontinuity.

Package and Fixture Preparation

Before performing the measurements, the package and the DUT interface must be fixtured. Proper fixturing ensures accurate and repeatable measurements. The mechanical sample for all inductance (self and mutual) measurements are finished units with all leads shorted to the internal ground. For packages without an internal ground (i.e., QFP, PLCC, etc.) the die-paddle is used instead. The mechanical sample for all capacitance (self & mutual) measurements are finished units with all internal leads floating. The DUT interface provides a physical connection between the oscilloscope and the DUT with minimum crosstalk and probe/DUT reflection. It also provides small ground loop to minimize ground inductance of the fixture.

Inductance and Capacitance Measurement Procedure

For inductance measurements, a minimum of 25% and maximum of 50% of packages leads, including all leads that are adjacent to the lead(s) under test, are insulated from the DUT fixture ground. All other leads, except for the lead(s) under test, are grounded. This insulation forces the current to return through a low impedance path created on the opposite side of the package. It also eliminates mutual coupling from the neighboring leads. Self-inductance is measured by sending a fast risetime step waveform through the lead under test. The inductive reflection waveform through the lead and the bondwire is then obtained. This reflection waveform, which includes the inductance of the die-paddle (for QFP and PLCC-type packages) and parallel combination of leads in the return path, is the self-inductance. The parasitic effects of the return path are small enough to ignore in the context of this method. For mutual-inductance measurement, two adjacent leads are probed. A fast risetime step waveform is sent through one of the leads. The current travels through the lead/bondwire and returns by the path of the low-impedance ground. On the adjacent “quiet” lead, a waveform is induced due to mutual coupling. This waveform is measured as the mutual inductance.

For capacitance measurements, all external leads except for the lead(s) under test are grounded to the DUT fixture. For QFP, PLCC, and Power Quad-type of packages, the die-paddle and the heat slug are left floating. Self-capacitance is measured by sending a fast risetime step waveform through the lead under test. The reflection waveform from the lead, which includes the sum of all capacitive coupling with respect to the lead under test, is then measured. Appropriately, the self-capacitance can also be called the “bulk” capacitance since the measured value includes the capacitance between the lead under test and all surrounding metal, including the ground plane and the heat slug. For mutual-capacitance measurement, two adjacent leads are probed. An incident waveform is sent through one lead, and the induced waveform on the neighboring lead is measured as the mutual capacitance.

In order to de-embed the electrical parasitics of the DUT fixture and the measuring probes, the short and the open compensation waveforms are also measured after each package measurement. This procedure compensates the DUT fixture to the very tip of the probes.

Inductance and Capacitance Model Extraction

All measured reflection waveforms are downloaded to a PC running the analysis software for package parasitic model extraction. The software uses a method called the Z-profile algorithm, or the impedance-profile algorithm, for parasitic analysis. This method translates the downloaded reflection waveforms into true impedance waveforms, from which package models for inductance and capacitance are extracted.

Data Acquisition and Package Electrical Database

Xilinx acquires electrical parasitic data only on the longest and the shortest lead/traces of the package. This provides the best and the worst case for each package type (defined by package design, lead/ball count, pad size, and vendor). For convenience, the corner interconnects are usually selected as the longest interconnect, while the center interconnects are usually selected as the shortest.

For symmetrical quad packages, all four sides of the package are measured and averaged. Three to five samples are usually measured for accuracy and continuity purposes. The average of these samples is then kept as the official measured parasitic data of that package type in the database.

Component Mass (Weight) by Package Type

Table 6: **Component Mass (Weight) by Package Type(1,2)**

Package	Description	JEDEC Outline #	Xilinx #	Mass (g)
BG225	Molded BGA 27 mm Full Matrix	MO-151-CAL	OBG0001	2.2
BG256	Molded BGA 27 mm SQ	MO-151-CAL	OBG0011	2.2
BG352	Super BGA: 35 x 35 mm Peripheral	MO-151-BAR	OBG0008	7.1
BG432	Super BGA:- 40 x 40 mm Peripheral	MO-151-BAU	OBG0009	9.1
BG560	Super BGA: 42.5 x 42.5 mm SQ	MO-192-BAV	OBG0010	11.5
CG560	Super BGA: 42.5 x 42.5 mm SQ	MO-192-BAV	OBG0010	11.5
CB100	NCTB Top Braze 3K Version	MO-113-AD(3)	OCQ0008	10.8
CB100	NCTB Top Braze 4K Version	MO-113-AD(3)	OCQ0006	10.8
CB164	NCTB Top Braze 3K Version	MO-113-AA-AD(3)	OCQ0003	11.5
CB164	NCTB Top Braze 4K Version	MO-113-AA-AD(3)	OCQ0007	11.5
CB196	NCTB Top Braze 4K Version	MO-113-AB-AD(3)	OCQ0005	15.3
CB228	NCTB Top Braze 4K Version	MO-113-AD(3)	OCQ0012	17.6
DD8	0.300 CERDIP Package	MO-036-AA	OPD0005	1.1
HQ160	Metric 28 28 -.65 mm 1.6H/S Die Up	MO-108-DDI	OPQ0021	10.8
HQ208	Metric 28 x 28 - H/S Die Up	MO-143-FA1	OPQ0020	10.8
HQ240	Metric QFP 32 32 - H/S Die Up	MO-143-GA	OPQ0019	15.0
HQ304	Metric QFP 40 40-H/S die Down	MO-143-JA	OPQ0014	26.2
PC20	PLCC JEDEC MO-047	MO-047-AA	OPC0006	0.8
PC44	PLCC JEDEC MO-047	MO-047-AC	OPC0005	1.2
PC68	PLCC JEDEC MO-047	MO-047-AE	OPC0001	4.8
PC84	PLCC JEDEC MO-047	MO-047-AF	OPC0001	6.8
PD8	DIP 0.300 Standard	MO-001-AA	OPD0002	0.5
PG84	Ceramic PGA CAV UP 11 x 11	MO-067-AC	OPG0003	7.2
PG120	Ceramic PGA 13 x 13 Matrix	MO-067-AE	OPG0012	11.5
PG132	Ceramic PGA 14 x 14 Matrix	MO-067-AF	OPG0004	11.8
PG156	Ceramic PGA 16 x 16 Matrix	MO-067-AH	OPG0007	17.1
PG175	Ceramic PGA 16 x 16 STD VER.	MO-067-AH	OPG0009	17.7
PG191	Ceramic PGA 18 x 18 STD - ALL	MO-067-AK	OPG0008	21.8
PG223	Ceramic PGA 18 x 18 Type	MO-067-AK	OPG0016	26.0
PG299	Ceramic PGA 20 x 20 Heatsink	MO-067-AK	OPG0022	37.5
PG299	Ceramic PGA 20 x 20 Type	MO-067-AK	OPG0015	29.8
PG411	Ceramic PGA 39 x 39 Stagger	MO-128-AM	OPG0019	36.7

Table 6: **Component Mass (Weight) by Package Type(1,2) *(Continued)***

Package	Description	JEDEC Outline #	Xilinx #	Mass (g)
PG475	Ceramic PGA 41 x 41 Stagger	MO-128-AM	OPG0023	39.5
PG559	Ceramic PGA 43 x 43	MO-128	OPG0025	44.50
PQ100	EIAJ 14 x 20 QFP - 1.60	MO-108-CC1	OPQ0013	1.6
PQ160	EIAJ 28 x 28 .65 mm 1.60	MO-108-DD1	OPQ0002	5.8
PQ208	EIAJ 28 x 28 .5 mm 1.30	MO-143-FAI	OPQ0003	5.3
PQ240	EIAJ 32 x 32 .5 mm	MO-143-GA	OPQ0010	7.1
SO8	Version: 0.150/55 mil	MO-150	OPD0006	0.1
FG256	Fine Pitch BGA 17 x 17 mm, 1.0 mm ball pitch	MO-151-AAF-1	OBG0021	0.8
FG456	Fine PItch BGA 23 x 23 mm, 1.0 mm ball pitch	MO-151-AAJ-1	OBG0019	2.1
FG556	Fine Pitch BGA 31 x 31 mm, 1.0 mm ball pitch	MO-151-AAN-1	OBG0020	3.92
FG676	Fine PItch BGA, 27 x 27 mm, 1.0 mm ball pitch	MO-151-AAL-1	OBG0018	3.3
FG680	Fine PItch BGA 40 x 40 mm, 1.0 mm ball pitch	MO-151-AAU-1	OBG0022	10.3
FG900	Fine Pitch BGA, 31 x 31 mm, 1.0 mm ball pitch	MO-151-AAN-1	OBG0027	4.0
FG1156	Fine Pitch BGA, 35 x 35 mm, 1.0 mm ball pitch	MO-151-AAR-1	OBG0028	5.5

Notes:

1. Data represents average values for typical packages with typical devices. The accuracy is between 7% to 10%.
2. More precise numbers (below 5% accuracy) for specific devices may be obtained from Xilinx through a factory representative or by calling the Xilinx Hotline.
3. Tie-bar details are specific to Xilinx package. Lead width minimum is 0.056”.

Xilinx Thermally Enhanced Packaging

The Package Offering

Xilinx Code	Body (mm)	THK (mm)	Mass (gm)	Heatsink Location	JEDEC No.	Xilinx No.
HQ160	28x28	3.40	10.8	DOWN	MO-108-DD1	OPQ0021
HQ208	28x28	3.40	10.0	DOWN	MO-143-FA	OPQ0020
HQ240	32x32	3.40	15.0	DOWN	MO-143-GA	OPQ0019
HQ304	40x40	3.80	26.2	TOP	MO-143-JA	OPQ0014

Overview

Xilinx offers thermally enhanced quad flat pack packages on certain devices. This section discusses the performance and usage of these packages (designated HQ). In summary:

- The HQ-series and the regular PQ packages conform to the same JEDEC drawings.
- The HQ and PQ packages use the same PCB land patterns.
- The HQ packages have more mass
- Thermal performance is better for the HQ packages

Where and When Offered

- HQ packages are offered as the thermally enhanced equivalents of PQ packages. They are used for high gate count or high I/O count devices in packages, where heat dissipation without the enhancement may be a handicap for device performance. Such devices include XC4013E, XC4020E, XC4025E, and XC5215.
- They are also being used in place of MQUAD (MQ) packages of the same lead count for new devices.
- The HQ series at the 240-pin count level or below are offered with the heatsink at the bottom of the package (Figure 9). This was done to ensure pin to pin compatibility with the existing PQ and MQ packages.
- At the 304-pin count level, the HQ is offered with the heatsink up (Figure 9). This arrangement offers a better potential for further thermal enhancement by the designer.

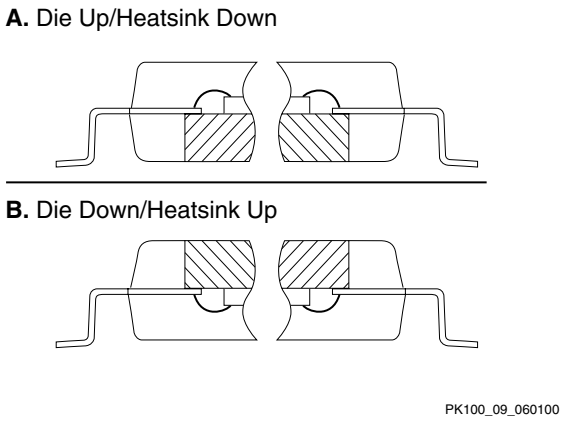


Figure 9: **Heatsink Orientation Diagram**

Mass Comparison

Because of the copper heatsink, the HQ series of packages are about twice as heavy as the equivalent PQ. Here is a quick comparison.

Table 7: **HQ vs. PQ Comparison**

	HQ (gm)	PQ (gm)
160-pin	10.8	5.8
208-pin	10.8	5.3
240-pin	15.0	7.1
304-pin	26.2	N/A

Thermal Data for the HQ

The data for individual devices may be obtained from Xilinx.

Table 8: **Still Air Data Comparison**

	HQ Θ_{JA} (°C/Watt)(1)	PQ Θ_{JA} (°C/watt)(1)
160-pin	13.5-14.5	20.5-38.5
208-pin	14-15	26-35
240-pin	12-13	19-28
304-pin	10-11	N/A

Notes:

1. Θ_{JC} is typically between 1°C/Watt and 2°C/Watt for HQ and MQ Packages. For PQs, it is between 2°C/Watt and 7 °C/Watt.

Table 9: **Data Comparison at Airflow - 250 LFM**

	HQ Θ_{JA} (°C/watt)	PQ Θ_{JA} (°C/watt)
160-pin	9-10	15-28.5
208-pin	9-10	14-26
240-pin	8-9	11-21
304-pin	6.5-8	N/A

Other Information

- Leadframe: Copper EFTEC-64 or C7025
- Heat Slug: Copper - Nickel plated → Heatsink metal is grounded
- Lead Finish 85/15 Sn/Pb 300 microinches minimum
- D/A material - Same as PQ; Epoxy 84-1LMISR4
- Mold Cpd. Same as PQ - EME7304LC
- Packed in the same JEDEC trays

Moisture Sensitivity of PSMCs

Moisture Induced Cracking During Solder Reflow

The surface mount reflow processing step subjects the Plastic Surface Mount Components (PSMC) to high thermal exposure and chemicals from solder fluxes and cleaning fluids during user's board mount assembly. The plastic mold compounds used for device encapsulation are, universally, hygroscopic and absorb moisture at a level determined by storage environment and other factors. Entrapped moisture can vaporize during rapid heating in the solder reflow process generating internal hydrostatic pressure. Additional stress is added due to thermal mismatch, and the Thermal Coefficient of Expansion (TCE) of plastic, metal lead frame, and silicon die. The resultant pressure may be sufficient to cause delamination within the package, or worse, an internal or external crack in the plastic package. Cracks in the plastic package can allow high moisture penetration, inducing transport of ionic contaminants to the die surface and increasing the potential for early device failure.

How the effects of moisture in plastic packages and the critical moisture content result in package damage or failure is a complex function of several variables. Among them are package construction details—materials, design, geometry, die size, encapsulant thickness,

encapsulant properties, TCE, and the amount of moisture absorbed. The PSMC moisture sensitivity has, in addition to package cracking, been identified as a contributor to delamination-related package failure artifacts. These package failure artifacts include bond lifting and breaking, wire neckdown, bond cratering, die passivation, and metal breakage.

Because of the importance of the PSMC moisture sensitivity, both device suppliers and device users have ownership and responsibility. The background for present conditions, moisture sensitivity standardized test and handling procedures have been published by two national organizations. Users and suppliers are urged to obtain copies of both documents (listed below) and use them rigorously. Xilinx adheres to both.

- JEDEC STANDARD JESD22-A112.
  Test Method A112 “Moisture-Induced Stress Sensitivity for Plastic Surface Mounted Devices”. Available through Global Engineering Documents
  Phone: USA and Canada 800-854-7179, International 1-303-792-2181
- IPC Standard IPC-SM-786A “Procedures for Characterizing and Handling of Moisture/Reflow Sensitive ICs”. Available through IPC
  Phone: 1-708-677-2850

None of the previously stated or following recommendations apply to parts in a socketed application. For board mounted parts careful handling by the supplier and the user is vital. Each of the above publications has addressed the sensitivity issue and has established 6 levels of sensitivity (based on the variables identified). A replication of those listings, including the preconditioning and test requirements, and the factory floor life conditions for each level are outlined in Table 10. Xilinx devices are characterized to their proper level as listed. This information is conveyed to the user via special labeling on the Moisture Barrier Bag (MBB).

In Table 10, the level number is entered on the MBB prior to shipment. This establishes the user’s factory floor life conditions as listed in the time column. The soak requirement is the test limit used by Xilinx to determine the level number. This time includes manufacturer’s exposure time or the time it will take for Xilinx to bag the product after baking.

Table 10: **Package Moisture Sensitivity Levels per J-STD-020**

Level	Factory Floor Life		Soak Requirements (Preconditioning)			
	Conditions	Time	Time			Conditions
1	≤30°C / 90% RH	Unlimited	168 hours			85°C / 85% RH
2	≤30°C / 60% RH	1 year	168 hours			85°C / 60% RH
			Time (hours)			
			X +(1)	Y =(2)	Z(3)	
3	≤30°C / 60% RH	168 hours	24	168	192	30°C / 60% RH
4	≤30°C / 60% RH	72 hours	24	72	96	30°C / 60% RH
5	≤30°C / 60% RH	24/28 hours	24	24/48	48/72	30°C / 60% RH
6	≤30°C / 60% RH	6 hours	0	6	6	30°C / 60% RH

Notes:

1. X = Default value of semiconductor manufacturer’s time between bake and bag. If the semiconductor manufacturer’s actual time between bake and bag is different from the default value, use the actual time.
2. Y = Floor life of package after it is removed from dry pack bag.
3. Z = Total soak time for evaluation.

Factory Floor Life

Factory floor life conditions for Xilinx devices are clearly stated on MBB containing moisture sensitive PSMCs. These conditions have been ascertained by following Test Methods outlined in JEDEC JESD22-A112 and are replicated in Table 10. If factory floor conditions are outside the stated environmental conditions (30°C/90% RH for level 1, and 30°C/60% RH for Levels 2-6) or if time limits have been exceeded, then recovery can be achieved by baking the devices before the reflow step. Identified in the next section are two acceptable bake schedules. Either can be used for recovery to the required factory floor level.

Dry Bake Recommendation and Dry Bag Policy

Xilinx recommends, as do the mentioned publications and other industry studies, that all moisture sensitive PSMCs be baked prior to use in surface mount applications, or comply strictly with requirements as specified on the MBB. Tape and Reeled parts are universally dry packed. Level 1 parts are shipped without the need for, or use of, an MBB.

Two bake schedules have been identified as acceptable and equivalent. The first is 24 hours in air at 125°C, in shipping media capable of handling that temperature. The second bake schedule is for 192 hours in a controlled atmosphere of 40°C, equal to or less than 5% RH.

Dry Devices are sealed in special military specification Moisture Barrier Bags (MBB). Enough desiccant pouches are enclosed in the MBB to maintain contents at less than 20% RH for up to 12 months from the date of seal. A reversible Humidity Indicator Card (HIC) is enclosed to monitor the internal humidity level. The loaded bag is then sealed shut under a partial vacuum with an impulse heat sealer.

Artwork on the bags provides storage, handling and use information. There are areas to mark the seal date, quantity, and moisture sensitivity level and other information. The following paragraphs contain additional information on handling PSMCs.

Handling Parts in Sealed Bags

Inspection

Note the seal date and all other printed or hand entered notations. Review the content information against what was ordered. Thoroughly inspect for holes, tears, or punctures that may expose contents. Xilinx strongly recommends that the MBB remain closed until it reaches the actual work station where the parts will be removed from the factory shipping form.

Storage

The sealed MBB should be stored, unopened, in an environment of not more than 90% RH and 40°C. The enclosed HIC is the only verification to show if the parts have been exposed to moisture. Nothing in part appearance can verify moisture levels.

Expiration Date

The seal date is indicated on the MBB. The expiration date is 12 months from the seal date. If the expiration date has been exceeded or HIC shows exposure beyond 20% upon opening the bag bake the devices per the earlier stated bake schedules. The three following options apply after baking:

1. Use the devices within time limits stated on the MBB.
2. Reseal the parts completely under a partial vacuum with an impulse sealer (hot bar sealer) in an approved MBB within 12 hours, using fresh desiccant and HIC, and label accordingly. Partial closures using staples, plastic tape, or cloth tape are unacceptable.
3. Store the out-of-bag devices in a controlled atmosphere at less than 20% RH. A desiccator cabinet with controlled dry air or dry nitrogen is ideal.

Other Conditions

Open the MBB when parts are to be used. Open the bag by cutting across the top as close to the seal as possible. This provides room for possible resealing and adhering to the reseal conditions outlined above. After opening, strictly adhere to factory floor life conditions to ensure that devices are maintained below critical moisture levels.

Bags opened for less than one hour (strongly dependent on environment) may be resealed with the original desiccant. If the bag is not resealed immediately, new desiccant or the old one that has been dried out may be used to reseal, **if the factory floor life has not been exceeded**. Note that factory floor life is cumulative. Any period of time when MBB is opened must be added to all other opened periods.

Both the desiccant pouches and the HIC are reversible. Restoration to dry condition is accomplished by baking at 125°C for 10-16 hours, depending on oven loading conditions.

Reflow Soldering Process Guidelines

To implement and control the production of surface mount assemblies, the dynamics of the solder reflow process and how each element of the process is related to the end result must be thoroughly understood.

The primary phases of the reflow process are as follows:

1. Melting the particles in the solder paste
2. Wetting the surfaces to be joined
3. Solidifying the solder into a strong metallurgical bond

The sequence of five actions that occur during this process is shown in Figure 10.

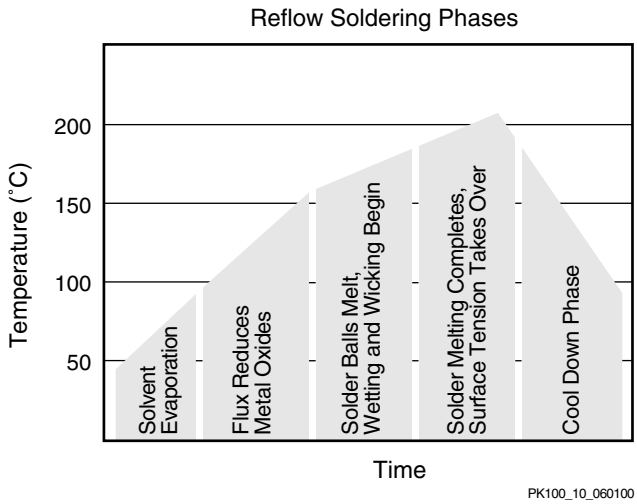


Figure 10: **Soldering Sequence**

Each phase of a surface mount reflow profile has min/max limits that should be viewed as a process window. The process requires a careful selection and control of the materials, geometries of the mating surfaces (package footprint vs. PCB land pattern geometries) and the time temperature of the profile. If all of the factors of the process are sufficiently optimized, there will be good solder wetting and fillet formation (between component leads and the land

patterns on the substrate). If factors are not matched and optimized there can be potential problems as summarized in Figure 11.

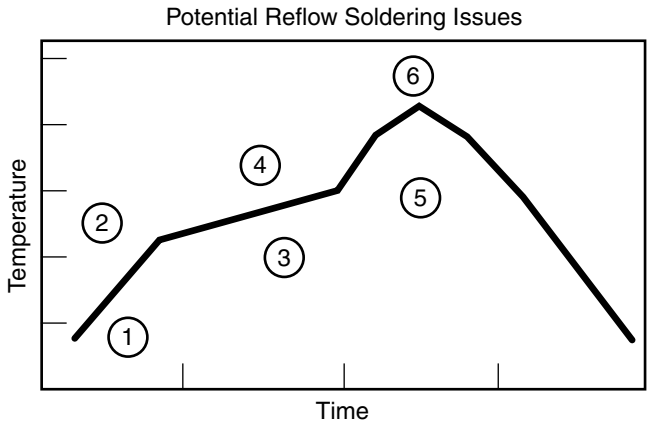


Figure 11: **Soldering Problems Summary**

Figure 12 and Figure 13 show typical conditions for solder reflow processing using IR/Convection or Vapor Phase. Both IR and Convection furnaces are used for BGA assembly. The moisture sensitivity of Plastic Surface Mount Components (PSMCs) must be verified prior to surface mount flow. See the preceding sections for a more complete discussion on PSMC moisture sensitivity.

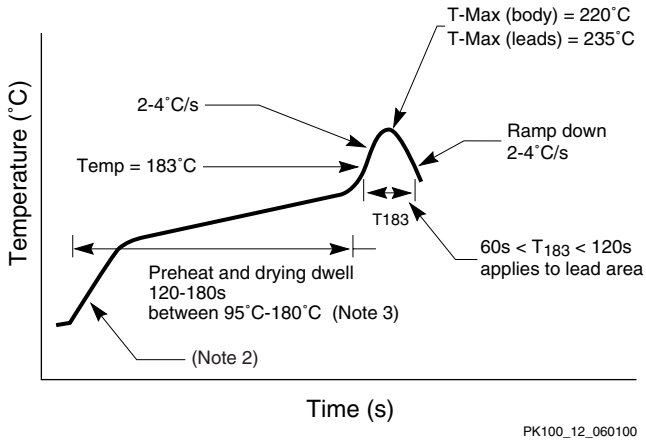


Figure 12: **Typical Conditions for IR Reflow Soldering**

Notes:

1. Max temperature range = 220°C-235°C (leads). Time at temp 30-60 seconds
2. Preheat drying transition rate 2-4°C/s
3. Preheat dwell 95-180°C for 120-180 seconds
4. IR reflow shall be performed on dry packages

   The IR process is strongly dependent on equipment and loading differences. Components may overheat due to lack of thermal constraints. Unbalanced loading may lead to significant temperature variation on the board. This guideline is intended to assist users in avoiding damage to the components; the actual profile should be determined by the users using these guidelines.

The peak reflow temperature of the PSMC body should not be more than 220°C in order to avoid internal package delamination. For multiple BGAs in a single board, it is recommended to check all BGA sites for varying temperatures because of differences in surrounding components.

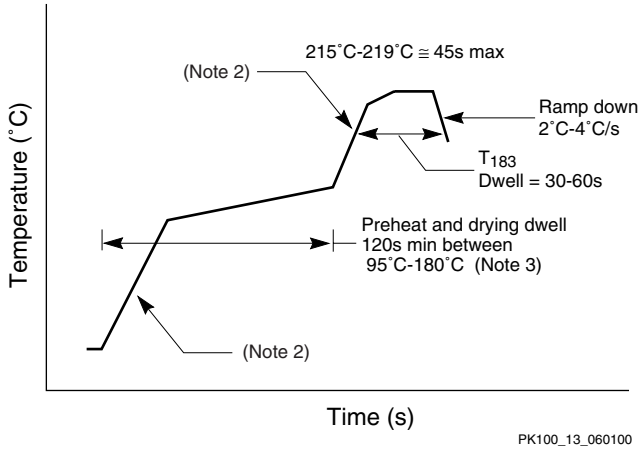


Figure 13: **Typical Conditions for Vapor Phase Reflow Soldering**

Notes:

1. Solvent - FC5312 or equivalent - ensures temperature range of leads at 215-219°C
2. Transition rate 4-5°C/s
3. Dwell is intended for partial dryout and reduces the difference in temperature between leads and PCB land patterns.
4. These guidelines are for reference. They are based on laboratory runs using dry packages. It is recommended that actual packages with known loads be checked with the commercial equipment prior to mass production.

Sockets

Table 11 lists manufacturers known to offer sockets for Xilinx Package types. This summary does not imply an endorsement by Xilinx. Each user has the responsibility to evaluate and approve a particular socket manufacturer.

Table 11: **Socket Manufacturers**

Manufacturer	Packages					
	DIP SO VO	PC WC	PQ HQ TQ VQ	PG PP	CB	BG CG
AMP Inc. 470 Friendship Road Harrisburg, PA 17105-3608 (800) 522-6752	X	X		X		
Augat Inc. 452 John Dietsch Blvd. P.O. Box 2510 Attleboro Falls, MA 02763-2510 (508) 699-7646	X	X		X		
McKenzie Socket Division 910 Page Avenue Fremont, CA 94538 (510) 651-2700	X	X		X		
3M Textool 6801 River Place Blvd. (800) 328-0411 (612) 736-7167				X	X	X
Wells Electronics 1701 South Main Street South Bend, IN 46613-2299 (219) 287-5941				X		
Yamaichi Electronics Inc. 2235 Zanker Road San Jose, CA 95131 (408) 456-0797		X	X	X	X	

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/15/00	1.0	Initial Xilinx release.

High-Reliability Package Drawings

Package Drawings

Package drawings are located on the High-reliability CD-ROM enclosed with this data book, or on the Xilinx web site: www.xilinx.com/partinfo/pkgs.htm

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For the nearest Xilinx Sales Office nearest you,

refer to the Xilinx web site:

http://www.xilinx.com/company/sales/offices.htm

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1-800-255-7778