XAPP370 (v1.0) January 3, 2002

Handheld Bicycle Computer (Cool Trak)

Summary

This document describes the implementation of Cool Trak, the grand prize winning design submission in the recently publicized "Cool Module Design Contest". All development for this contest was performed using the Insight Springboard™ development platform which allows for rapid development of Handspring modules. This development platform incorporates the reprogrammable Xilinx CoolRunner™ XPLA3 CPLD and uses the Handspring Visor™ PDA expansion slot. Low power CoolRunner CPLDs are the ideal programmable logic solution for portable, handheld applications.

The Cool Trak module for Handspring Personal Digital Assistants functions as an advanced cycling computer, providing not only time, speed, and distance measurements, but also pedal cadence, air temperature, humidity and heart rate statistics (Figure 1). The CPLD and Handspring design files for Cool Trak are available and can be found at **Download Pack**, page 10.

Figure 1: **Cool Trak Design Submission**

A visual presentation of the Cool Trak submission is provided to show operation and functionality. This on demand video is available on the Xilinx website at: **http://www.xilinx.com/apps/video.htm**

Introduction

In January of 2001, Xilinx, Handspring and Portable Design Magazine announced the "Cool Module Design Contest," a design contest that highlights the use of Xilinx CoolRunner XPLA3 CPLDs to quickly develop Springboard modules for the Handspring Visor PDA. About 250 contest registrations were received and nearly 100 contest design ideas were submitted. From these submissions, ten were chosen to receive a Handspring Visor and an Insight Springboard development kit. These ten finalists were given three months to complete their designs in order to compete for a "winner takes all" grand prize of $10,000. All finalists were required to include a written description of the project, all design files, and the necessary software to make their Springboard module prototypes operate. All the finalists did a great job. This application note is derived from the grand prize winning submission supplied by the Frog Design Team (Preston Brown, Henri Cao, Mikal Greaves, Eric Freedman, and Greg Wilson). Figure 2 below shows the Cool Module Design Contest judges posing with the winning design (from left to right: Jeff Hawkins (CPO, Handspring), Bill Carter (CTO, Xilinx), Richard Nass (Editor, Portable Design Magazine)).

Figure 2: **Cool Module Design Contest Judges and Cool Trak**

Appendix A outlines existing Xilinx application notes that are appropriate for understanding this application note. These are available on the Xilinx website at: **http://www.xilinx.com/**.

Design Description

The Cool Trak Springboard module allows any Handspring Visor PDA to function as an advanced cycling computer. It is a cycling enthusiast's dream come true — a computer that measures critical performance data for the duration of a bike ride. Cool Trak has the ability to measure time, speed, distance, pedal cadence, air temperature, barometric pressure, humidity and heart rate data. In addition to providing information to the rider, the Cool Trak is also a data recorder, which logs all of the above parameters throughout the duration of the journey for later analysis. The entire unit is designed to mount directly onto a pre-designed frame which in turn is mounted on the handlebars of a bicycle. This is shown in Figure 3. Cool Trak is designed for recreational cyclists with their eye on fitness, as well as for competitive or professional riders looking to achieve maximum performance.

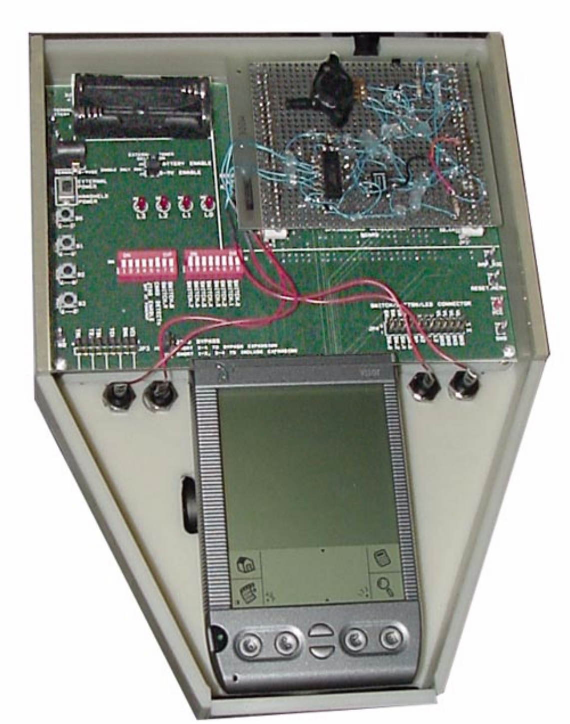

Figure 3: **Cool Trak Springboard Module**

System Design Overview

Because of Cool Trak's wide range of functions, a multitude of sensors are required. A Xilinx XPLA3 CoolRunner CPLD is used to allow all of these sensors to communicate with the Visor PDA. Some sensors are directly connected to the CoolRunner device (neglecting some signal conditioning). Other sensors require a TI ADS7870 Data Acquisition System to convert the analog output signal to a digital one that the CoolRunner CPLD can read. The CoolRunner device's patented combination of ultra low power, high speed, and 100% routability allow the Cool Trak design to keep all real-time input activity constrained in hardware, thereby relieving the Handspring CPU from being swamped with interrupt activity.

The following is a list of sensors used by Cool Trak:

- High Resolution Speed Sensor
- Cadence Sensor
- Heartrate Sensor Interface
- Humidity Sensor
- Temperature Sensor
- Altimeter/Barometer

A more detailed description of the CPLD and software design is presented later in this application note.

End Module Applications

The Cool Trak design is an ambitious one, and as such, time constraints allowed only the major functions to be implemented. Table 1 below illustrates the functionality of the Cool Trak module.

Future versions of Cool Trak will incorporate the functions listed in the "Not Implemented" column.

Table 1: **Cool Trak Functionality**

Category	Implemented	Not Implemented
Time Data	Elapsed Time Total Time	Time of Day Date Stop Watch Lap Time Interval Alarm
Speed Sensor Data	Speed Average Speed Maximum Speed Minimum Speed Trip Distance Total Distance	Distance to Go Estimated Arrival Time
Cadence Sensor Data	Cadence Gear Ratio	Gear Inches
Temperature Data	Air Temperature	-
Heart Rate Sensor Data	Heart Rate Average Heart Rate	Heart Rate in Zone Heart Rate Above Zone Heart Rate Below Zone Total Time in Zone Recovery Time
Humidity Sensor Data	Humidity	-
Altitude Sensor Data	Altitude	Climb Rate

Operating Instructions

The Cool Trak design can be downloaded from the Xilinx website. The download pack includes the necessary files needed to run the Cool Trak module, see **Download Pack**, page 10.

Starting the Application

The Cool Trak software is easy to use. Once the Cool Trak application is started from the Application Launcher, all hardware will be initialized.

Software Features

The software provides four types of information display:

1. The Summary Screen
2. The Human Factor Screen
3. The Exterior Factor Screen
4. Ride Information Screen

On the top right corner of the Cool Trak Application is the route name, shown as "Pacific Coast Hwy 1" by default.

Figure 4 shows the various graphic user interfaces in the Cool Trak Application.

Figure 4: **Cool Trak Application**

Setup

A pen tap in the route name area invokes the Setup screen and the user can choose the default setup data: Route name, Min target bpm, Max target bpm, and Total trip distance

Navigation

A pen tap in any screen area other than the Software Title (also known as menu area) makes the Route Name cycle through each of the four screens.

Resetting Trip Data

Pressing button four (the Memo Button) causes the cumulative trip data such as ride distance, average speed, maximum speed, etc. to reset to zero.

Trip Timer and Split Timer

Pressing button one (or Calendar) starts the timer from zero.

Pressing button two (or Phone Book) marks the split time and split number

Pressing button one again stops the timer.

Hardware Description

Cool Track was implemented using a total of six sensors: a Speed Sensor, a Cadence Sensor, a Heart Rate Sensor, a Temperature Sensor, a Humidity Sensor and an Altimeter. The first three sensors do not require an A/D (Analog to Digital) Converter. The last three sensors, however, use the TI ADS7870 Data Acquisition System. As shown in Figure 5, the CoolRunner device is used as the system controller. The speed, cadence and heart rate sensors are read directly by the XPLA3 CPLD. The other sensors are routed into a TI ADS7870 device which is also controlled by the CoolRunner device via a serial interface. Ultimately, the CoolRunner CPLD is used to implement logic that will allow data to be routed in to and out of the Handspring Visor Springboard Interface.

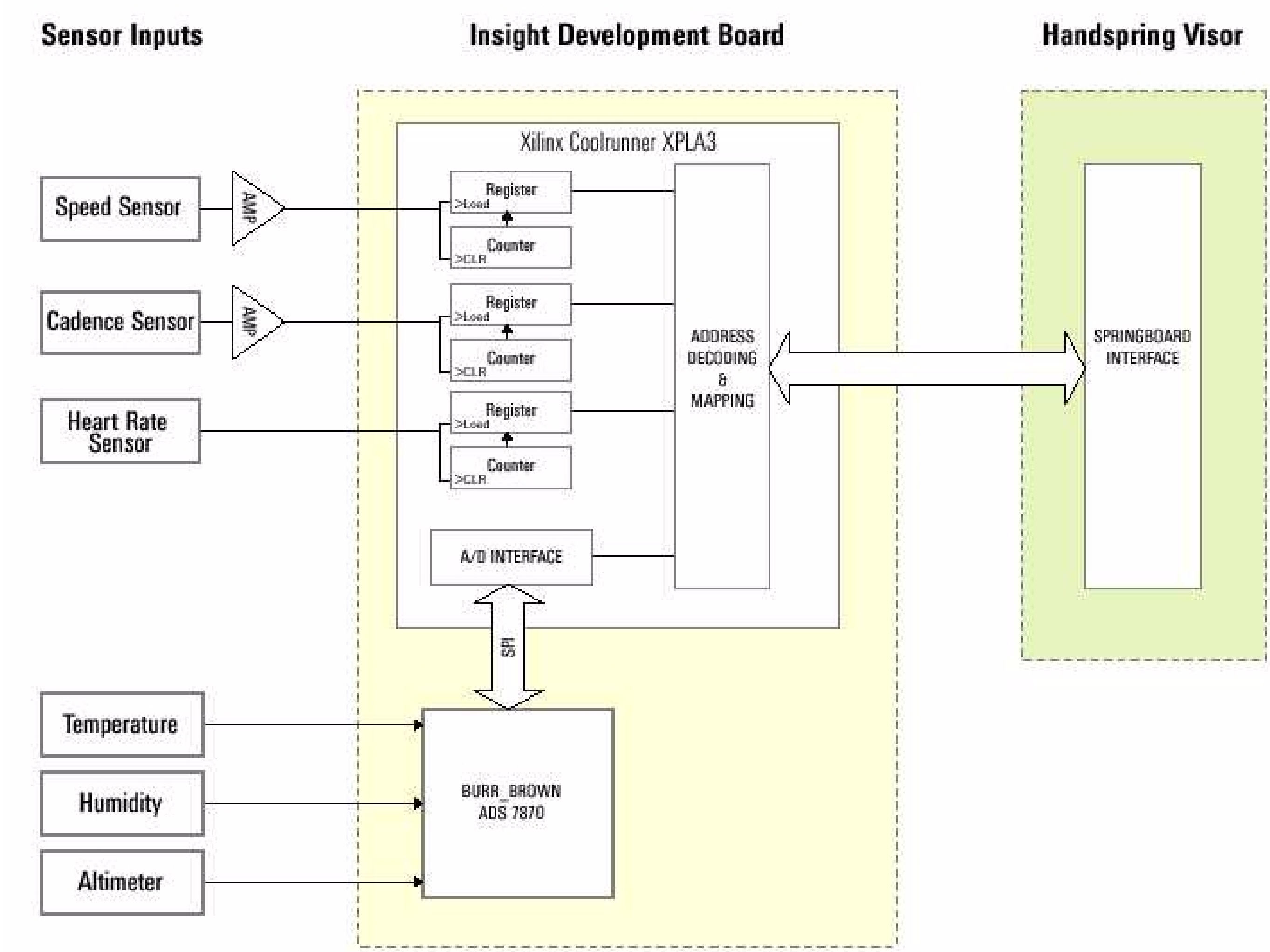

Figure 5: **Cool Trak Block Diagram**

CoolRunner XPLA3 CPLD

A CoolRunner XPLA3256XL programmable logic device is used in this design. Implemented in the CoolRunner device are three identical 10-bit resolution counters that measure speed, cadence and heart rate. The XPLA3 CPLD also provides an interface to the ADS7870 Data Acquisition System. Memory mapped registers implemented in the CPLD store the sensor results and allow the Visor to retrieve and display all measurements. The CoolRunner XPLA3 CPLD is a 3.3V device, making it ideal to connect V_{CC} of the CPLD to the Springboard's V_{CC}.

Texas Instruments ADS7870 Data Acquisition System

The TI ADS7870 Data Acquisition system (formerly manufactured by Burr-Brown) is an ultra-low power 3.3V system that contains a 12-bit serial A/D Converter. It is capable of sampling as high as 52 kilo-samples/second and can sample up to eight single-ended channels or four differential channels.

For this design, the ADS7870 Data Acquisition System is used to sample the temperature sensor, humidity sensor and the altimeter. The CoolRunner CPLD is used to provide a serial to parallel interface for the ADS7870 device.

High Resolution Speed Sensor

The speed sensor is an Avocet magnetic sensor designed for operation on a bicycle. It is mounted on the front wheel of the bicycle to determine how fast (in MPH) the bike is traveling. This sensor has 12 cycles per revolution. A differential amplifier is needed to create a signal that can be measured by the Xilinx XPLA3 CPLD. The output of this sensor is periodic. Therefore, in order to interpret the actual speed, a 10-bit counter in the CoolRunner device is used to measure output frequency. The Visor PDA takes this frequency number and translates it into an actual speed.

The differential amplifier circuit used is shown in Figure 6.

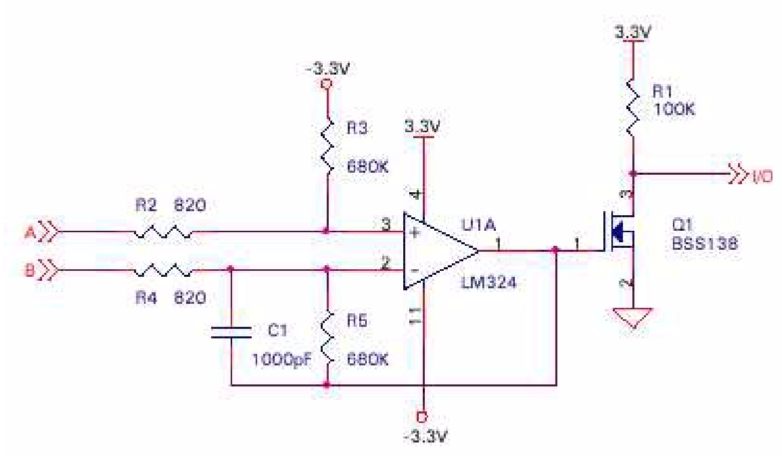

Figure 6: **Differential Amplifier Circuit**

Cadence Sensor

The cadence sensor is a duplicate of the speed sensor (an Avocet Magnetic Sensor), but it is mounted around the bicycle's crank instead of the front wheel. This allows the rider to examine his/her peddling rate in terms of rotations per minute (rpm). The same differential amplifier circuit is used as shown above in Figure 6 and again, a 10-bit counter in the CPLD measures the periodic output of the sensor. Figure 7 below shows the cadence sensor mounted on the bicycle's crank.

Figure 7: **Cadence Sensor Located On Bicycle Crank**

Heartrate Sensor Interface

Cool Trak uses a wireless, chest mounted heart rate sensor. There are several available wireless heart rate sensors of this type available in the market. Any of those could be used with Cool Trak. The Cool Trak design submission uses heart rate sensor manufactured by Polar. These sensors provide a wireless magnetic induction signal output, consisting of short 5 kHz pulses, once per heartbeat. The transmitter contains two electrodes to detect the electrical signal present on the cyclist's skin. The electrodes are mounted in a sealed transmitter. This transmitter is attached directly to the chest via an elastic belt. On every heart beat, the Polar transmitter detects the voltage differential on the skin and sends a wireless signal continuously using an electromagnetic field to the receiver. The Polar chest-mounted wireless transmitter is shown below.

Figure 8: **Polar Transmitter**

To retrieve the wireless pulses, a simple magnetic coil receiver is used to recover the pulses. Again, a 10-bit counter in the CPLD measures the period between pulses in order to determine the cyclist's heart rate.

Temperature Sensor

A thermistor is used to measure temperature using the 12-bit A/D converter in the ADS7870 Data Acquisition System. The presence of an A/D converter on the Insight Springboard Development Board helped achieve the rapid prototyping goal of the Cool Trak concept.

The thermistor circuit is shown in Figure 9

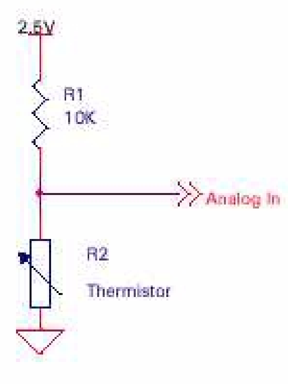

Figure 9: **Thermistor Circuit**

Humidity Sensor

The humidity sensor from JLC International is a variable capacitor. A FET is used to charge the capacitor, and the voltage is evaluated with the ADS7870 device a short time later. This allows the capacitance to be calculated. The relative humidity can be easily determined by the Handspring Visor, since the capacitance varies linearly with relative humidity.

Altimeter/Barometer

The altimeter/barometer is based on a Motorola absolute pressure sensor (MXP2100AP). The ADS7870 is used in differential mode with the input gain set to the maximum 20X. Figure 10 shows the Altimeter diagram.

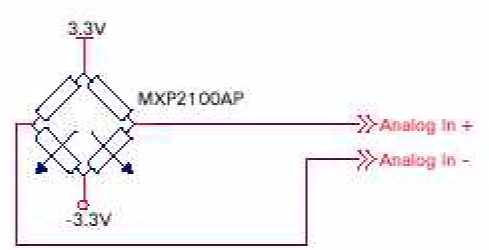

Figure 10: **Altimeter/Barometer Circuit**

CPLD Design

The design was successfully implemented in a Xilinx CoolRunner XPLA3 256 Macrocell CPLD. Table 2 shows the fitting statistics of the actual implementation. The device is approximately 77.7% utilized. It is worth noting that the CoolRunner architecture allows for 100% routability, thereby allowing it to retain the same pinout throughout numerous design changes.

Table 2: **CPLD Device Resource Summary**

Resource	Available	Used	Utilization
Clock Inputs	4	1	25.00%
Global Control Terms	4	4	100.00%
Function Blocks	16	14	87.50%
I/O Pins	160	67	41.88%
Macrocells	256	199	77.74%

Table 2: **CPLD Device Resource Summary *(Continued)***

Resource	Available	Used	Utilization
Registers	256	157	61.33%
PLA Product Terms	768	436	56.78%
PLA Sum Terms	256	181	70.71%
Block Control Terms	128	31	24.22%
Foldback Nands	128	16	12.50%

The source code and implementation results for the CPLD design is included in the available download pack (see **Download Pack**, page 10).

Download Pack

THIRD PARTIES MAY HAVE PATENTS ON COOL TRAK. BY PROVIDING THIS HDL CODE AS ONE POSSIBLE IMPLEMENTATION OF THIS DESIGN, XILINX IS MAKING NO REPRESENTATION THAT THE PROVIDED IMPLEMENTATION OF THIS DESIGN IS FREE FROM ANY CLAIMS OF INFRINGEMENT BY ANY THIRD PARTY. XILINX EXPRESSLY DISCLAIMS ANY WARRANTY OR CONDITIONS, EXPRESS, IMPLIED, STATUTORY OR OTHERWISE, AND XILINX SPECIFICALLY DISCLAIMS ANY IMPLIED WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR A PARTICULAR PURPOSE, THE ADEQUACY OF THE IMPLEMENTATION, INCLUDING BUT NOT LIMITED TO ANY WARRANTY OR REPRESENTATION THAT THE IMPLEMENTATION IS FREE FROM CLAIMS OF ANY THIRD PARTY. FURTHERMORE, XILINX IS PROVIDING THIS REFERENCE DESIGNS "AS IS" AS A COURTESY TO YOU.

XAPP370 - **http://www.xilinx.com/products/xaw/coolvhdlq.htm**

Conclusion

The Cool Trak springboard module was the $10,000 grand prize winner in the 2001 Cool Module Design Contest sponsored by Xilinx, Handspring, and Portable Design Magazine. The Xilinx CoolRunner XPLA3 CPLD played a critical role in the design of Cool Trak, as it was designated to be the main system controller. Xilinx CoolRunner CPLDs are the only ultra-low power programmable logic devices available in the market. In fact, CoolRunner CPLDs have been accepted as the de facto standard for PDA units and PDA modules.

Appendix A

Appendix A lists appropriate Xilinx CoolRunner CPLD application notes. These application notes can be found by searching the Xilinx website and keying on the specific XAPP#. Many include appropriate driver software along with high level design code. All have been constructed and work.

PDA Springboard Design

XAPP147: Low Power Handspring Springboard Module Design with CoolRunner CPLDs

XAPP359: Understanding the Insight Springboard Development Kit

XAPP357: CoolRunner Visor Springboard LED Test

XAPP355: Serial ADC Interface Using a CoolRunner CPLD

XAPP146: Designing an Eight Channel Digital Volt Meter with the Insight Springboard Kit

XAPP149: Designing an Oscilloscope for the Insight Springboard Development Kit

XAPP349: XPATH Handspring Design Module

XAPP363: Handheld Sonic Access Module

XAPP364: Handheld Sound Bouncer

XAPP365: Handheld Automotive Scan Tool

XAPP366: Handheld Musical Instrument Tuner

XAPP367: Handheld Chatterbox

XAPP368: Handheld Logic Analyzer

XAPP369: Handheld 1553 Military Bus Analyzer

References

Frog Design website: http://www.frogdesign.com/

Handspring website: http://www.handspring.com/

Avocet website: http://www.avocet.com/

Polar website: http://www.polar.fi

JLC International: http://www.jlcinternational.com/

Motorola: http://www.mot-sps.com/

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/03/02	1.0	Initial Xilinx release.