



XAPP375 (v1.0) January 3, 2002

# Understanding the CoolRunner-II Timing Model

## Summary

This document describes the CoolRunner™-II timing model. Understanding the CoolRunner-II timing model is essential to creating a CPLD design that meets the desired timing requirements.

## Introduction

CPLD designers often require an understanding of the device timing model to compare design specific timing requirements. CPLD designers can use the CoolRunner-II timing model to create a design that fits required timing requirements and compare design critical paths. Designers can use the timing model to create equations of time delays for each logic path in a design. This document will describe the CoolRunner-II timing model in detail and provide examples for using this timing model.

A brief overview of the CoolRunner-II architecture as it pertains to the timing model will be described in the following section.

## CoolRunner-II Architecture

The CoolRunner-II architecture consists of function blocks that are interconnected by a routing matrix called the Advanced Interconnect Matrix (AIM). Each function block contains a Programmable Logic Array (PLA) and 16 macrocells. A total of eight global signals are multiplexed with eight I/O pins and include three clocks, four output enables, and one set/reset signal. The CoolRunner-II architecture allows these global signals to be driven by internal logic. **Figure 1** illustrates a block diagram of the CoolRunner-II architecture.

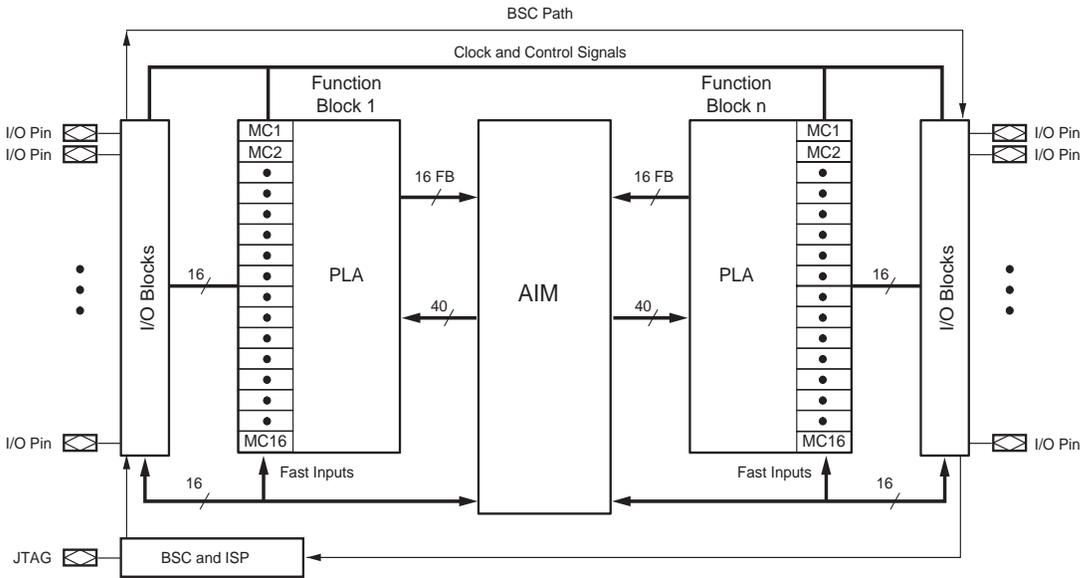


Figure 1: CoolRunner-II Architecture

The function block product term and sum term array is a pure PLA (programmable AND array, programmable OR array). Each PLA has 40 inputs from the AIM (true and complement) and contains 56 unique product terms. Product terms can be used as macrocell clocks, control

© 2002 Xilinx, Inc. All rights reserved. All Xilinx trademarks, registered trademarks, patents, and disclaimers are as listed at <http://www.xilinx.com/legal.htm>. All other trademarks and registered trademarks are the property of their respective owners. All specifications are subject to change without notice.

terms (reset, preset, asynchronous clock, clock enable, or output enable), or as needed as logic by the macrocells in the function block.

Of the function block product terms, four are available as control terms. The control terms, CTC, CTR, CTS, and CTE, can be a macrocell clock, reset, preset, or output enable. In addition to these function block control terms, each macrocell has three dedicated product terms available as additional control terms, local to that macrocell. PTA can be used as the macrocell reset or preset, PTB for the macrocell output enable, and PTC for the clock enable or product term clock. Note that if these product terms are not needed as control terms, they are available for other logic. **Figure 2** illustrates the CoolRunner-II macrocell.

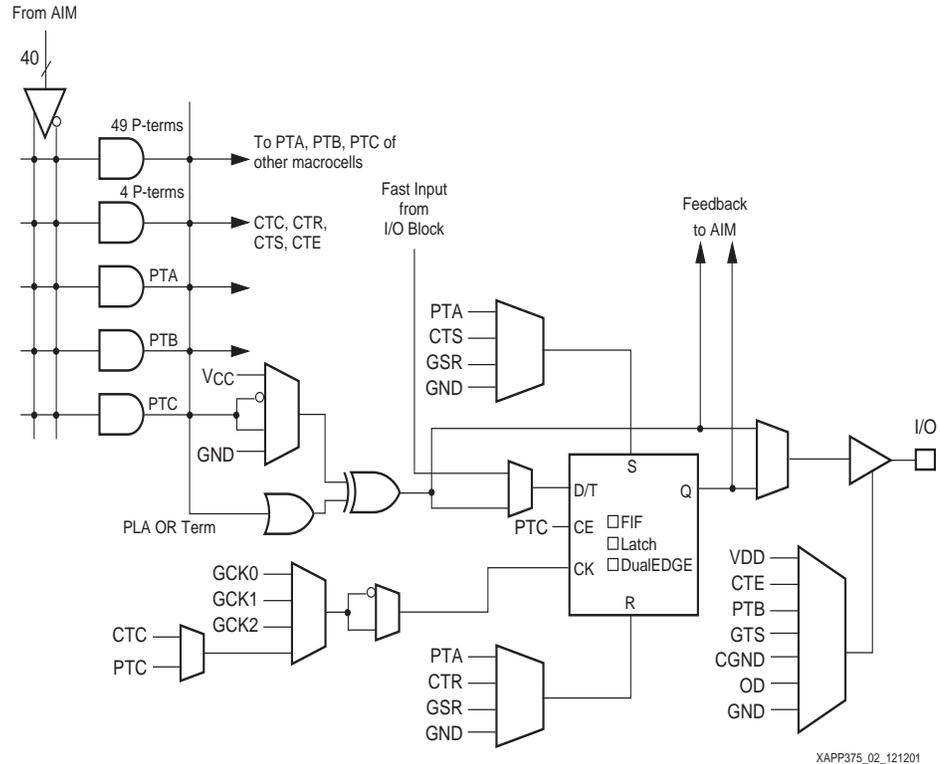


Figure 2: CoolRunner-II Macrocell

## Timing Model

### Overview

External signals enter at the pins and are delivered through the I/O block to the AIM. From the AIM, they are dispatched to the various function blocks (FBs). As the signals enter the FBs, they incur incremental time delays depending on how the signals are used within the FB. For example, all logic signals must pass through the AND array where product terms are created and a time delay is incurred as the signal progresses. The number of product terms in a logic equation will impact the time delay encountered on the signal. With the CoolRunner-II architecture, each macrocell has a fast path that contains one product term, PTC (see **Figure 2**), in a logic equation. With this path, the OR term is bypassed and fed directly into the macrocell register. Logic equations with two or more product terms must enter the OR term and will therefore encounter an additional time delay.

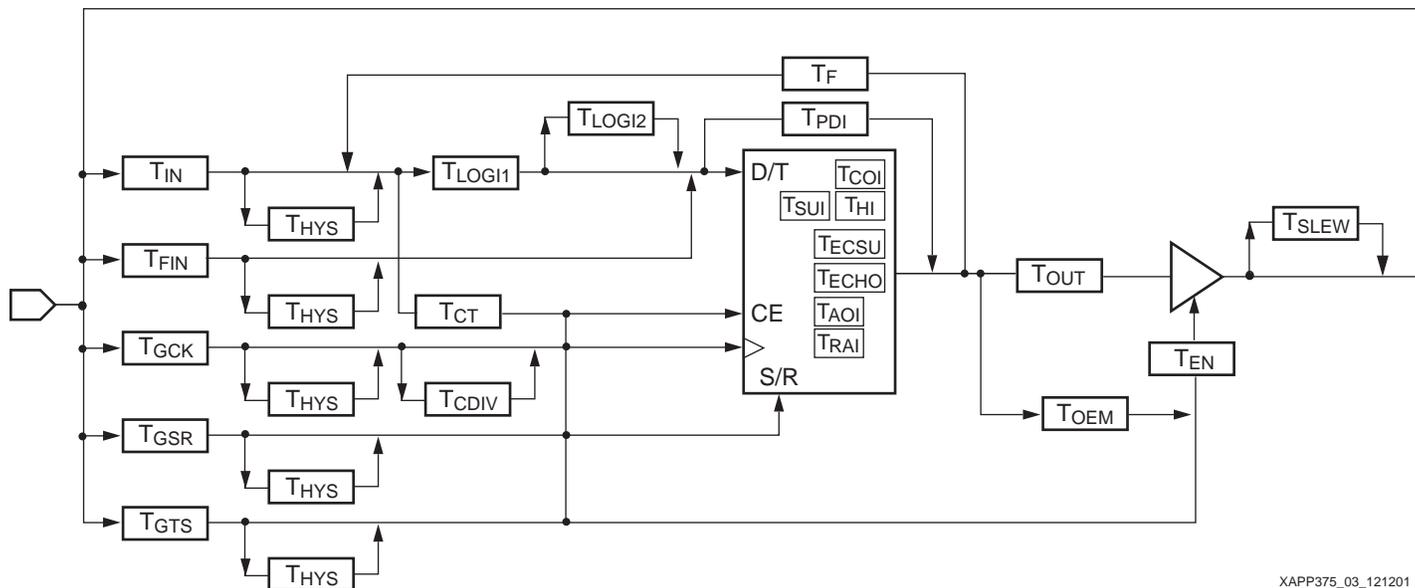
There are additional timing requirements such as setup and clock-to-output times involved when passing signals through a flip-flop. The macrocell output is either directed to the I/O block and pin, or are fed back into the AIM switch matrix for additional logic operations.

Design timing can be manually analyzed as separate signals, each having unique timing parameters that are easily calculated. However, the Xilinx development tools provide a detailed timing report that tallies and summarizes all paths specified by the designer. The timing report

is based on the model described here and is a convenient text based mechanism for isolating and displaying timing relationships.

### Description

The timing model, shown in **Figure 3**, is used by the Xilinx development software which provides complete fitting for the CoolRunner-II family as well as timing models for simulation and detailed static timing reports.



XAPP375\_03\_121201

Figure 3: CoolRunner-II Timing Model

The timing model shown in **Figure 3** represents the CoolRunner-II macrocell with additional time delays included to account for the AIM switch matrix and I/O buffers. As signals progress through a CoolRunner-II device, they encounter some of these delays which are tallied to arrive at a cumulative time delay for that signal. **Table 1** provides a detailed definition of each parameter contained in **Figure 3**. The exact values for each device can be obtained from the specific data sheets.

Table 1: CoolRunner-II Internal Timing Parameters

Parameter	Description
<b>Buffer Delays</b>	
T <sub>IN</sub>	Input buffer delay (see <b>Table 2</b> )
T <sub>FIN</sub>	Fast input buffer delay (input registers) (see <b>Table 2</b> )
T <sub>GCK</sub>	Global clock buffer delay (see <b>Table 2</b> )
T <sub>GSR</sub>	Global set/reset buffer delay (see <b>Table 2</b> )
T <sub>GTS</sub>	Global tristate buffer delay (see <b>Table 2</b> )
T <sub>OUT</sub>	Output buffer delay (see <b>Table 2</b> )
T <sub>EN</sub>	Output buffer enable/disable delay
<b>Product Term Delays</b>	
T <sub>CT</sub>	Control term delay (single P-term or FB control term)
T <sub>LOG1</sub>	Internal logic delay (single P-term)
T <sub>LOG2</sub>	Multiple P-term delay adder

Table 1: CoolRunner-II Internal Timing Parameters (Continued)

Parameter	Description
<b>Internal Register and Combinatorial Delays</b>	
$T_{PDI}$	Macrocell input to output valid
$T_{SUI}$	Macrocell register setup time
$T_{HI}$	Macrocell register hold time
$T_{ECSU}$	Macrocell register clock enable setup time
$T_{ECHO}$	Macrocell register clock enable hold time
$T_{COI}$	Macrocell register clock to output delay
$T_{AOI}$	Macrocell register set/reset to output delay
$T_{RAI}$	Macrocell register set/reset recovery before clock
<b>Feedback Delays</b>	
$T_F$	AIM delay
$T_{OEM}$	Macrocell to global output enable delay
<b>Time Delays</b>	
$T_{HYS}$	Hysteresis time delay (see Table 2)
$T_{SLEW}$	Slew rate limited delay (see Table 2)
$T_{CDIV}$	Clock divider delay adder

The CoolRunner-II architecture features a selectable clock divider available on global clock, GCK2. Note that the clock divider feature is available only on CoolRunner-II 128 macrocell devices and larger.

Table 2 illustrates various timing parameters associated with the available I/O standards on CoolRunner-II devices. Note that the SSTL and HSTL standards are only available on 128 macrocell and larger CoolRunner-II CPLDs. Values for the parameters shown in Table 2 are available in the specific product data sheet. Note that values shown in Table 2 are timing delay adders.

Table 2: I/O Standard Related Timing Parameters

Parameter	Description
<b>1.8V LVCMOS</b>	
$T_{IN18}$	Input buffer adder for $T_{IN}$ , $T_{FIN}$ , $T_{GCK}$ , $T_{GSR}$ , and $T_{GTS}$
$T_{HYS18}$	Input hysteresis input adder for $T_{IN}$ , $T_{FIN}$ , $T_{GCK}$ , $T_{GSR}$ , and $T_{GTS}$
$T_{OUT18}$	Output delay adder
$T_{SLEW18}$	Output slew adder
<b>2.5V LVCMOS</b>	
$T_{IN25}$	Input buffer adder for $T_{IN}$ , $T_{FIN}$ , $T_{GCK}$ , $T_{GSR}$ , and $T_{GTS}$
$T_{HYS25}$	Input hysteresis input adder for $T_{IN}$ , $T_{FIN}$ , $T_{GCK}$ , $T_{GSR}$ , and $T_{GTS}$
$T_{OUT25}$	Output delay adder
$T_{SLEW25}$	Output slew adder

Table 2: I/O Standard Related Timing Parameters (Continued)

Parameter	Description
<b>3.3V TTL/LVCMOS</b>	
$T_{IN33}$	Input buffer adder for $T_{IN}$ , $T_{FIN}$ , $T_{GCK}$ , $T_{GSR}$ , and $T_{GTS}$
$T_{HYS33}$	Input hysteresis input adder for $T_{IN}$ , $T_{FIN}$ , $T_{GCK}$ , $T_{GSR}$ , and $T_{GTS}$
$T_{OUT33}$	Output delay adder
$T_{SLEW33}$	Output slew adder
<b>SSTL2-I</b>	
$T_{INSS2}$	Input buffer adder for $T_{IN}$ , $T_{FIN}$ , $T_{GCK}$ , $T_{GSR}$ , and $T_{GTS}$
$T_{OUTSS2}$	Output delay adder
<b>SSTL3-I</b>	
$T_{INSS3}$	Input buffer adder for $T_{IN}$ , $T_{FIN}$ , $T_{GCK}$ , $T_{GSR}$ , and $T_{GTS}$
$T_{OUTSS3}$	Output delay adder
<b>HSTL-I</b>	
$T_{INHS1}$	Input buffer adder for $T_{IN}$ , $T_{FIN}$ , $T_{GCK}$ , $T_{GSR}$ , and $T_{GTS}$
$T_{OUTH1}$	Output delay adder

### External Timing Parameters

Table 3 shows how key external timing parameters are derived from the internal timing parameters.

Table 3: Expressions for External Timing Parameters

Parameter	Description	Equation
$T_{PD1}$	Propagation delay time (single P-term)	$T_{IN} + T_{LOG11} + T_{PDI} + T_{OUT}$
$T_{PD2}$	Propagation delay time (OR array)	$T_{IN} + T_{LOG11} + T_{LOG12} + T_{PDI} + T_{OUT}$
$T_{SU1}$	Fast input register setup time	$T_{FIN} + T_{SUI} - T_{GCK}$
$T_{SU2}$	Setup time	$T_{IN} + T_{LOG11} + T_{LOG12} + T_{SUI} - T_{GCK}$
$T_{H1}$	Fast input register hold time	$T_{GCK} [+ T_{CDIV}] + T_{HI} - T_{FIN}^{(1)}$
$T_{H2}$	Hold time	$T_{GCK} [+ T_{CDIV}] + T_{HI} - T_{IN} - T_{LOG11}^{(1)}$
$T_{CO}$	Clock to output (global synchronous clock pin)	$T_{GCK} [+ T_{CDIV}] + T_{COI} + T_{OUT}$
$T_{CYCLE}$	Minimum clock period	$T_{COI} + T_F + T_{LOG11} + T_{LOG12} + T_{SUI}$
$f_{SYSTEM}$	Maximum system frequency	$1/T_{CYCLE}$
$f_{EXT}$	Maximum external frequency	$1/(T_{SU2} + T_{CO})$
$T_{PSU1}$	Fast input register P-term clock setup time	$T_{FIN} + T_{SUI} - T_{IN} - T_{CT}$
$T_{PSU2}$	P-term clock setup time	$T_{IN} + T_{LOG11} + T_{LOG12} + T_{SUI} - T_{IN} - T_{CT}$
$T_{PH1}$	Fast input register P-term clock hold time	$T_{IN} + T_{CT} + T_{FIN} + \text{skew}$
$T_{PH2}$	P-term clock hold	$T_{IN} + T_{CT} + T_{HI} - T_{IN} - T_{LOG11}^{(1)}$
$T_{PCO}$	P-term clock to output	$T_{IN} + T_{CT} + T_{COI} + T_{OUT}$
$T_{OE}/T_{OD}$	Global OE to output enabled/disabled	$T_{GTS} + T_{EN}$
$T_{POE}/T_{POD}$	P-term OE to output enabled/disabled	$T_{IN} + T_{CT} + T_{EN}$

Table 3: Expressions for External Timing Parameters (Continued)

Parameter	Description	Equation
$T_{MOE}/T_{MOD}$	Macrocell driven OE to output enabled/disabled	$T_{GCK} [+ T_{CDIV}] + T_{COI} + T_{OEM} + T_{EN}$
$T_{PAO}$	P-term set/reset to output set/reset	$T_{IN} + T_{CT} + T_{AOI} + T_{OUT}$
$T_{AO}$	Global set/reset to output set/reset	$T_{GSR} + T_{AOI} + T_{OUT}$
$T_{SUEC1}$	Fast input register clock enable setup time	$T_{FIN} + T_{ECSU} - T_{GCK} [- T_{CDIV}]$
$T_{SUEC2}$	Register clock enable setup time	$T_{IN} + T_{LOGI1} + T_{LOGI2} + T_{ECSU} - T_{GCK} [- T_{CDIV}]$
$T_{HEC1}$	Fast input register clock enable hold time	$T_{GCK} [+ T_{CDIV}] + T_{ECHO} - T_{FIN}$
$T_{HEC2}$	Register clock enable hold time	$T_{GCK} [+ T_{CDIV}] + T_{ECHO} - T_{IN} - T_{LOGI1}$
$T_{CW}$	Global clock pulse width (high or low)	Please see product data sheet
$T_{PCW}$	P-term clock pulse width (high or low)	Please see product data sheet

**Notes:**

1. All CoolRunner-II devices guarantee a zero hold time, even though the equations shown here may create a negative hold time value.

Please note that these times will change if multiple feedback passes (internal nodes) are used. The following sections provide a few examples of how the device timing is calculated. These calculations are automatically done for the user by software development tools but examples are provided here to help the user better understand how the software calculates device timing. Please note these examples do not cover every possible case.

## Combinatorial Timing Examples

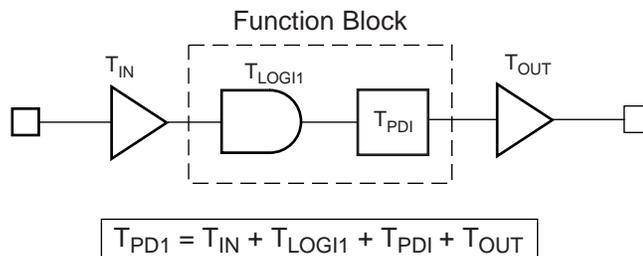
This section provides various combinatorial timing examples. The examples provided here include propagation delay with a single P-term, multiple P-terms, and multiple levels of logic.

One combinatorial timing example is propagation delay, or  $T_{PD}$ . CoolRunner-II  $T_{PD}$  is separated into two individual timing parameters,  $T_{PD1}$  and  $T_{PD2}$ .  $T_{PD1}$  is calculated based on a single P-term path in the PLA structure.  $T_{PD2}$  is calculated based on more than one P-term existing in the data path.

### Single Product Term Propagation Delay

The CoolRunner-II architecture provides a fast path  $T_{PD}$  with a single product term logic equation. With a single P-term logic equation, the OR term can be bypassed, and the P-term is fed directly in the macrocell using PTC (see Figure 2).

$T_{PD1}$  is calculated as the sum of the input buffer time delay ( $T_{IN}$ ), the single P-term logic time delay ( $T_{LOGI1}$ ), the bypass path of the macrocell ( $T_{PDI}$ ), and the output buffer time delay ( $T_{OUT}$ ), as shown in Figure 4. Note that the input buffer delay is combined with the AIM time delay since the entering signal passes through the AIM switch matrix.

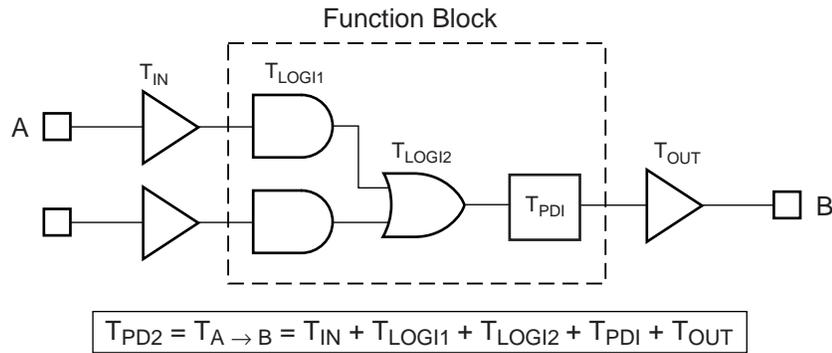


XAPP375\_04\_121301

Figure 4:  $T_{PD1}$  with a Single Product Term

### Multiple Product Term Propagation Delay

Figure 5 illustrates a variation to the simple  $T_{PD1}$  example with the addition of more product terms. The time delay from input A is slightly altered with  $T_{PD2}$ , which accounts for additional product terms.  $T_{PD2}$  is the same independent of the number of product terms, ranging from 2 to 56.

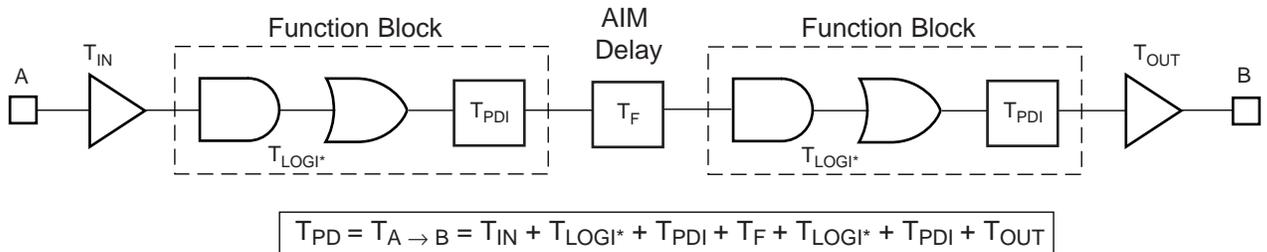


XAPP375\_05\_112701

Figure 5:  $T_{PD2}$  with 2 to 56 Product Terms

### Multiple Logic Level Propagation Delay

If combinational data requires multiple passes of logic,  $T_{PD}$  will increase accordingly. Figure 6 illustrates the case where  $T_{PD}$  is calculated based on cascaded levels of logic. In this case, there is a single pass through the input buffer, a pass through the function block logic, a pass through the feedback path, an additional pass through the function block logic, and the output buffer.



XAPP375\_06\_112701

Figure 6:  $T_{PD}$  with Two Levels of Logic

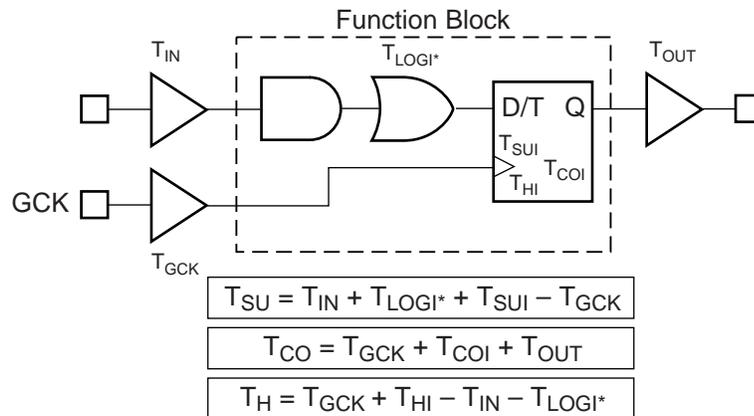
**Note:**  $T_{LOGI*} = T_{LOGI1}$  if a single P-term is used, and  $T_{LOGI*} = T_{LOGI1} + T_{LOGI2}$  if 2 to 56 P-terms are used.

## Registered Timing Examples

### Simple Registered Path

A simple registered timing example is shown in Figure 7 which illustrates a macrocell flip-flop with a CoolRunner-II global synchronous clock signal, GCK. The equations for  $T_{SU}$ ,  $T_{CO}$ , and  $T_H$  are valid for this arrangement. In this example, the equations for  $T_{SU}$ ,  $T_{CO}$ , and  $T_H$  are not for fast input register or any special clocking features, i.e., divider or doubler. An example of

these will be discussed later in the document. The equations shown in Figure 7 are closely related to  $T_{SU2}$ ,  $T_{CO}$ , and  $T_{H2}$  described in Table 3.

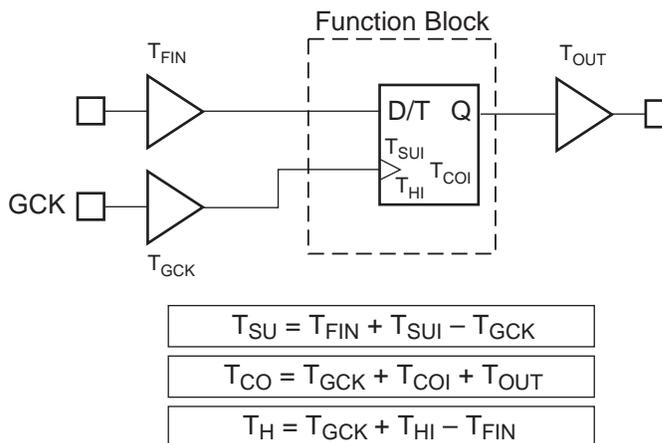


XAPP375\_07\_112801

Figure 7: Simple Registered Path

### Fast Input Register

Figure 8 illustrates the CoolRunner-II fast input register architecture feature. Fast input registers allow a designer to capture data from a high speed external bus with minimal  $T_{SU}$ . The equations shown in Figure 8 are closely related to  $T_{SU1}$ ,  $T_{CO}$ , and  $T_{H1}$  described in Table 3.



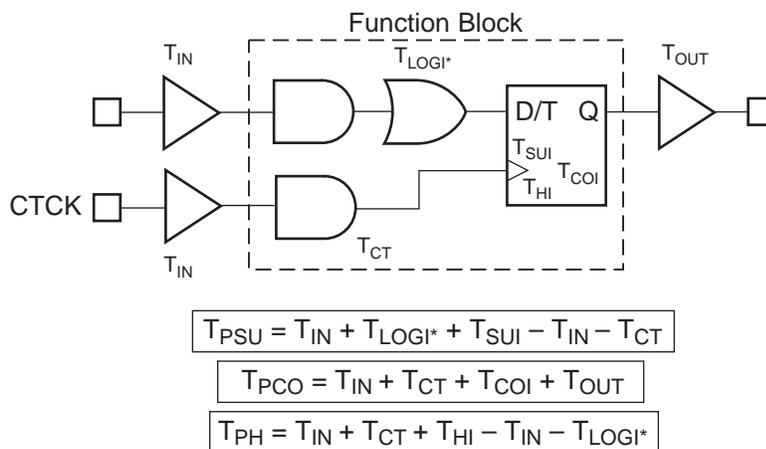
XAPP375\_08\_112801

Figure 8: Fast Input Register Path

### Product Term Clocking

Another architectural feature available in CoolRunner-II is product term register clocking. Product terms clocks available in each CoolRunner-II macrocell include, CTC and PTC shown in Figure 2. PTC is dedicated to each macrocell, while CTC is shared among macrocells within a function block. Figure 9 illustrates the timing parameters for product term clocking on a single flip-flop. This implementation is similar to Figure 7 except the clock source is now a

product/control term. The timing parameters,  $T_{PSU}$ ,  $T_{PCO}$ , and  $T_{PH}$  shown in Figure 9 are closely related to the equations for  $T_{PSU2}$ ,  $T_{PCO}$ , and  $T_{PH2}$  described in Table 3.

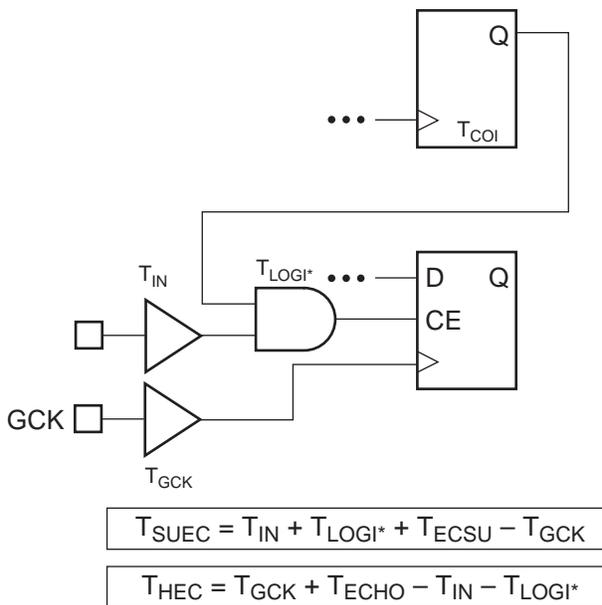


XAPP375\_09\_112801

Figure 9: Product Term Clocking

### Register Clock Enable

CoolRunner-II CPLDs provide true clock enables at each flip-flop as shown in Figure 10. Each macrocell has one dedicated clock enable, PTC. The clock enable has both setup ( $T_{SUEC}$ ) and hold ( $T_{HEC}$ ) timing parameters. The  $T_{SUEC}$  and  $T_{HEC}$  equations shown in Figure 10 are closely related to  $T_{SUEC2}$  and  $T_{HEC2}$  shown in Table 3.



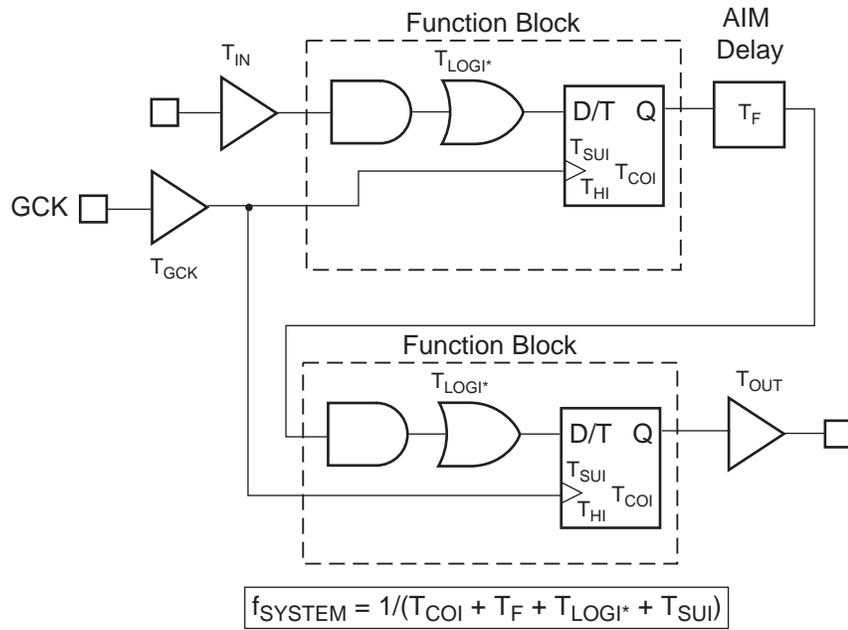
XAPP375\_10\_112801

Figure 10: Clock Enable Timing Parameters

### Registered Logic with Multiple Levels

Figure 11 illustrates multiple levels of logic clocked by the global clock, GCK. The calculation for maximum system frequency is shown in Figure 11. Maximum system frequency is determined by the time delay of one flip-flop output to the next flip-flop input. As shown in Figure 11,  $f_{SYSTEM}$

is determined by the first flip-flop output,  $T_{CO}$ , the AIM feedback delay,  $T_F$ , the delay through the PLA,  $T_{LOGI^*}$ , and the register setup time,  $T_{SUI}$ .



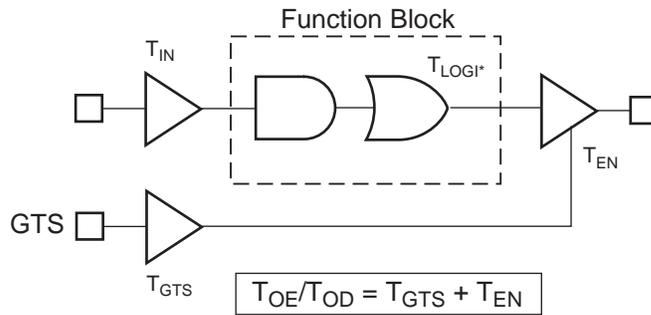
XAPP375\_11\_112801

Figure 11: Multiple Logic Levels

**I/O Related  
Timing  
Examples**

**Global Output Enable**

Output enable timing can be calculated for both the CoolRunner-II global output enable, GTS and product term driven OE control. The timing delay from the CoolRunner-II global output enable, GTS to enabling or disabling the output is shown in Figure 12.

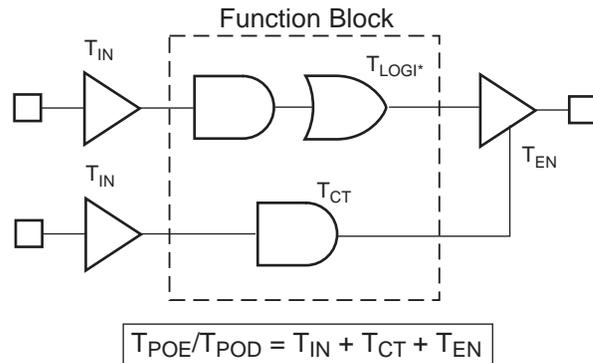


XAPP375\_12\_112801

Figure 12: Global Output Enable Timing

### Product Term Output Enable

For product output enable control, each macrocell has one dedicated OE and one function block OE control shown in Figure 2. The timing parameters when using one of these product term driven output enables is shown in Figure 13.

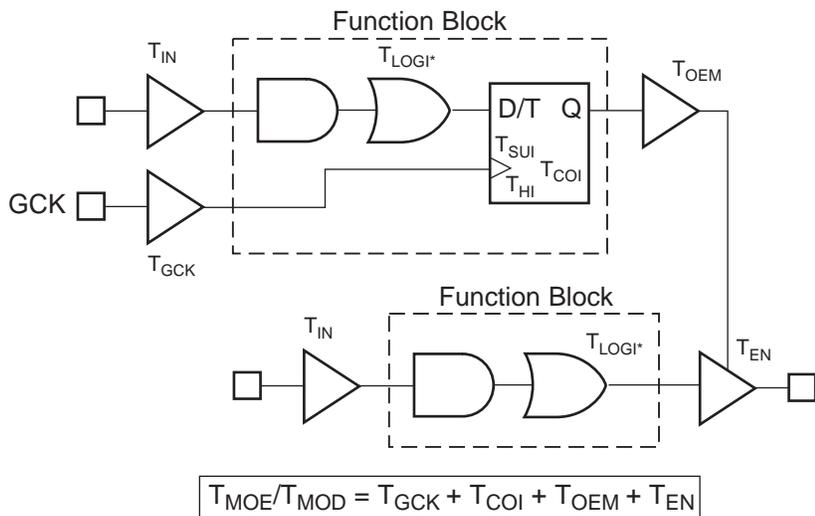


XAPP375\_13\_112801

Figure 13: Product Term Output Enable Timing

### Macrocell Driven Output Enable

The CoolRunner-II architecture also allows a macrocell to drive the global output enable. The macrocell output can be routed to one of the four available global output enables, GTS[3:0]. Figure 14 illustrates this case and the associated  $T_{MOE}/T_{MOD}$  timing parameters. Note the lower function block drawing is for the data output.



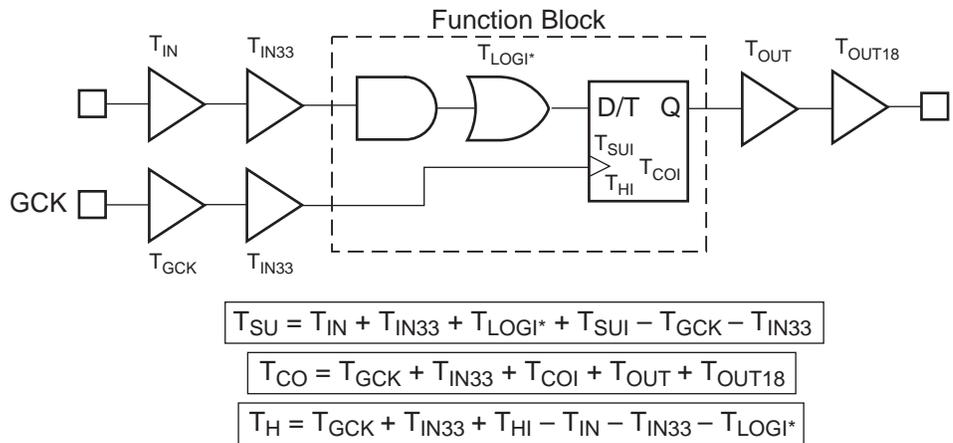
XAPP375\_14\_112801

Figure 14: Macrocell Driven Output Enable Timing

### I/O Standard Timing

Figure 15 illustrates a registered timing example using multiple I/O standards. This example utilizes 3.3V LVCMOS tolerant inputs and drives 1.8V LVCMOS outputs. Note the addition of the 3.3V LVCMOS timing delay,  $T_{IN33}$  on both the data and GCK inputs. Also note the addition

of the 1.8V LVCMOS output delay,  $T_{OUT18}$ . The associated  $T_{SU}$ ,  $T_{CO}$  and  $T_H$  timing parameters are shown in Figure 15.



XAPP375\_15\_112901

Figure 15: I/O Standard Timing Example

These examples should start to illustrate how timing parameters are calculated from the Xilinx software tools. When calculating register hold times, skew should also be accounted in the equation. Other timing delays, such as  $T_{SLEW}$  are easily added to the output timing requirements.

## Conclusion

Studying the CoolRunner-II timing model should provide a basic understanding of how timing parameters are calculated. Understanding the timing model allows designers to maximize system performance in any CoolRunner-II CPLD design.

## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/03/02	1.0	Initial Xilinx release.