Virtex-II DSP Engines Enable Software Defined Radio

Use Virtex-II FPGAs to create high-performance, flexible SDR systems.

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Migrating an existing communication infrastructure from one generation to another is enormously expensive, requiring service providers and operators to make significant investments in new hardware equipment. To address this problem, the industry has developed a software upgradeable communication system known as Software Defined Radio (SDR). This concept is enabled by new and extremely fast FPGAs, such as the Virtex™-II family, that are designed for programmable, high performance, digital signal processing.

SDR solutions require high data sample rates and channel integration, creating the need for very high-performance, yet fully programmable, digital signal processing designs. The conventional digital signal processor (DSP)-based solution cannot meet this need. For example, today's cutting edge analog to digital converters deliver data rates of over 100 Mega Samples per Second (MSPS) with 12 to 14-bit resolution. The performance of a traditional DSP device falls short by an order of magnitude – a new way of processing data is needed if you are to take advantage of the SDR concept and meet the challenges created by future wireless communication standards.

Virtex-II FPGAs – Ideal for SDR

SDR solutions are required to perform many sophisticated signal processing tasks, including advanced compression algorithms, power control, channel estimation, equalization, forward error correction, adaptive antennas, rake processing, and protocol management. While there is a plethora of silicon alternatives available for implementing these functions, such as traditional DSPs and Application Specific Integrated Circuits (ASICs), FPGAs are ideal solutions and are often the only option.

Advanced process technology has enabled us to develop high-density FPGA devices that are extremely well suited to the needs of high-performance real-time signal processing. The Virtex-II family provides a valuable combination of high performance and configurability – both required for SDR systems.

Example SDR Applications

An example of an SDR system is shown in Figure 1. Digital filters are at the heart of the system. On the transmit side these filters help shape and translate a signal from the baseband to the Intermediate Frequency (IF) before it is converted to an analog signal and sent by the antenna. On the receive side, filters are used in the digital down converter, in the channel equalizer, and for the digital re-sampling of a signal in the timing recovery and acquisition loop. With recent FPGA technology, these essential filter functions are easily designed using the highly parallel structure of a Virtex-II FPGA. Figure 2 shows how the Virtex-II platform can be used to implement a "farm" of forward error correction (FEC) algorithms.

Extreme DSP Performance

The digital filter used most often within an SDR is the Finite Impulse Response (FIR) filter. There are multiple ways to implement a FIR filter within an FPGA.
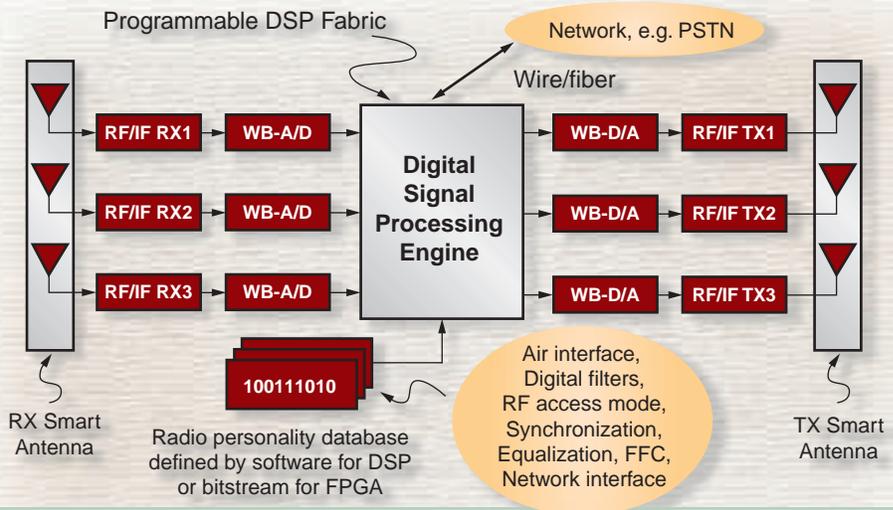

Figure 1 - SDR system diagram

However, the most common approach is to use a multiply-accumulate (MAC) unit. Depending on the performance required, you may need multiple MAC units for your filter design. The Virtex-II architecture is ideal for implementing multiple MACs. The performance of Virtex-II-based DSPs already exceeds 128 billion MACs per second. This is significantly higher than that of conventional DSPs available from mainstream DSP suppliers. Virtex-II FPGAs can extend this performance capability to 600 billion MACs per second because of the highly parallel architecture within the device.

In addition to implementing billions of MACs per second, Virtex-II FPGAs give you virtually complete control of the silicon. This enables you to decide how much real estate to allocate for the MAC units and determine the necessary performance/area trade-offs that all designs require. You can combine the MAC units, used to create the digital filter within the SDR solution, with additional Virtex-II resources to create a sophisticated, high-performance DSP engine.

Additional DSP-enhancing features include configurable dual-port block memories, distributed RAM, and multiplier arrays. The block and distributed memories are ideal for storing large amounts of data, required in the calculations for wireless standards. The multiplier array allows the system to have anywhere from 4 to 192 multipliers. Therefore, you can implement complex SDR designs in very compact solutions. The flexibility of the Virtex fabric enables you to replace multiple DSP processors, often referred to as a DSP farm, with a few Virtex-II devices. Not only does this reduce board complexity, but it also reduces power consumption.

Flexibility

One of the key aspects of an SDR system is that the same hardware can support multiple standards. Additionally, the continuing evolution of communication standards and the competitive pressures in the marketplace dictate that you must start your design and development while standards are still fluid. The flexible Virtex-II fabric enables you to control, integrate, and adapt critical DSP algorithms within the signal-processing engine.
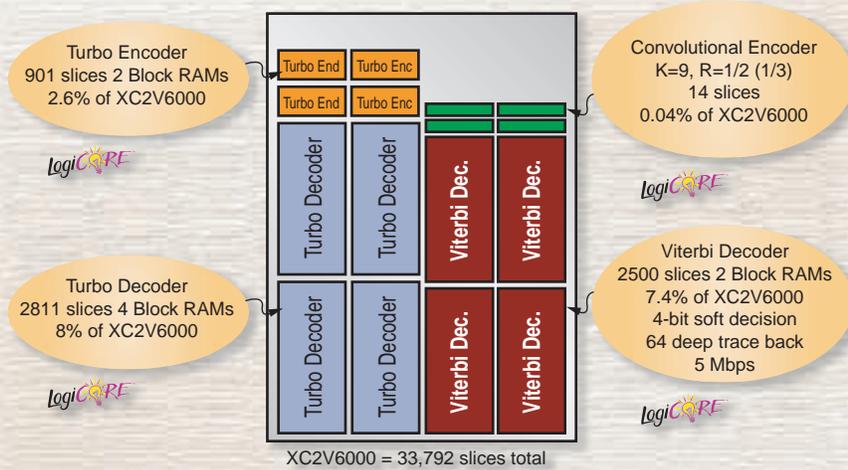

Figure 2. Virtex-II Integrates a 3G FEC Farm

As the SDR standard develops, more and more of the design will become digital. Using an FPGA, you can optimize and incorporate more and more of the digital functionality without adding more hardware – your system architecture grows and develops as the standards grow and develop. Additionally, you aren't locked into one design and you don't need go through the risks, the costs, and the long delays of respinning an ASIC solution.

The Complete SDR Solution

In addition to the Virtex-II platform FPGA, Xilinx is expanding the XtremeDSP™ Initiative to support SDR. As part of the initiative, Xilinx and its partners are providing Virtex-II development boards and a wide range of pre-engineered DSP-related algorithms including a Viterbi Decoder and a Turbo Codec.

Xilinx also offers a complete solution for general DSP development and has made significant advances to dramatically shorten the FPGA DSP design cycle. To enhance productivity, Xilinx has over 70 DSP algorithms (cores) that you can use to shorten development time and accelerate time-to-market. These solutions enable you to get to market quickly using proven technology. A complete list can be found on the Xilinx IP Center at *www.xilinx.com/ipcenter*.

Two examples of productivity enhancing DSP tools are The MathWorks System Generator for Simulink and the Filter Generator. The System Generator bridges the gap between FPGA and conventional DSP design flows. It enables you to develop DSP designs using the familiar Simulink/MATLAB tools. The Filter Generator is unlike any other filter tool in the market. Not only does it speed up the otherwise lengthy process of filter design, but it also has the ability to generate the most optimal area for a given performance level or degree of parallelism.

Conclusion

The Xilinx Virtex-II solution is uniquely positioned to meet the digital signal processing requirements demanded by SDR. Through the XtremeDSP Initiative, Xilinx provides the performance, flexibility, and productivity you need. The Virtex-II architecture delivers the platform for creating high performance, flexible, and upgradeable SDR systems. Parameterizable algorithms, partnerships with industry leaders, and third party development boards enable you to get to market quickly by using proven technologies. Additional details are available on the Xilinx DSP website at: *www.xilinx.com/dsp/*.